

## CD4013B CMOS Dual D-Type Flip-Flop

## 1 Features

- Asynchronous Set-Reset Capability
- Static Flip-Flop Operation
- Medium-Speed Operation: 16 MHz (Typical) Clock Toggle Rate at 10-V Supply
- Standardized Symmetrical Output Characteristics
- Maximum Input Current Of 1- $\mu$ A at 18 V Over Full Package Temperature Range:
  - 100 nA at 18 V and 25°C
- Noise Margin (Over Full Package Temperature Range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V

## 2 Applications

- Power Delivery
- Grid Infrastructure
- Medical, Healthcare, and Fitness
- Body Electronics and Lighting
- Building Automation
- Telecom Infrastructure
- Test and Measurement

### 3 Description

The CD4013B device consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and  $\bar{Q}$  outputs. These devices can be used for shift register applications, and, by connecting  $\bar{Q}$  output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

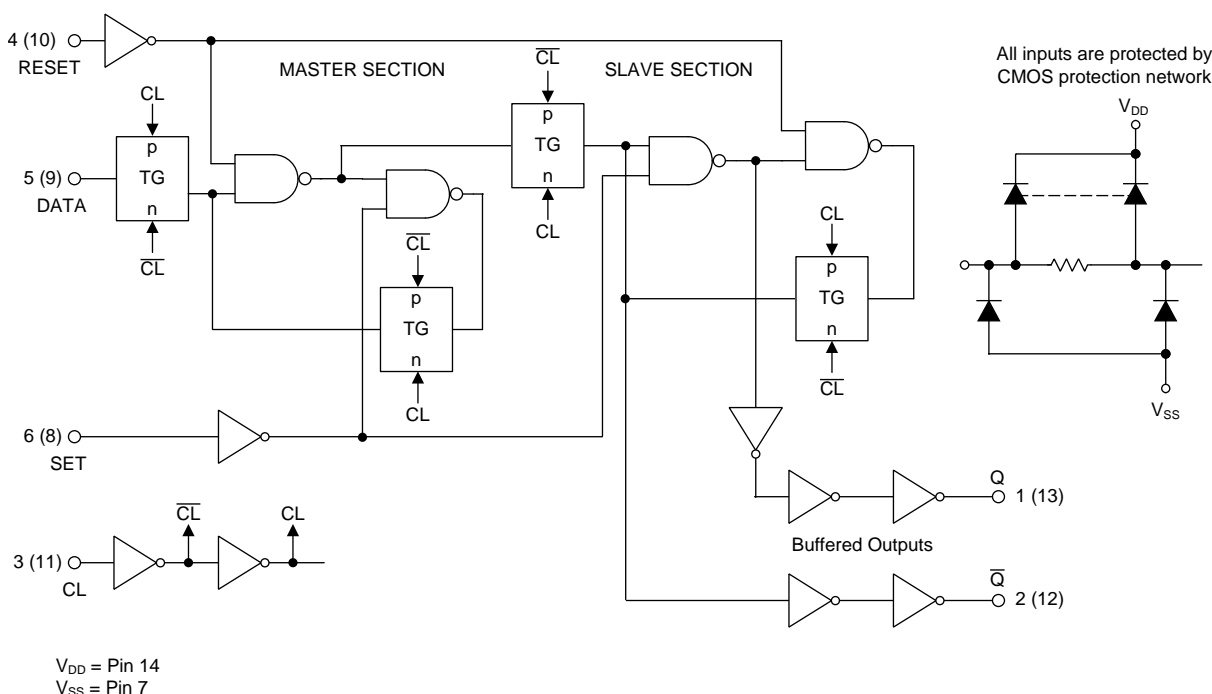
The CD4013B types are supplied in 14-pin dual-inline plastic packages (E suffix), 14-pin small-outline packages (M, MT, M96, and NSR suffixes), and 14-pin thin shrink small-outline packages (PW and PWR suffixes).

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD4013BE	PDIP (14)	19.30 mm x 6.35 mm
CD4013BF	CDIP (14)	19.50 mm x 6.92 mm
CD4013BM	SOIC (14)	8.65 mm x 3.90 mm
CD4013BNS	SO (14)	10.20 mm x 5.30 mm
CD4013BPW	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Logic Diagram



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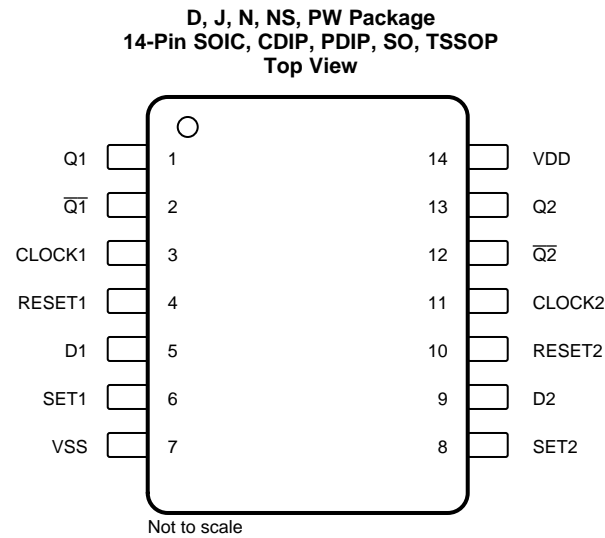
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## 4 Revision History

Changes from Revision D (March 2005) to Revision E	Page
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>
<ul style="list-style-type: none"> <li>Added <i>Thermal Information</i> table .....</li> </ul>	<b>5</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Q1	O	Channel 1 output
2	$\overline{Q1}$	O	Inverted channel 1 output
3	CLOCK1	I	Channel 1 clock input
4	RESET1	I	Channel 1 reset
5	D1	I	Channel 1 data input
6	SET1	I	Channel 1 set
7	V <sub>SS</sub>	—	Ground
8	SET2	I	Channel 2 set
9	D2	I	Channel 2 data input
10	RESET2	I	Channel 2 reset
11	CLOCK2	I	Channel 2 clock input
12	$\overline{Q2}$	O	Inverted channel 2 output
13	Q2	O	Channel 2 output
14	V <sub>DD</sub>	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
DC supply voltage, $V_{DD}$ <sup>(2)</sup>	−0.5	20	V
Input voltage, all inputs	−0.5	$V_{DD} + 0.5$	V
DC input current, any one input		10	mA
Power dissipation, $P_D$	$T_A = -55^{\circ}\text{C}$ to $100^{\circ}\text{C}$	500	mW
	$T_A = 100^{\circ}\text{C}$ to $125^{\circ}\text{C}$ <sup>(3)</sup>	200	
Device dissipation per output transistor		100	mW
Operating temperature, $T_A$	−55	125	$^{\circ}\text{C}$
Storage temperature, $T_{stg}$	−65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltages reference to  $V_{SS}$  terminal
- (3) Derate linearity at 12 mW/ $^{\circ}\text{C}$

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage		3		18	V
$t_S$ Data setup time	$V_{DD} = 5$	40			ns
	$V_{DD} = 10$	20			
	$V_{DD} = 15$	15			
$t_W$ Clock pulse width	$V_{DD} = 5$	140			ns
	$V_{DD} = 10$	60			
	$V_{DD} = 15$	40			
$f_{CL}$ Clock input frequency	$V_{DD} = 5$	3.5	7		MHz
	$V_{DD} = 10$	8	16		
	$V_{DD} = 15$	12	24		
$t_{rCL}^{(1)}$ $t_{fCL}$ Clock rise or fall time	$V_{DD} = 5$			15	$\mu\text{s}$
	$V_{DD} = 10$			10	
	$V_{DD} = 15$			5	
$t_W$ Set or reset pulse width	$V_{DD} = 5$	180			ns
	$V_{DD} = 10$	80			
	$V_{DD} = 15$	50			

- (1) If more than one unit is cascaded in a parallel clocked operation,  $t_{rCL}$  must be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	CD4013B				UNIT
	N (PDIP)	D (SOIC)	NS (SO)	PW (TSSOP)	
	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	47.1	92.5	89.3	121	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	34.5	54	47.1	49.6	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	27.1	46.8	48	62.7	°C/W
$\Psi_{JT}$ Junction-to-top characterization parameter	19.4	19	17	5.9	°C/W
$\Psi_{JB}$ Junction-to-board characterization parameter	27	46.5	47.7	62.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics: Static

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{DDmax}$ Quiescent device current	$V_{IN} = 0$ or 5, $V_{DD} = 5$	$T_A = -55^{\circ}\text{C}$			1	$\mu\text{A}$
		$T_A = -40^{\circ}\text{C}$			1	
		$T_A = 25^{\circ}\text{C}$		0.02	1	
		$T_A = 85^{\circ}\text{C}$			30	
		$T_A = 125^{\circ}\text{C}$			30	
	$V_{IN} = 0$ or 10, $V_{DD} = 10$	$T_A = -55^{\circ}\text{C}$			2	
		$T_A = -40^{\circ}\text{C}$			2	
		$T_A = 25^{\circ}\text{C}$		0.02	2	
		$T_A = 85^{\circ}\text{C}$			60	
		$T_A = 125^{\circ}\text{C}$			60	
	$V_{IN} = 0$ or 15, $V_{DD} = 15$	$T_A = -55^{\circ}\text{C}$			4	
		$T_A = -40^{\circ}\text{C}$			4	
		$T_A = 25^{\circ}\text{C}$		0.02	4	
		$T_A = 85^{\circ}\text{C}$			120	
		$T_A = 125^{\circ}\text{C}$			120	
	$V_{IN} = 0$ or 20, $V_{DD} = 20$	$T_A = -55^{\circ}\text{C}$			20	
		$T_A = -40^{\circ}\text{C}$			20	
		$T_A = 25^{\circ}\text{C}$		0.04	20	
		$T_A = 85^{\circ}\text{C}$			600	
		$T_A = 125^{\circ}\text{C}$			600	

## Electrical Characteristics: Static (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OLmin}$	Output low (sink) current	$V_O = 0.4$ , $V_{IN} = 0$ or $5$ , $V_{DD} = 5$	$T_A = -55^{\circ}\text{C}$	0.64			mA
			$T_A = -40^{\circ}\text{C}$	0.61			
			$T_A = 25^{\circ}\text{C}$	0.51	1		
			$T_A = 85^{\circ}\text{C}$	0.42			
			$T_A = 125^{\circ}\text{C}$	0.36			
	$V_O = 0.5$ , $V_{IN} = 0$ or $10$ , $V_{DD} = 10$		$T_A = -55^{\circ}\text{C}$	1.6			
			$T_A = -40^{\circ}\text{C}$	1.5			
			$T_A = 25^{\circ}\text{C}$	1.3	2.6		
			$T_A = 85^{\circ}\text{C}$	1.1			
			$T_A = 125^{\circ}\text{C}$	0.9			
	$V_O = 1.5$ , $V_{IN} = 0$ or $15$ , $V_{DD} = 15$		$T_A = -55^{\circ}\text{C}$	4.2			
			$T_A = -40^{\circ}\text{C}$	4			
			$T_A = 25^{\circ}\text{C}$	3.4	6.8		
			$T_A = 85^{\circ}\text{C}$	2.8			
			$T_A = 125^{\circ}\text{C}$	2.4			
$I_{OHmin}$	Output high (source) current	$V_O = 4.6$ , $V_{IN} = 0$ or $5$ , $V_{DD} = 5$	$T_A = -55^{\circ}\text{C}$	-0.64			mA
			$T_A = -40^{\circ}\text{C}$	-0.61			
			$T_A = 25^{\circ}\text{C}$	-0.51	-1		
			$T_A = 85^{\circ}\text{C}$	-0.42			
			$T_A = 125^{\circ}\text{C}$	-0.36			
	$V_O = 2.5$ , $V_{IN} = 0$ or $5$ , $V_{DD} = 5$		$T_A = -55^{\circ}\text{C}$	-2			
			$T_A = -40^{\circ}\text{C}$	-1.8			
			$T_A = 25^{\circ}\text{C}$	-1.6	-3.2		
			$T_A = 85^{\circ}\text{C}$	-1.3			
			$T_A = 125^{\circ}\text{C}$	-1.15			
	$V_O = 9.5$ , $V_{IN} = 0$ or $10$ , $V_{DD} = 10$		$T_A = -55^{\circ}\text{C}$	-1.6			
			$T_A = -40^{\circ}\text{C}$	-1.5			
			$T_A = 25^{\circ}\text{C}$	-1.3	-2.6		
			$T_A = 85^{\circ}\text{C}$	-1.1			
			$T_A = 125^{\circ}\text{C}$	-0.9			
	$V_O = 13.5$ , $V_{IN} = 0$ or $15$ , $V_{DD} = 15$		$T_A = -55^{\circ}\text{C}$	-4.2			
			$T_A = -40^{\circ}\text{C}$	-4			
			$T_A = 25^{\circ}\text{C}$	-3.4	-6.8		
			$T_A = 85^{\circ}\text{C}$	-2.8			
			$T_A = 125^{\circ}\text{C}$	-2.4			
$V_{OLmax}$	Low-level output voltage	$V_{IN} = 0$ or $5$ , $V_{DD} = 5$	$T_A = -55^{\circ}\text{C}$ , $-40^{\circ}\text{C}$ , $25^{\circ}\text{C}$ , $85^{\circ}\text{C}$ , and $125^{\circ}\text{C}$		0	0.05	V
		$V_{IN} = 0$ or $10$ , $V_{DD} = 10$	$T_A = -55^{\circ}\text{C}$ , $-40^{\circ}\text{C}$ , $25^{\circ}\text{C}$ , $85^{\circ}\text{C}$ , and $125^{\circ}\text{C}$		0	0.05	
		$V_{IN} = 0$ or $15$ , $V_{DD} = 15$	$T_A = -55^{\circ}\text{C}$ , $-40^{\circ}\text{C}$ , $25^{\circ}\text{C}$ , $85^{\circ}\text{C}$ , and $125^{\circ}\text{C}$		0	0.05	
$V_{OHmin}$	High-level output voltage	$V_{IN} = 0$ or $5$ , $V_{DD} = 5$	$T_A = -55^{\circ}\text{C}$ , $-40^{\circ}\text{C}$ , $25^{\circ}\text{C}$ , $85^{\circ}\text{C}$ , and $125^{\circ}\text{C}$	4.95	5		V
		$V_{IN} = 0$ or $10$ , $V_{DD} = 10$	$T_A = -55^{\circ}\text{C}$ , $-40^{\circ}\text{C}$ , $25^{\circ}\text{C}$ , $85^{\circ}\text{C}$ , and $125^{\circ}\text{C}$	9.95	10		
		$V_{IN} = 0$ or $15$ , $V_{DD} = 15$	$T_A = -55^{\circ}\text{C}$ , $-40^{\circ}\text{C}$ , $25^{\circ}\text{C}$ , $85^{\circ}\text{C}$ , and $125^{\circ}\text{C}$	14.95	15		

## Electrical Characteristics: Static (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ILmax}$ Input low voltage	$V_O = 0.5$ or $4.5$ , $V_{DD} = 5$	$T_A = -55^{\circ}C, -40^{\circ}C, 25^{\circ}C, 85^{\circ}C, \text{ and } 125^{\circ}C$			1.5
	$V_O = 1$ or $9$ , $V_{DD} = 10$	$T_A = -55^{\circ}C, -40^{\circ}C, 25^{\circ}C, 85^{\circ}C, \text{ and } 125^{\circ}C$			3
	$V_O = 1.5$ or $13.5$ , $V_{DD} = 15$	$T_A = -55^{\circ}C, -40^{\circ}C, 25^{\circ}C, 85^{\circ}C, \text{ and } 125^{\circ}C$			4
$V_{IHmin}$ Input high voltage	$V_O = 0.5$ or $4.5$ , $V_{DD} = 5$	$T_A = -55^{\circ}C, -40^{\circ}C, 25^{\circ}C, 85^{\circ}C, \text{ and } 125^{\circ}C$			3.5
	$V_O = 1$ or $9$ , $V_{DD} = 10$	$T_A = -55^{\circ}C, -40^{\circ}C, 25^{\circ}C, 85^{\circ}C, \text{ and } 125^{\circ}C$			7
	$V_O = 1.5$ or $13.5$ , $V_{DD} = 15$	$T_A = -55^{\circ}C, -40^{\circ}C, 25^{\circ}C, 85^{\circ}C, \text{ and } 125^{\circ}C$			11
$I_{INmax}$ Input current	$V_{IN} = 0$ or $18$ , $V_{DD} = 18$	$T_A = -55^{\circ}C$		$\pm 0.1$	$\mu A$
		$T_A = -40^{\circ}C$		$\pm 0.1$	
		$T_A = 25^{\circ}C$	$\pm 10^{-5}$	$\pm 0.1$	
		$T_A = 85^{\circ}C$		$\pm 1$	
		$T_A = 125^{\circ}C$		$\pm 1$	

## 6.6 Electrical Characteristics: Dynamic

at  $T_A = 25^{\circ}C$ , input  $t_r, t_f = 20$  ns,  $C_L = 50$  pF,  $R_L = 20$  k $\Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}, t_{PLH}$ Propagation delay time, clock to Q or $\bar{Q}$ outputs	$V_{DD} = 5$		150	300	ns
	$V_{DD} = 10$		65	130	
	$V_{DD} = 15$		45	90	
$t_{PLH}$ Set to Q or reset to $\bar{Q}$	$V_{DD} = 5$		150	300	ns
	$V_{DD} = 10$		65	130	
	$V_{DD} = 15$		45	90	
$t_{PHL}$ Set to $\bar{Q}$ or reset to Q	$V_{DD} = 5$		200	400	ns
	$V_{DD} = 10$		85	170	
	$V_{DD} = 15$		60	120	
$t_{THL}, t_{TLH}$ Transition time	$V_{DD} = 5$		100	200	ns
	$V_{DD} = 10$		50	100	
	$V_{DD} = 15$		40	80	
$f_{CL}$ Maximum clock input frequency <sup>(1)</sup>	$V_{DD} = 5$	3.5	7		MHz
	$V_{DD} = 10$	8	16		
	$V_{DD} = 15$	12	24		
$t_W$	Minimum clock pulse width	$V_{DD} = 5$	70	140	ns
		$V_{DD} = 10$	30	60	
		$V_{DD} = 15$	20	40	
	Minimum set or reset pulse width	$V_{DD} = 5$	90	180	ns
		$V_{DD} = 10$	40	80	
		$V_{DD} = 15$	25	50	
$t_S$ Minimum data setup time	$V_{DD} = 5$		20	40	ns
	$V_{DD} = 10$		10	20	
	$V_{DD} = 15$		7	15	
$t_H$ Minimum data hold time	$V_{DD} = 5, 10, 15$		2	5	ns

(1) Input  $t_r, t_f = 5$  ns

## Electrical Characteristics: Dynamic (continued)

at  $T_A = 25^\circ\text{C}$ , input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 20\text{ k}\Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rCL}, t_{fCL}$ Clock input rise or fall time	$V_{DD} = 5$			15	$\mu\text{s}$
	$V_{DD} = 10$			10	
	$V_{DD} = 15$			5	
$C_{IN}$ Input capacitance	Any input		5	7.5	pF

## 6.7 Typical Characteristics

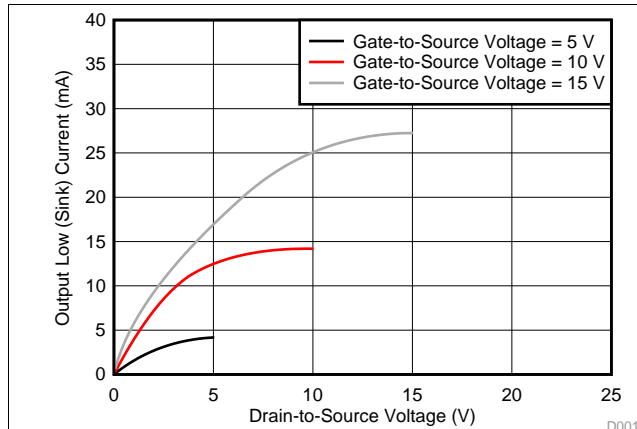


Figure 1. Typical Output Low (Sink) Current

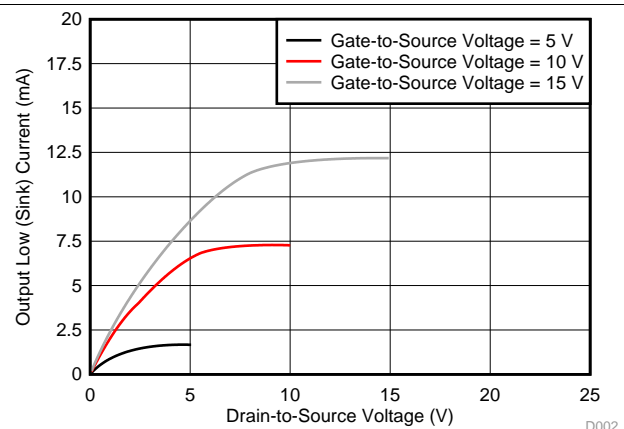


Figure 2. Minimum Output Low (Sink) Current

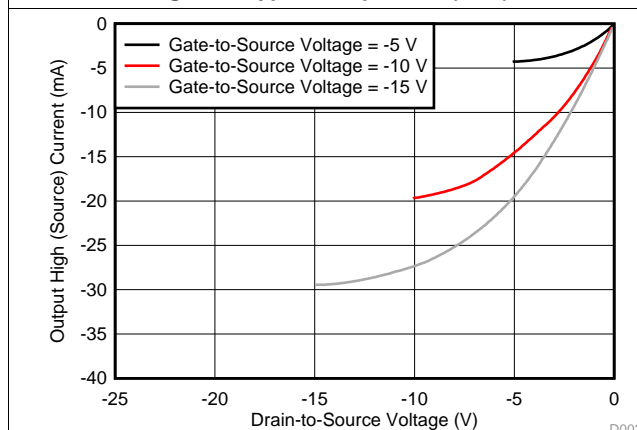


Figure 3. Typical Output High (Source) Current

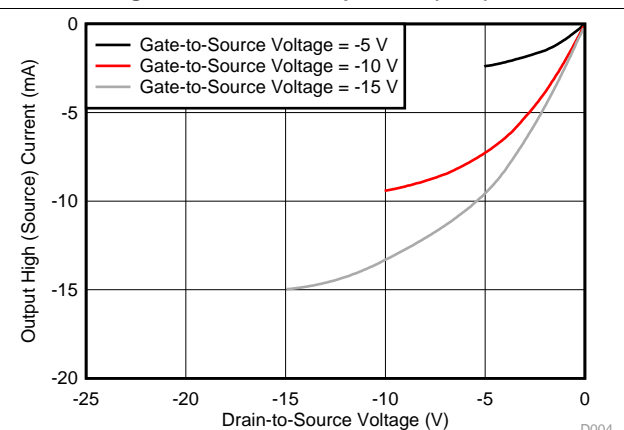
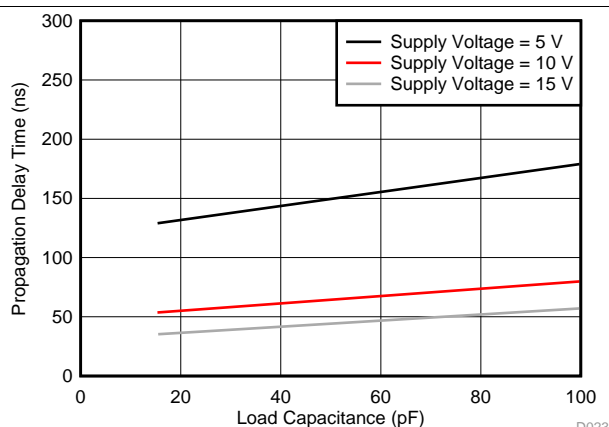


Figure 4. Minimum Output High (Source) Current

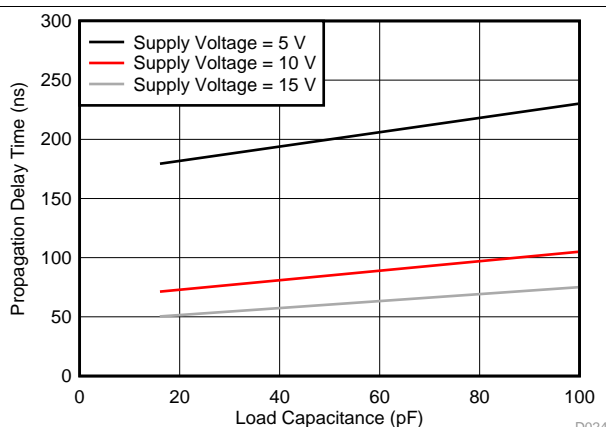


## Typical Characteristics (continued)



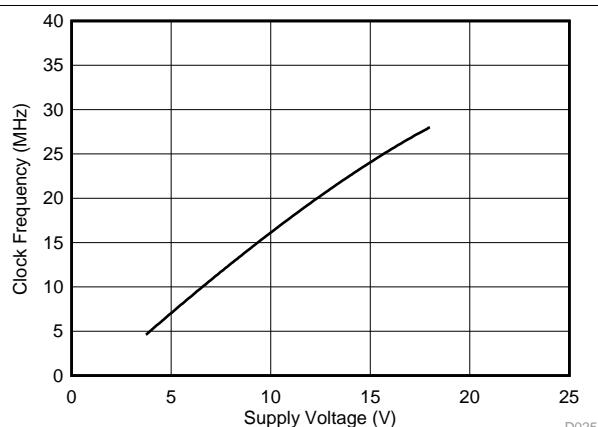
CLOCK or SET to Q, CLOCK or RESET to  $\bar{Q}$

**Figure 5. Typical Propagation Delay Time vs Load Capacitance**

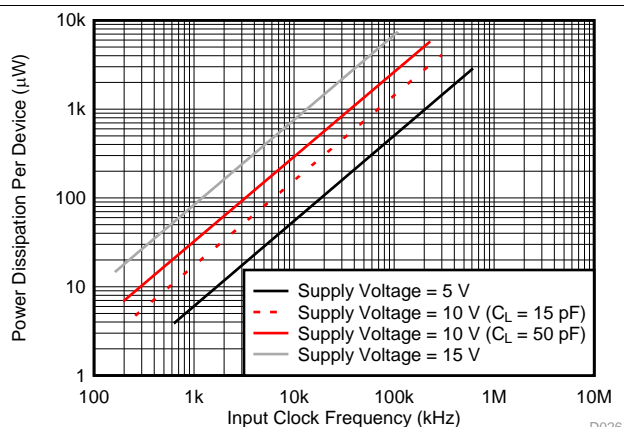


SET to  $\bar{Q}$  or RESET to Q

**Figure 6. Typical Propagation Delay Time vs Load Capacitance**



**Figure 7. Typical Maximum Clock Frequency vs Supply Voltage**



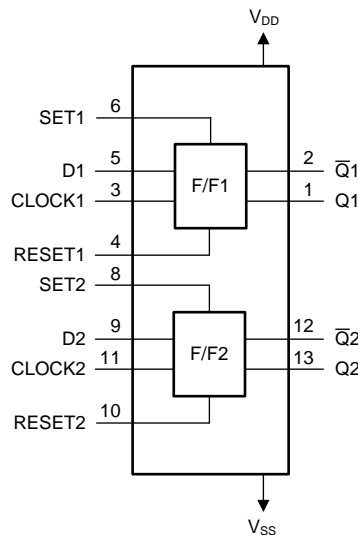
**Figure 8. Typical Power Dissipation vs Frequency**

## 7 Detailed Description

### 7.1 Overview

The CD4013B device consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and  $\bar{Q}$  outputs. These devices are ideal for data and memory hold functions, including shift register applications, or by connecting  $\bar{Q}$  output to the data input, this device is used for counter and toggle applications. The CD4013B is a positive-edge triggered device, meaning that the logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

CD4013B has standardized symmetrical output characteristics and a wide operating voltage range from 3 V to 18 V with quiescent current tested at 20 V. This has a medium operation speed  $-t_{PHL}$ ,  $t_{PLH} = 30$  ns (typical) at 10 V. The operating temperature is from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 7.4 Device Functional Modes

Table 1 lists the functional modes of the CD4013B.

**Table 1. Function Table**

INPUTS				OUTPUT (Q)	INVERTED OUTPUT ( $\bar{Q}$ )
CLOCK	SET	RESET	D		
$\uparrow$	0	0	0	0	1
$\uparrow$	0	0	1	1	0
$\downarrow$	0	0	X	$Q_0$	$\bar{Q}$
X	0	1	X	0	1
X	1	0	X	1	0
X	1	1	X	1	1

## 8 Application and Implementation

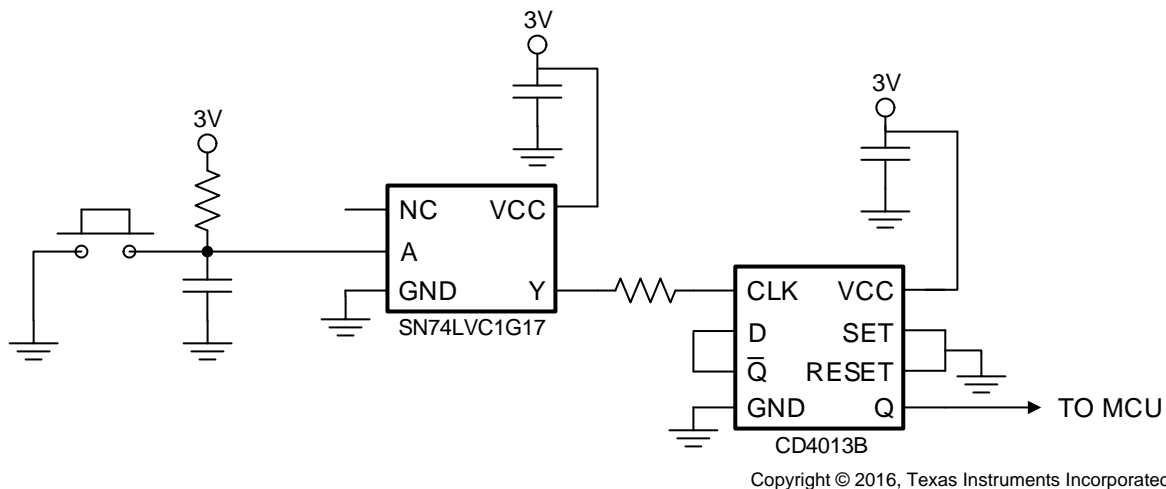
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

A high level at the SET or RESET inputs sets or resets the outputs, regardless of the levels of the other inputs. When SET and RESET are inactive (low), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. The resistor and capacitor at the RESET pin are optional. If they are not used, the RESET and SET pin must be connected directly to ground to be inactive.

### 8.2 Typical Application



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**Figure 9. Power Button Circuit**

#### 8.2.1 Design Requirements

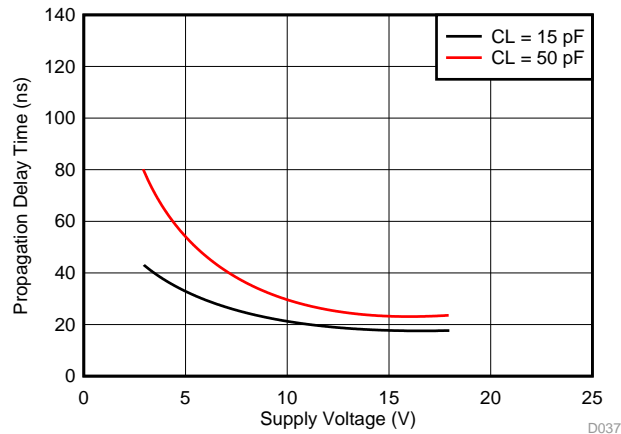
Input signals must be designed and implemented so that they do not exceed the voltage level of the power supply.

#### 8.2.2 Detailed Design Procedure

The recommended input conditions for this application example includes rise time and fall time specifications (see  $\Delta t/\Delta V$  in [Recommended Operating Conditions](#)) and specified high and low levels (see  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#)). Inputs are not overvoltage tolerant and must be below  $V_{CC}$  level because of the presence of input clamp diodes to  $V_{CC}$ . The recommended output condition for the CD4013B application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through  $V_{CC}$  or GND) for the device. These limits are located in [Absolute Maximum Ratings](#). Outputs must not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 8.2.3 Application Curve



**Figure 10. Typical Transition Time vs Load Capacitance**

## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#). Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor. If there are multiple  $V_{CC}$  pins, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 10 Layout

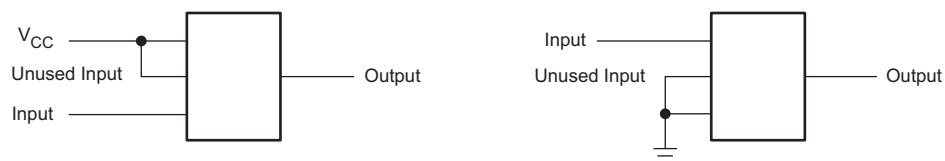
### 10.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, digital logic device functions or parts of these functions are unused (for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. This rule must be observed under all circumstances specified in the next paragraph.

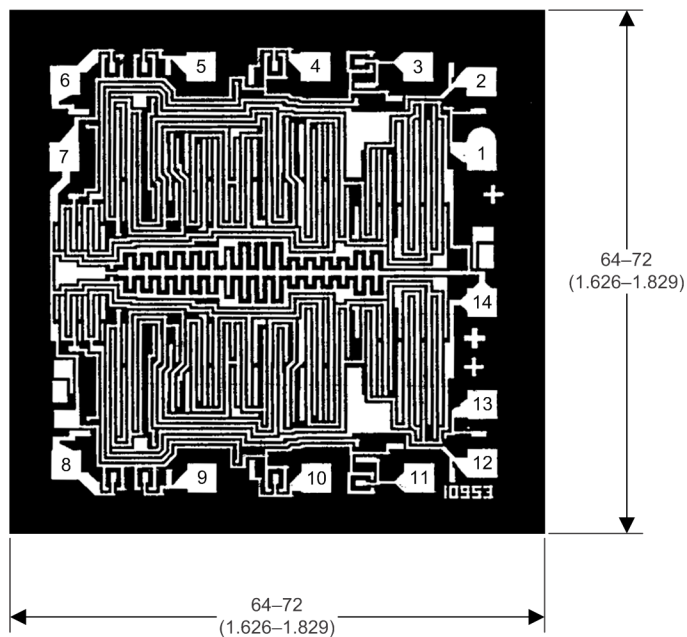
All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. See application note, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004), for more information on the effects of floating inputs. The logic level must apply to any particular unused input depending on the function of the device. Generally, they are tied to GND or  $V_{CC}$  (whichever is convenient).

### 10.2 Layout Example



**Figure 11. Layout Example for CD4013B**

## Layout Example (continued)



**Figure 12. Dimensions and Pad Layout for CD4013B**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4013BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4013BE	<a href="#">Samples</a>
CD4013BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4013BE	<a href="#">Samples</a>
CD4013BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4013BF	<a href="#">Samples</a>
CD4013BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4013BF3A	<a href="#">Samples</a>
CD4013BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013BM	<a href="#">Samples</a>
CD4013BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013B	<a href="#">Samples</a>
CD4013BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4013B	<a href="#">Samples</a>
CD4013BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM013B	<a href="#">Samples</a>
CD4013BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM013B	<a href="#">Samples</a>
CD4013BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM013B	<a href="#">Samples</a>
CD4013BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM013B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/05151BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05151BCA	<a href="#">Samples</a>
M38510/05151BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05151BCA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD4013B, CD4013B-MIL :**

- Catalog: [CD4013B](#)
- Military: [CD4013B-MIL](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4013BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4013BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4013BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4013BNSR	SO	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4013BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

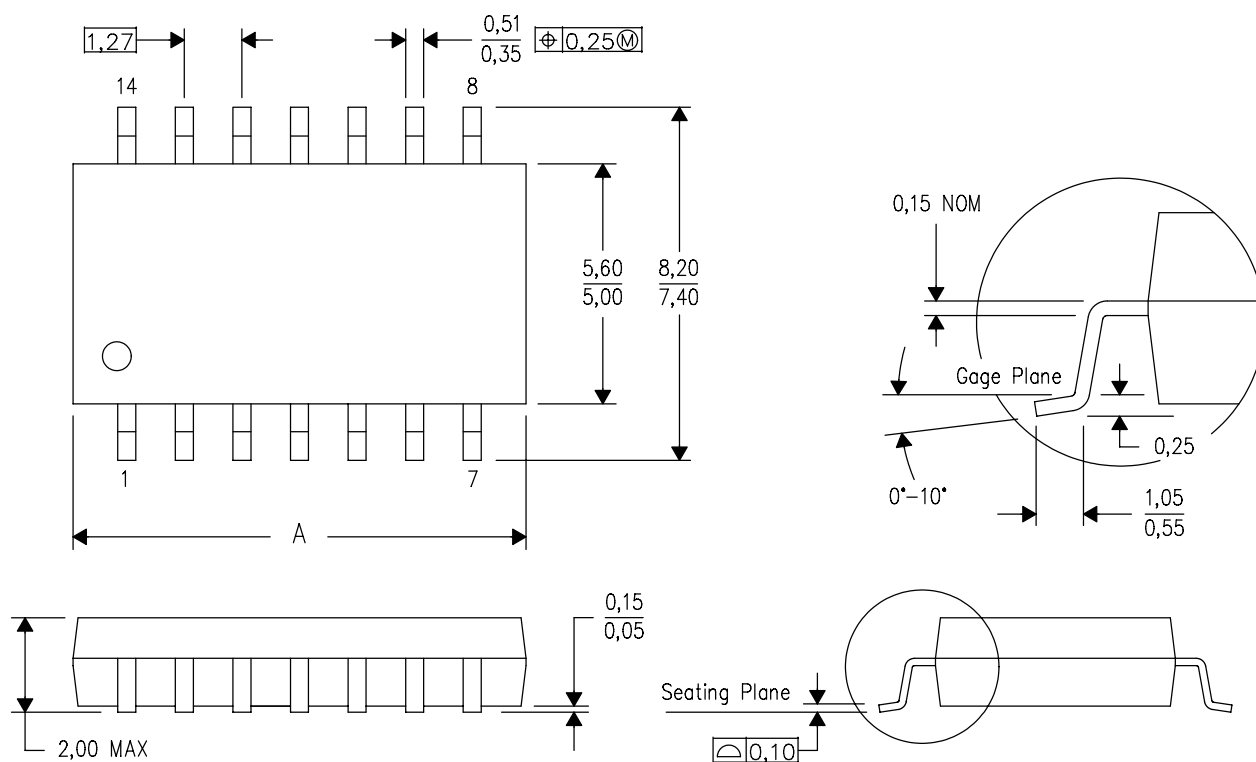
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4013BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4013BM96G4	SOIC	D	14	2500	367.0	367.0	38.0
CD4013BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4013BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4013BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

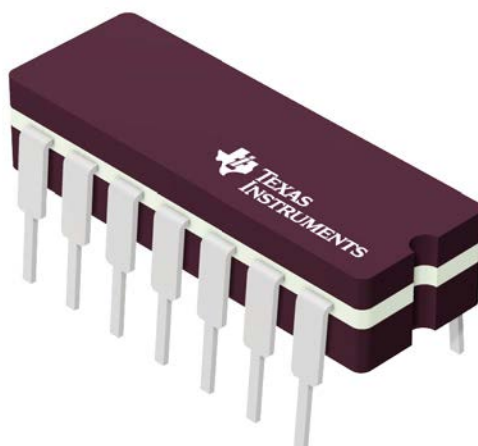
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**J 14**

## GENERIC PACKAGE VIEW

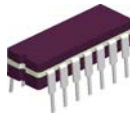
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

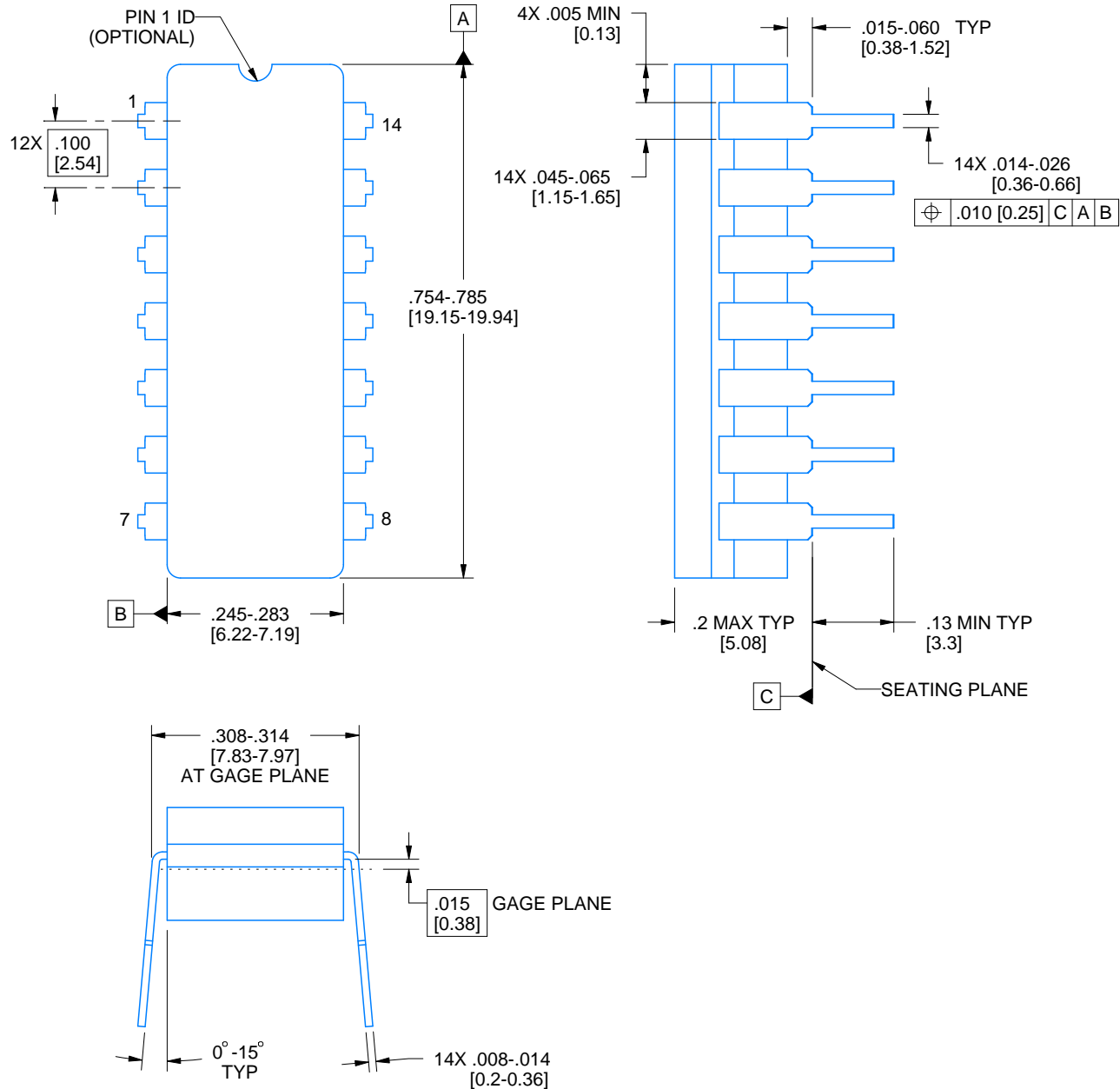


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

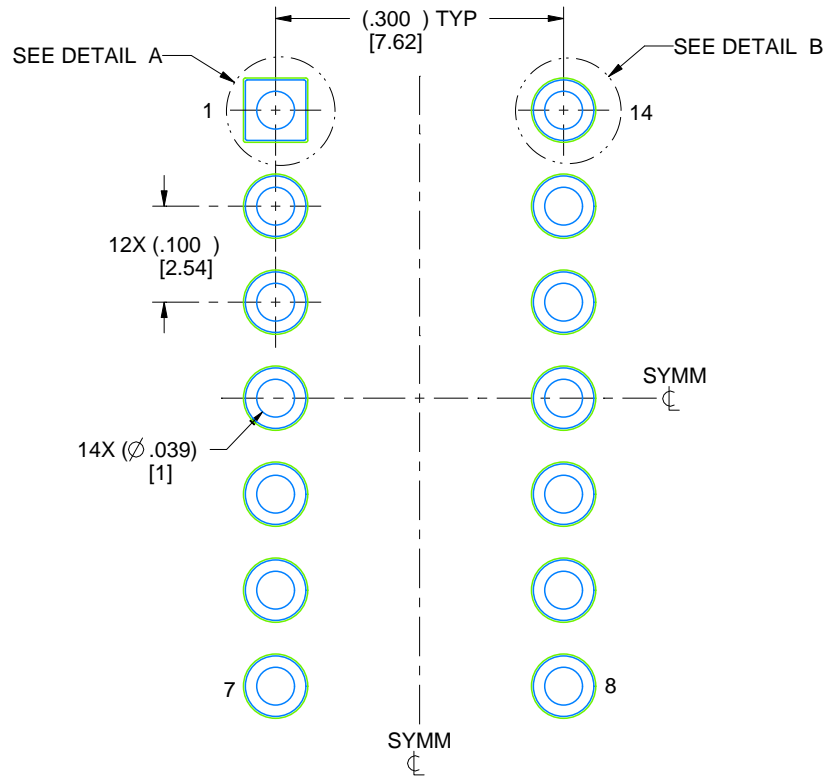
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

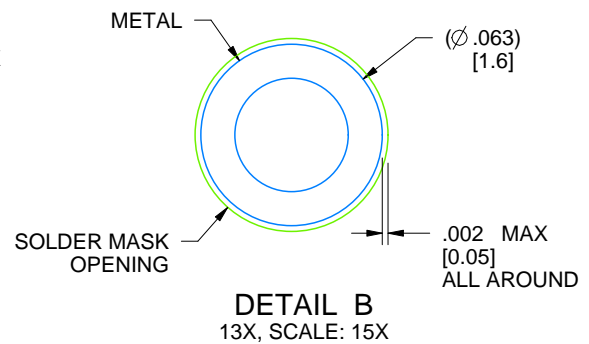
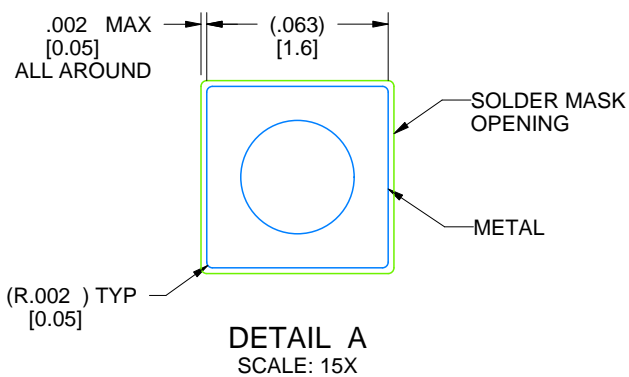
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



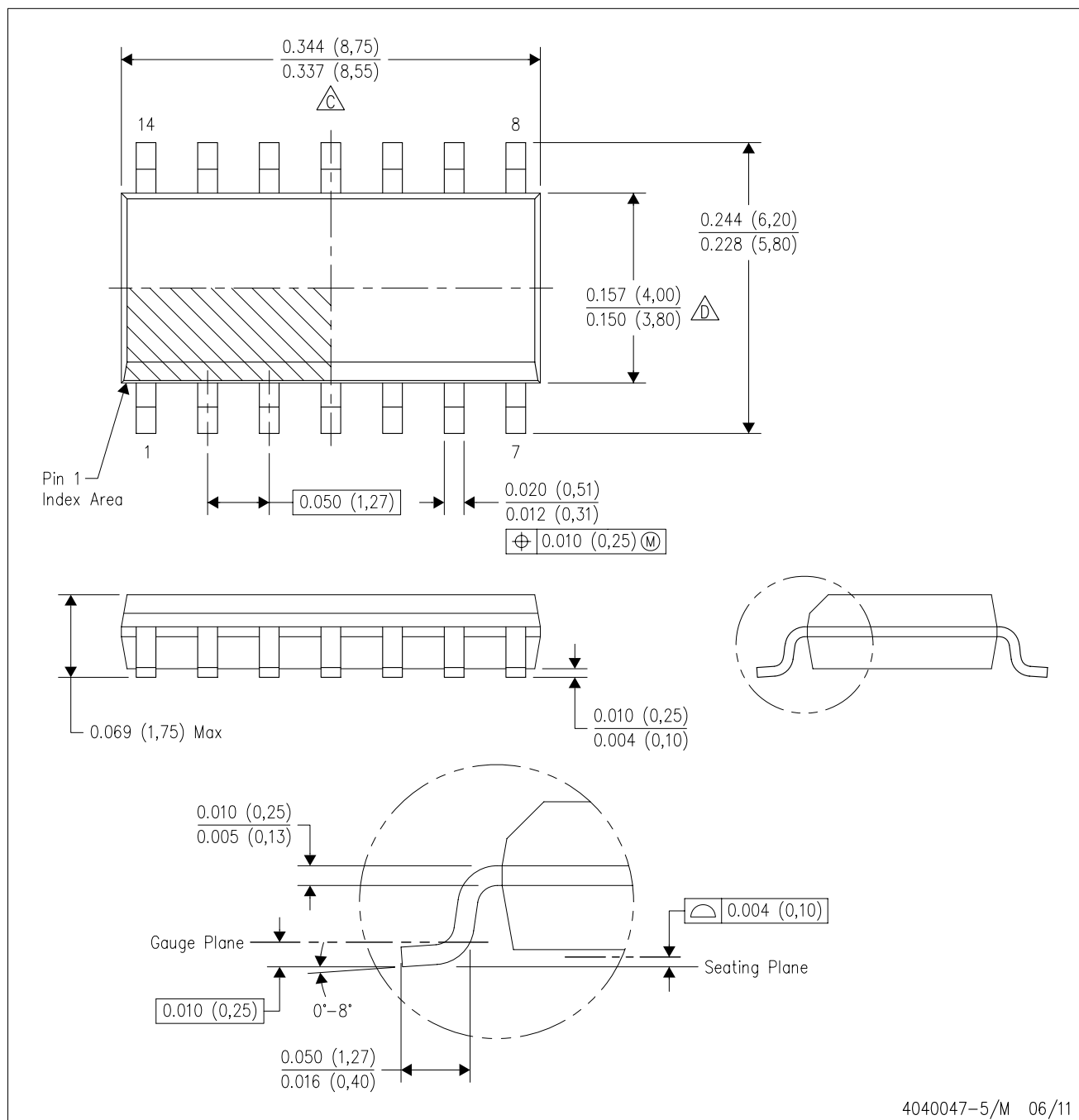
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

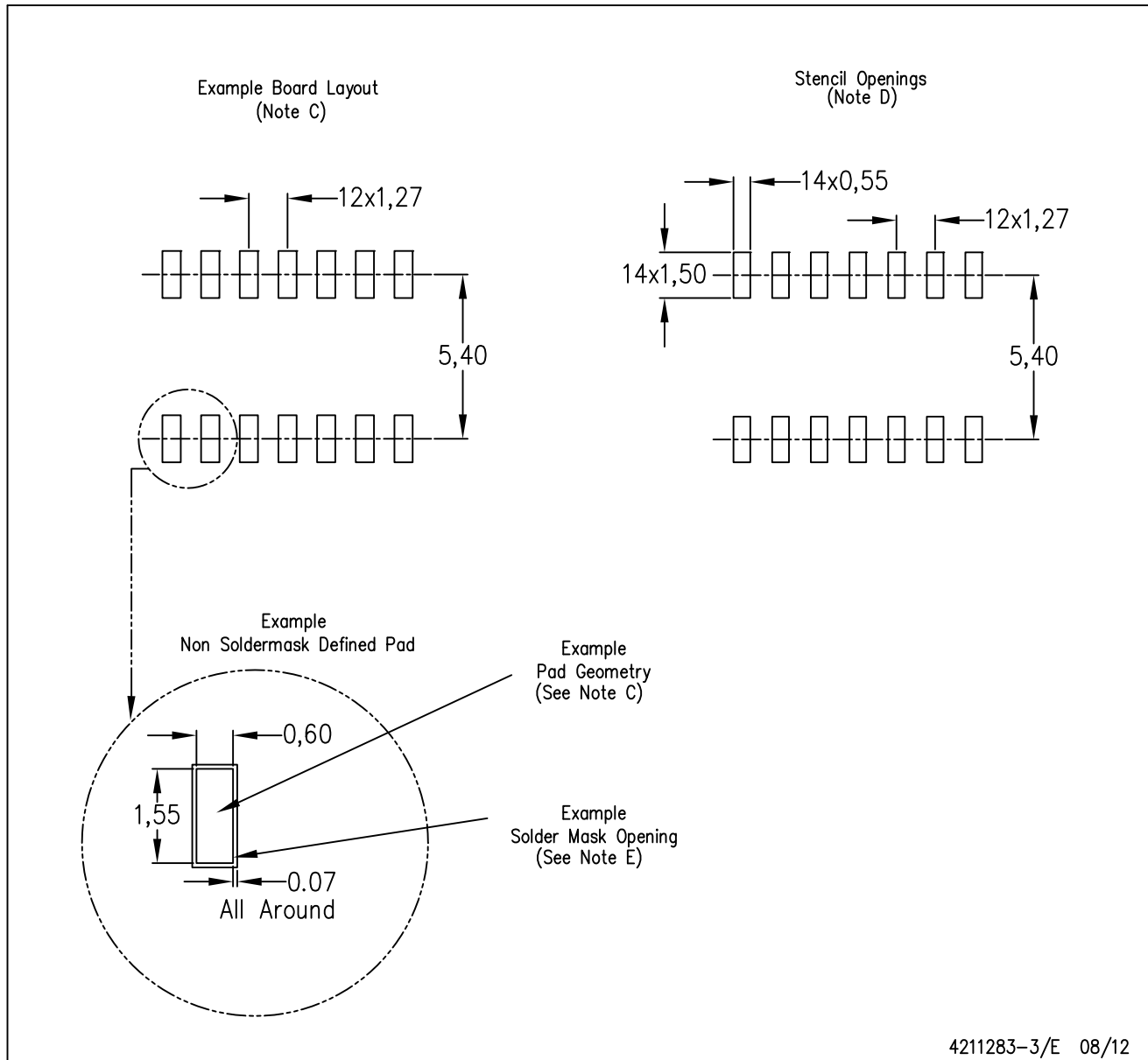
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

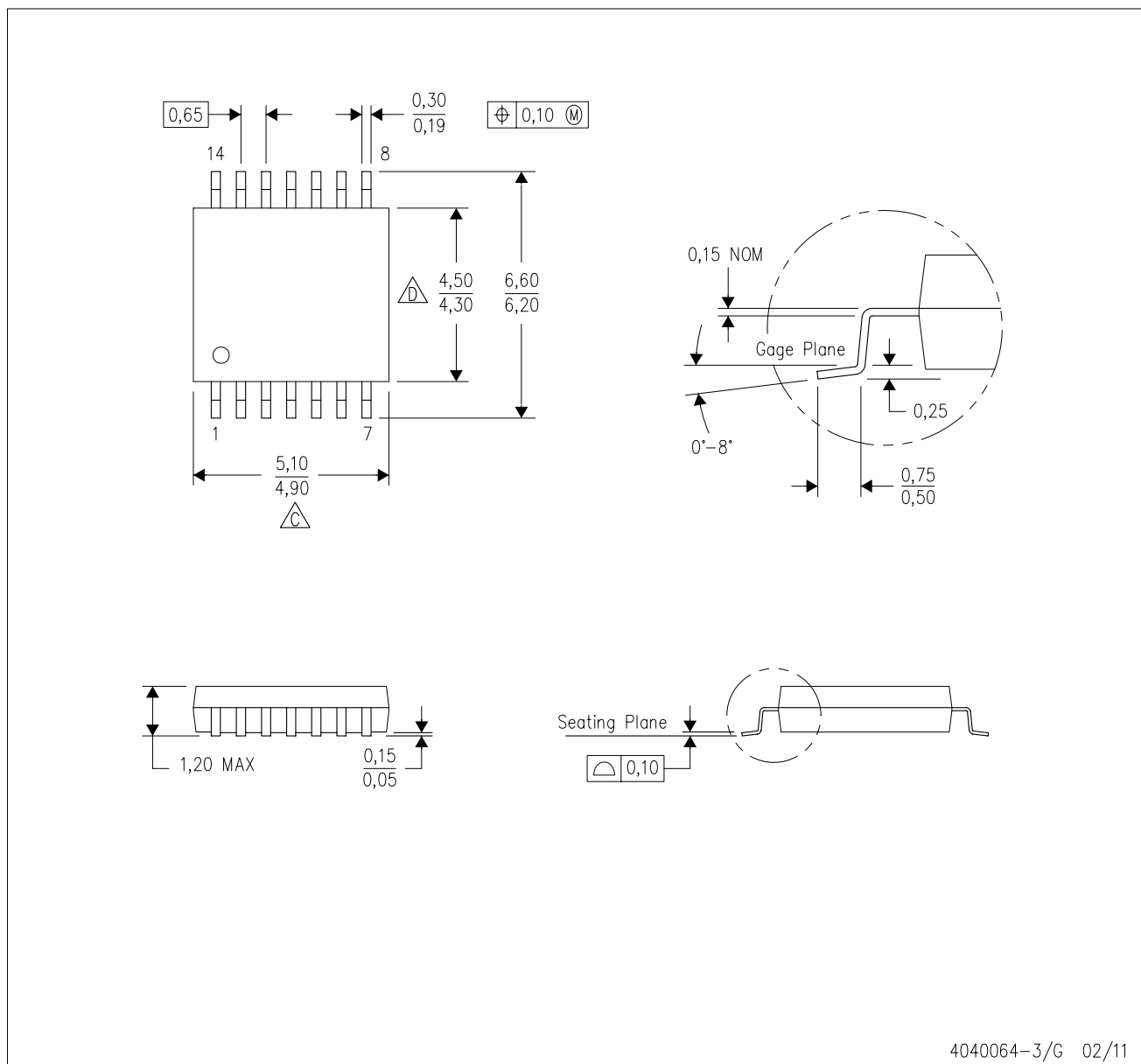
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

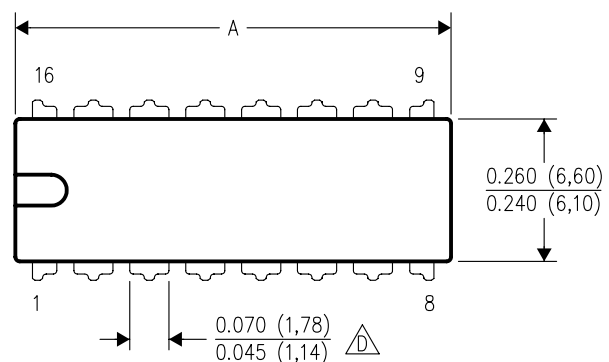


4040064-3/G 02/11

N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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