# Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 120 Powerful Instructions Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
- Data and Non-volatile Program and Data Memories
  - 2/4K Bytes of In-System Self Programmable Flash
     Endurance 10,000 Write/Erase Cycles
  - 128/256 Bytes In-System Programmable EEPROM
    - Endurance: 100,000 Write/Erase Cycles
  - 128/256 Bytes Internal SRAM
  - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Modes
  - Four PWM Channels
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with On-chip Oscillator
  - USI Universal Serial Interface
  - Full Duplex USART
- Special Microcontroller Features
  - debugWIRE On-chip Debugging
  - In-System Programmable via SPI Port
  - External and Internal Interrupt Sources
  - Low-power Idle, Power-down, and Standby Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit
  - Internal Calibrated Oscillator
- I/O and Packages
  - 18 Programmable I/O Lines
  - 20-pin PDIP, 20-pin SOIC, 20-pad MLF/VQFN
- Operating Voltage
  - 1.8 5.5V
- Speed Grades
  - 0 4 MHz @ 1.8 5.5V
  - 0 10 MHz @ 2.7 5.5V
  - 0 20 MHz @ 4.5 5.5V
- Industrial Temperature Range: -40°C to +85°C
- Low Power Consumption
  - Active Mode
    - 190 µA at 1.8V and 1MHz
  - Idle Mode
    - + 24  $\mu A$  at 1.8V and 1MHz
  - Power-down Mode
    - + 0.1  $\mu A$  at 1.8V and +25°C



8-bit **AVR**<sup>®</sup> Microcontroller with 2/4K Bytes In-System Programmable Flash

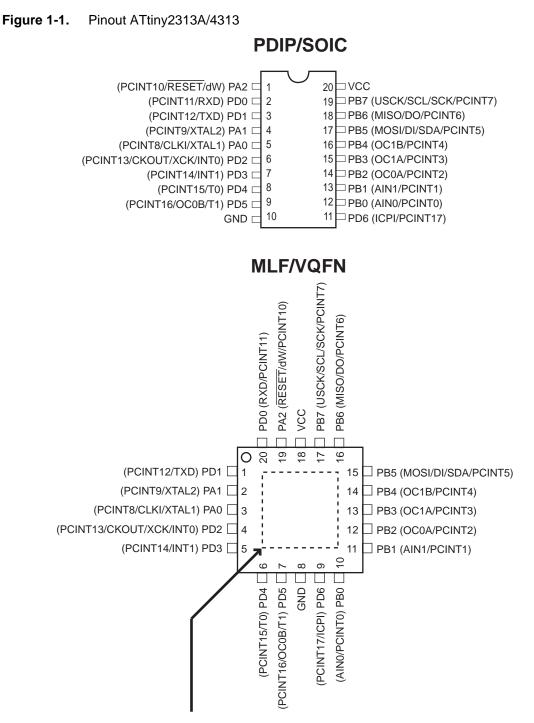
ATtiny2313A ATtiny4313

Summary





# 1. Pin Configurations



NOTE: Bottom pad should be soldered to ground.

### 1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

### 1.1.2 GND

Ground.

### 1.1.3 Port A (PA2..PA0)

Port A is a 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability, except PA2 which has the RESET capability. To use pin PA2 as I/O pin, instead of RESET pin, program ("0") RSTDISBL fuse. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny2313A/4313 as listed on page 61.

### 1.1.4 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny2313A/4313 as listed on page 62.

### 1.1.5 Port D (PD6..PD0)

Port D is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATtiny2313A/4313 as listed on page 66.

### 1.1.6 **RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided that the reset pin has not been disabled. The minimum pulse length is given in Table 22-3 on page 201. Shorter pulses are not guaranteed to generate a reset. The Reset Input is an alternate function for PA2 and dW.

The reset pin can also be used as a (weak) I/O pin.

### 1.1.7 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit. XTAL1 is an alternate function for PA0.





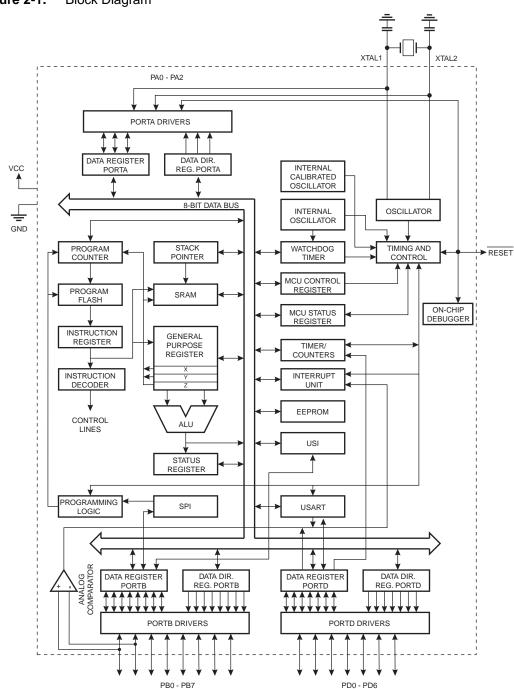
### 1.1.8 XTAL2

Output from the inverting Oscillator amplifier. XTAL2 is an alternate function for PA1.

## 2. Overview

The ATtiny2313A/4313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny2313A/4313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### 2.1 Block Diagram









The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny2313A/4313 provides the following features: 2/4K bytes of In-System Programmable Flash, 128/256 bytes EEPROM, 128/256 bytes SRAM, 18 general purpose I/O lines, 32 general purpose working registers, a single-wire Interface for On-chip Debugging, two flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, or by a conventional non-volatile memory programmer. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny2313A/4313 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny2313A/4313 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

### 2.2 Comparison Between ATtiny2313A and ATtiny4313

The ATtiny2313A and ATtiny4313 differ only in memory sizes. Table 2-1 summarizes the different memory sizes for the two devices.

Device	Flash	EEPROM	RAM
ATtiny2313A	2K Bytes	128 Bytes	128 Bytes
ATtiny4313	4K Bytes	256 Bytes	256 Bytes

Table 2-1. Memory Size Summary

# 3. About

### 3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at http://www.atmel.com/avr.

### 3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically, this means "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR". Note that not all AVR devices include an extended I/O map.

### 3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.



BodF (DSP)         SPEC0         I         T         H         S         V         N         Z         C         B           DATE (DSP)         SPL	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
BacD Duch)         SPI         SPI         SPI         SPI         SPI         SPI         SPI         T2           6x82 (bdS)         CMRKE         NTT         NTT         NTT         PCE0         PCE1         -         -         50           6x83 (bdS)         CMR         NTT         NTT         PCE0         PCE1         -         -         50           6x81 (bdS)         ORTR         NTT         NTT<	0x3F (0x5F)	SREG	I	Т	Н	S	V	N	Z	С	9
965C (95C)         OCR08         ITTERCOUNTER_Courset_Courset Registril 8         68           0608 (056)         GMRK         NTTFI         NTTF         PCIG         PCIZ         <	0x3E (0x5E)	Reserved	-	-	-	-	-	-	-	-	
0x88.80x80         0.4Mx84         NT1         NT0         PCI2         PCI3         Description         Sol           0x84.00x80         PIPR         NT1         NT0         PCI2         PCI3         Description         State           0x88.00x90         TIMEK         TOSI         0x0EixA         PORIT         COURSA         PR0.115           0x76.00x97         SPMCSR         -         ASI         COURSA         PR0.115         PORIT			SP7	SP6					SP1	SP0	
Bock Joucki J.         OFFE         INTEL         INTEL         OCIE 18         OCIE 18 <t< td=""><td>· · · · · · · · · · · · · · · · · · ·</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>	· · · · · · · · · · · · · · · · · · ·										
0.69 (de)g)         TMBK         TOEI         OOEKa         OOEKa         TOEI         OOEKa         B6, 115           0.69 (de)g)         BFR         T         OOEKA         B6, 115         OCFA         B7040         OCEAA         B6, 115           0.69 (de)g)         OOEKA         T         BSU         CTPS         RTLS         PQRT         PQRT         DPMT         175           0.69 (de)g)         MCURA         -         -         NUMM         BORT         PCMT         DEVT         46           0.69 (de)g)         MCURA         -         -         -         WAMAZ         CS02         CS01         650         64           0.69 (de)g)         MCURA         POCA         FOCA         FOCA         FOCA         FOCA         S03         CS02         CA11         CA10         53           0.69 (de)g)         TCCBAL         COMA1         COMA0         COMA0         COMA0         CA11         CA11         CA10         53         TTRE         CS12         CS12         CS12         CS12         TTRE         TTRE         TTRE         CA11         CA11         CA11         TTRE         TTRE         TTRE         CA11         CA10         TTRE         <								-	-		
668.6668         TTRE         TOVI         OCF18         CF1         DCF08         TTREN         OCF04         AB.115           0x87.0x671         SPK0578         -         -         RS0         SC11         SC10						PCIF2					
0.07         SPACER         -         RSG         CTPM         PFLB         PGWRT         PGES         SPAIN         175           0.051         0.063         MCURK         PUD         SM1         SE         SM0         ISC11         ISC10         ISC01         ISC02         S6, 56, 56           0.041         0.056         MCURK         PUD         SM1         SE         SM0         ISC11         ISC10         ISC02         S6, 56         SM1         SE         SM0         ISC11         ISC10         ISC02         S6, 56         SM1         SE         SM0         ISC11         ISC10         ISC02         C501         C500         B4         ISC02         SM1         SM1         SM1         SM2         SM1	· · · · · ·										
0.05.00/03         OCR0A         Trans/Counter-Counge Register A         95           0.053.00/03         MCUCR         PUD         SM1         SEC11         ISC01         ISC01         SEC01         CAL1         CAL2         CAL1         CAL2         CAL1	· · · · · ·					СТРВ					
0x56 (bcb)         MCLOR         PUD         SM1         SF         840         (SC11         (SC01         (SC01         SC00         SK0.68           0x54 (bc64)         MCLOR         FOC08										-	
0-033 (MS3)         TOCR8         FOCA6         FOCA6         CALS	0x35 (0x55)	MCUCR	PUD	SM1					ISC01	ISC00	36, 50, 68
0.62 (0x5)         TONTO         THERE/Current() (Feb.)         0.63         0.641         0.641         0.642         0.642         0.641         0.640         0.71         0.640         0.71         0.640         0.71         0.640         0.71         0.640         0.71 <td>0x34 (0x54)</td> <td>MCUSR</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>WDRF</td> <td>BORF</td> <td>EXTRF</td> <td>PORF</td> <td>44</td>	0x34 (0x54)	MCUSR	-	-	-	-	WDRF	BORF	EXTRF	PORF	44
0-31 (MoS1)         OSECUL         Image: CAL6         CAL7         CAL3	0x33 (0x53)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	84
0.000         TCCENA         COMMA1         COMMA0         COMM10         COMM11         COMM10         COMM11         COMM11<	· · · · · ·									1	
0x2F         COMPLE         ComPLE </td <td></td> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>			-								
0x2E (0x4E)         TOCR18         IONC1         ICES1         IVeXH12         CS12         CS11         CS10         112           0x2E (0x4D)         TORT11.         Timer/Contret - Contrer Register MpB trie         114           0x2B (0x4D)         OCR14H.         Timer/Contret - Compare Register ALm But etc.         114           0x2B (0x4D)         OCR14H.         Timer/Contret - Compare Register But But etc.         114           0x2B (0x4D)         OCR14H.         Timer/Contret - Compare Register But But etc.         114           0x2B (0x4D)         OCR15H.         Timer/Contret - Compare Register But But etc.         114           0x2B (0x4D)         OCR15H.         Timer/Contret - Compare Register But But etc.         114           0x2B (0x4D)         CLKPCE         -         -         -         -           0x4D (0x4D)         CLKPCE         -         -         -         -         -           0x4D (0x4D)         CCKPCE         -         -         -         -         -         -         114           0x2D (0x4D)         CCKPCE         -         -         -         -         -         113           0x2D (0x4D)         VDTCR         PCKNT         PCKNT         PCKNT         PCKNT	· · · · · ·							-			
9x20 (0x40)         TONTH         Thermocontert - Counter Register Migh Byte         114           0x20 (0x40)         CRN14H         ThermoCountert - Counter Register A High Byte         114           0x28 (0x40)         OCR14AL         ThermoCountert - Counter Register A High Byte         114           0x28 (0x40)         OCR14AL         ThermoCountert - Counter Register A High Byte         114           0x28 (0x40)         OCR18H         ThermoCountert - Counter Register B High Byte         114           0x28 (0x40)         OCR18H         ThermoCountert - Counter Register B High Byte         114           0x28 (0x40)         OCR18H         ThermoCountert - Input Capture Register High Byte         114           0x28 (0x40)         ICLNPS         CLNPS1         CLNPS0         31           0x28 (0x40)         ICR1H         ThermoCountert - Input Capture Register High Byte         114           0x28 (0x40)         ICR1H         ThermoCountert - Input Capture Register High Byte         114           0x28 (0x40)         ICR1H         ThermoCountert - Input Capture Register High Byte         114           0x28 (0x40)         ICR1H         ThermoCountert - Input Capture Register High Byte         114           0x28 (0x40)         ICR1H         PCR1HI         PCR1HI         PCR1HI           0x28 (0x4	· · · · · · · · · · · · · · · · · · ·				COM1B1			-			
Becc (setC)         TONTL         TimerCounter 1 - Counter Register Low Byte         114           0x26 (setA)         COR1AL         TimerCounter 1 - Compare Register A Low Byte         114           0x28 (setA)         COR1AL         TimerCounter 1 - Compare Register B High Byte         114           0x28 (setA)         COR1AL         TimerCounter 1 - Compare Register B High Byte         114           0x28 (setA)         COR1AL         TimerCounter 1 - Compare Register B High Byte         114           0x28 (setA)         CLKPES         -         -         -           0x28 (setA)         CLKPES         -         -         -         -           0x28 (setA)         CLKPES         -         -         -         -         -           0x28 (setA)         CLKPES         CLKPES         CLKPES         0.114         -         -           0x28 (setA)         CLKPE         -			ICNC1	ICES1	 Tim				CS11	6510	
0a28 (0x4b)         CCR1AH         TimerCounter1 - Compare Register A Log Bys         114           0x28 (0x4b)         CCR1AH         TimerCounter1 - Compare Register B Light Byt         114           0x28 (0x4b)         OCR1BH         TimerCounter1 - Compare Register B Light Byt         114           0x28 (0x4b)         OCR1BL         TimerCounter1 - Compare Register B Light Byt         114           0x28 (0x4b)         CLKPCE         -         -         -         CLKPS3         CLKPS3         CLKPS1         CLKPS3         CLKPS3         CLKPS1         TimerCounter1 - Input Capture Register Light Byt         114           0x28 (0x4b)         CRTCR         - <td></td>											
0±28 (0x4)         OCR18L         Timer/Counter1 - Compare Register ALow Syst         114           0±28 (0x48)         OCR18L         Timer/Counter1 - Compare Register B Ligh Byte         114           0±28 (0x48)         OCR18L         Timer/Counter1 - Compare Register B Ligh Byte         114           0±28 (0x48)         OLKPSL         CLKPSL         CLKPSL         0           0±28 (0x48)         OLKPSL         CLKPSL         CLKPSL         0         114           0±28 (0x44)         ICR1L         Timer/Counter1 - Input Capture Register Ligh Byte         114         114           0±28 (0x44)         ICR1L         Timer/Counter1 - Input Capture Register Low Byte         114         114           0±28 (0x44)         ICR1L         Timer/Counter1 - Input Capture Register Low Byte         114         114           0±28 (0x44)         ICRCR         FOC1A         FOC1B         F											
0x28 (0x48)         OCK181H         Timer/Counter1 - Compare Register B Hugh Byte         114           0x28 (0x48)         OCK18L         Timer/Counter1 - Compare Register B Aux Byte         114           0x28 (0x48)         CLKPS         CLKPS0         21           0x28 (0x44)         CLKP         -         1114           0x28 (0x42)         GTCCR         -         -         -         -         -         -         -         1114           0x28 (0x42)         GTCCR         FOC1A         FOC1B         -         -         -         -         1114         0x28 (0x42)         0x18 (0x44)         0x1							· · · · ·	* *			
0x28 (0x46)         CLKPR         CLKPR         CLKPR         CLKPR         CLKPR         CLKPR         CLKPR         CLKPS											
0x26 (0x46)         CLKPR         CLKPR2         CLKPR3         CLK	0x28 (0x48)	OCR1BL			Timer	/Counter1 - Com	pare Register B L	ow Byte			114
IDSC [0x46]         IDR1H         Timer/Constant - Impul Capture Register Law Byte         114           0x24 (0x44)         ICR1L         Timer/Constant - Impul Capture Register Law Byte         114           0x23 (0x43)         GTCCR         -         -         -         -         PSR10         113           0x23 (0x42)         TCCK1C         FOC1A         FOC1B         -	0x27 (0x47)	Reserved	_	_	_	-	_	-	-	-	
0x24 (bx4)         ICRL         Timer/Content - Impu Capture Register tore Byte         114           0x23 (bx42)         GTCCR1C         FOC1A         FOC1B         -         -         -         P         -         -         P         -         -         P         P         -         -         P         P         113           0x21 (bx41)         WDICSR         WDIF         WDE         WDP3         WDCE         WDE         WDP1         WDP0         44           0x20 (bx40)         PCMSTA         PCINT3	0x26 (0x46)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	31
Inc.23 (or.43)         GTCCR         -         -         -         -         -         -         PSR10         118           0x22 (or.42)         TCCR1C         FOC1A         FOC1B         -         -         -         -         -         113           0x22 (or.41)         WDTCSR         WDIF         WDIF         WDP         WDP         WDP         44           0x21 (or.41)         WDTCSR         WDIF         PCINT5         PCINT4         PCINT1         PCINT0         53           0x11 (or.35)         Reserved         -         DDA1         DDA3         068         010 (or.30)         EERE         EERE         EERE         23         0414 (or.34)         DDR4         -         -         -         DDA2         DDA1         DDA3         68         014 (or.34)         00140         D03         0163	0x25 (0x45)	ICR1H			Timer/	Counter1 - Input (	Capture Register	High Byte			114
Doc2 (ox42)         TCCR1C         FOC1A         FOC1B         -         -         -         -         -         -         -         -         -         -         113           0x21 (0x41)         WDTCSR         WDIF         WDIE         WDE         WDE         WDE         WDP1         WDP0         44           0x20 (0x40)         PCMRS0         PCINT3         PCINT	· · · · · ·				Timer/	Counter1 - Input (	Capture Register	Low Byte			
Doz1 (0x41)         WDIFSR         WDIF         WDIE         WDP3         WDCE         WDE         WDP2         WDP1         WDP0         44           0x20 (0x40)         PCINT7         PCINT6         PCINT6         PCINT3         PCINT2         PCINT1         PCINT3         PCINT1         PCINT3         PCINT3 <td< td=""><td>· · · · · ·</td><td></td><td></td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td></td><td></td></td<>	· · · · · ·				-	-	-	-	-		
0x20 (0x40)         PCMSK0         PCINT7         PCINT6         PCINT5         PCINT3         PCINT2         PCINT1         PCINT0         53           0x1F (0x5E)         EERR         -         DOR1A         PORTA         -         -         -         -         DOR1A         PORTA         -         -         -         DOR1A         PORTA         -         -         -         DOR1A         PORTA         -         -         DOR1A         PORTA         PORTA         -         -         DOR1A         DOR1A         DOR1A         DOR1A         DOR1A         DOR1A         DOR1A         DOR1A         D					-				-		
OxtF (0x3F)         Reserved         -         DDA2         DDA1         DDA0         68           0x16 (0x36)         PORTB         PORTB<	· · · · · ·										
Dx1E (0x3E)         EEAR         -         EEPROM Address Register         23           0x1D (0x30)         EEDR         -         EEPROM Data Register         23           0x1D (0x30)         EEDR         -         -         EPROM Data Register         23           0x1B (0x38)         PORTA         -         -         -         PORTA2         PORTA1         PORTA0         68           0x1A (0x33)         DDRA         -         -         -         -         DDA2         DDA11         DDA0         68           0x13 (0x39)         PINA         -         -         -         -         PORTB2         PORTB1         PORTB0         69           0x16 (0x38)         PINB         DDB7         DDB6         DDB5         DDB4         DDB3         PINB2         PINB1         PINB0         69           0x16 (0x38)         PINB         PINB7         PINB6         PINB5         PINB4         PINB3         PINB2         PINB1         PINB0         69           0x13 (0x33)         GPIOR1         General Purpose I/O Register 1         24         24         24         24         24         24         24         24         24         24         24         24 <td>· · · · · ·</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>PCIN13</td> <td></td> <td></td> <td></td> <td>53</td>	· · · · · ·						PCIN13				53
Ox1D (0x3D)         EEDR         EEPROM         EEPROM         Data Register         23           0x1C (0x3C)         EECR         -         -         EEPNM         EENIE         EENIE         EEPE         EERE         23           0x116 (0x3B)         PORTA         -         -         -         -         PORTA2         PORTA1         PORTA0         68           0x14 (0x3A)         DDRA         -         -         -         -         PORTA2         PORTA1         PORTA0         68           0x14 (0x3A)         DDRA         -         -         -         -         PORTB2         PORTB1         PORTB0         69           0x16 (0x3B)         PORTB         PORTB7         PORTB6         PORTB5         PORTB3         PORTB1         PORTB0         69           0x15 (0x35)         GPIOR2					_		PROM Address R		_	_	23
Ox1C (0x3C)         EECR         -         -         EEPM1         EEPM0         EERIE         EEMPE         EERE         23           0x1B (0x3B)         PORTA         -         -         -         -         PORTA2         PORTA1         PORTA0         68           0x14 (0x3A)         DDRA         -         -         -         -         DDA2         DDA1         DDA0         68           0x13 (0x39)         PINA         -         -         -         -         PINA2         PINA1         PINA0         69           0x16 (0x36)         PORTB         PORTB7         PORTB6         PORTB5         PORTB4         PORTB3         PORTB2         PORTB0         69           0x16 (0x36)         PINB         PINB7         PINB6         PINB5         PINB4         PINB3         PINB2         PINB1         PINB0         69           0x13 (0x33)         GPIOR0         -         -         PORTD6         PORTD5         PORTD4         PORTD2         PORTD1         24         24           0x13 (0x33)         GPIOR0         -         PORT06         PORTD5         PORTD4         PORT02         PORTD1         PORT00         69           0x11 (0x33)				I				egiotei			
0x18 (0x38)         PORTA         -         -         -         -         PORTA2         PORTA1         PORTA0         68           0x14 (0x3A)         DDRA         -         -         -         -         DDA2         DDA1         DDA0         68           0x19 (0x3A)         PDRTB         PORTB7         PORTB6         PORTB5         PORTB3         PORTB2         PORTB1         PORTB0         69           0x16 (0x36)         PINB         PINB7         PINB6         PINB5         PINB5         PINB3         PINB2         PINB1         PINB0         69           0x16 (0x33)         GPIOR2         General Purpose UO Register 1         24 <td< td=""><td></td><td></td><td>-</td><td>-</td><td>EEPM1</td><td></td><td></td><td>EEMPE</td><td>EEPE</td><td>EERE</td><td></td></td<>			-	-	EEPM1			EEMPE	EEPE	EERE	
Dx19 (0x39)         PINA         -         -         -         PINA2         PINA1         PINA0         69           0x18 (0x38)         PORTB         PORTB7         PORTB6         PORTB5         PORTB4         PORTB3         PORTB2         PORTB0         69           0x17 (0x37)         DDRB         DDB7         DDB6         DDB5         DDB4         DDB3         DDB2         DDB1         DDB00         69           0x16 (0x36)         PINB         PINB7         PINB6         PINB6         PINB3         PINB2         PINB1         PINB0         69           0x16 (0x36)         GPIOR2         General Purpose U/O Register 2         24         24         24           0x13 (0x32)         GPIOR0         General Purpose U/O Register 0         24         24         24           0x12 (0x32)         PORTD         PORTD6         PORTD5         PORTD3         PORTD2         PORTD1         PORTD0         69           0x11 (0x30)         PIND         DDB6         DDD5         DDD4         DDD3         DDD2         DD01         DD00         69           0x06 (0x2F)         USIDR         USIDR         USIDA         USIDA         USICNT3         USICNT3         USICNT1		PORTA	-	-	-	-	-	PORTA2	PORTA1	PORTA0	68
0x18 (0x38)         PORTB         PORTB5         PORTB4         PORTB3         PORTB2         PORTB1         PORTB0         69           0x17 (0x37)         DDR8         DD87         DD86         DD85         DD84         DD83         DD82         DD81         DD80         69           0x16 (0x36)         PINB         PINB7         PINB6         PINB5         PINB4         PINB3         PINB2         PINB1         PINB0         69           0x15 (0x35)         GPIOR1         GEneral Purpose I/O Register 1         24         24           0x13 (0x33)         GPIOR0         GEneral Purpose I/O Register 0         24           0x13 (0x32)         PORTD         -         PORTD6         PORTD4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x11 (0x30)         PIND         -         PORTD6         PORTD5         PORTD3         PORTD2         PORTD1         PORTD0         69           0x06 (0x2E)         USIR         USIR         USIR         USINF         USIOF         USICA         USICAT1         USICAT1         USICAT0         164           0x06 (0x2E)         USIR         USINF         USIOF         USICA         USICAT1         USICAT1	0x1A (0x3A)	DDRA	-	-	-	-	-	DDA2	DDA1	DDA0	68
0x17 (0x37)         DDRB         DDB7         DD86         DDB5         DDB4         DDB3         DDB2         DDB1         DDB0         69           0x16 (0x36)         PINB         PINB7         PINB6         PINB6         PINB5         PINB3         PINB3         PINB2         PINB1         PINB0         69           0x16 (0x35)         GPIOR1         General Purpose I/O Register 1         24           0x13 (0x33)         GPIOR0         General Purpose I/O Register 0         24           0x13 (0x33)         GPIOR0         PORTD6         PORTD5         PORTD4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x11 (0x30)         PIND         -         PIND6         PIND5         PIND4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x01 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x06 (0x2C)         USIR         USISIE         USIOIE         USICAT<	0x19 (0x39)	PINA	-		-	-	-	PINA2		PINA0	69
0x16 (0x36)         PINB         PINB7         PINB6         PINB5         PINB4         PINB3         PINB2         PINB1         PINB0         69           0x15 (0x35)         GPIOR2         General Purpose I/O Register 2         24           0x14 (0x34)         GPIOR2         General Purpose I/O Register 0         24           0x13 (0x33)         GPIOR0         General Purpose I/O Register 0         24           0x12 (0x32)         PORTD         -         PORTD6         PORTD5         PORTD4         PORTD2         PORTD1         PORTD0         69           0x10 (0x30)         PIND         -         PORD6         POD5         PON4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x06 (0x2F)         USIDR         USIDR         USIDR         USICK1         USICNT0         164           0x06 (0x2C)         UDR         USINF         USIDC         USINT3         USICNT1         USICNT0         164           0x06 (0x2A)         UCSRA         RXC         TXC         UDRE         FE	· · · · · ·										
0x15 (0x35)         GPIOR2         General Purpose I/O Register 2         24           0x14 (0x34)         GPIOR1         General Purpose I/O Register 1         24           0x13 (0x33)         GPIOR0         General Purpose I/O Register 0         24           0x13 (0x32)         GPIOR1         -         PORTD6         PORTD5         PORTD4         PORTD2         PORTD1         PORTD0         69           0x11 (0x31)         DDR0         -         DDD6         DDD5         DDD4         DDD2         DDD1         DD00         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND2         PIND1         PIND0         69           0x06 (0x2F)         USIBR         USISIF         USIOF         USIPF         USIDC         USICNT3         USICNT1         USICNT1         USICNT1         USICNT1         USICNT1         USICNT1         USICNT1         105           0x06 (0x2E)         UJBR         USIOIE         USIWM1         USIWM0         USICS1         USICS0         USICK         USICNT1         USICNT1         105           0x06 (0x2A)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X											
0x14 (0x34)         GPIOR1         General Purpose I/O Register 1         24           0x13 (0x33)         GPIOR0         General Purpose I/O Register 0         24           0x12 (0x32)         PORTD         -         PORTD6         PORTD5         PORTD4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x11 (0x31)         DDRD         -         DDD6         DDD5         DDD4         DDD3         DDD2         DDD1         DDD0         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x06 (0x2F)         USIDR         -         USIOF         USIPF         USIDC         USICNT3         USICNT1         USICNT0         165           0x06 (0x2C)         USR         USISIF         USIOIF         USIW1         USIW0         USICS1         USICNT1         USICNT0         164           0x06 (0x2C)         UDR         VDR         VART bata Register         136         137         136         137         136           0x06 (0x2A)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X			PINB7	PINB6	PINB5				PINB1	PINB0	
0x13 (0x3)         GPIOR0         General Purpose I/O Register 0         24           0x12 (0x32)         PORTD         -         PORTD6         PORTD5         PORTD4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x11 (0x31)         DDR0         -         DDD6         DDD5         DDD4         DDD3         DDD2         DDD1         DD00         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x06 (0x2F)         USIDR         USIDR         USID4         PIND3         PIND2         USICNT1         USICNT0         165           0x06 (0x2D)         USICR         USISIF         USIOIF         USIVM1         USIVM0         USICS1         USICNT1         USICNT0         164           0x00 (0x2D)         USICR         USISIE         USIVM1         USIVM0         USICS1         USICNT1         USICNT0         162           0x06 (0x2B)         UCSRA         RXCIE         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x06 (0x28)         UCSRB         RXCIE         T	· · · · · ·						Ű				
0x12 (0x32)         PORTD         -         PORTD6         PORTD5         PORTD4         PORTD3         PORTD2         PORTD1         PORTD0         69           0x11 (0x31)         DDRD         -         DDD6         DDD5         DDD4         DD3         DDD2         DDD1         DDD0         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x0F (0x2F)         USIDR         USISR         USISR         USISF         USIOF         USIPF         USIC         USICNT3         USICNT2         USICNT1         USICNT0         164           0x0D (0x2D)         USICR         USISF         USIOF         USIVM1         USIWM0         USICS1         USICNT1         USICNT0         164           0x0D (0x2C)         UDR         -         UART Data Register (8-bit)         -         136           0x0A (0x2A)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x08 (0x28)         UGSRA         RXCIE         TXCIE         UDRIE         RXEN         TXEN         UCSZ2         RXB	· · · · · ·						ž				
0x11 (0x31)         DDRD         -         DDD6         DDD5         DDD4         DDD3         DDD2         DD11         DD00         69           0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x0F (0x2F)         USIDR         USISR         USISF         USIOF         USIPF         USIC         USICNT3         USICNT1         USICNT0         165           0x0E (0x2E)         USISR         USISF         USIOF         USIPF         USIDC         USICNT3         USICNT1         USICNT0         164           0x0D (0x2D)         USICR         USISE         USIWM1         USIWM0         USICS1         USICNT1         USICNT0         164           0x0C (0x2C)         UDR         -         -         UART Data Register (8-bit)         -         136           0x06 (0x2A)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x06 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167			_	PORTD6	PORTD5				PORTD1	PORTDO	
0x10 (0x30)         PIND         -         PIND6         PIND5         PIND4         PIND3         PIND2         PIND1         PIND0         69           0x0F (0x2F)         USIDR         USIDR         USIDR         165           0x0E (0x2E)         USISR         USISIF         USIOIF         USIPF         USIDC         USICNT3         USICNT1         USICNT0         164           0x0D (0x2D)         USICR         USISIE         USIOIE         USIWM1         USIWM0         USICS1         USICS0         USICK         USICC         162           0x0C (0x2C)         UDR         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x08 (0x2B)         UCSRA         RXCIE         TXCIE         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS0         167           0x09 (0x29)         UBRRL         USRRI[7:0]         UBRRH[7:0]         YEBR         TXEN         UCS22         RXB8         138           0x09 (0x28)         ACSR	· · · · · · · · · · · · · · · · · · ·		-								
OxOF (0x2F)         USIDR         USIOF         USIOF         USIPF         USIDC         USICNT3         USICNT2         USICNT1         USICNT0         165           0x0E (0x2E)         USISR         USISF         USIOF         USIPF         USIDC         USICNT3         USICNT2         USICNT1         USICNT0         164           0x0D (0x2D)         USICR         USISE         USIOE         USIVM1         USIVM0         USICS1         USICN0         USICLK         USIC         162           0x0C (0x2C)         UDR         UART Data Register (8-bit)         136         136         137         136           0x0A (0x2A)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x0A (0x2A)         UCSRB         RXCIE         TXCIE         UDRIE         RXEN         TXEN         UCSZ2         RXB8         TXB8         138           0x09 (0x29)         UBRRL         UBRRH[7:0]         140         140         140         140         140         0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS0         167         140         140			-								
Ox0E (0x2E)         USISR         USISIF         USIOIF         USIPF         USIDC         USICNT3         USICNT2         USICNT1         USICNT0         164           0x0D (0x2D)         USICR         USISIE         USIOIE         USIW1         USIWM0         USICS1         USICNT1         USICNT1         USICNT0         164           0x0D (0x2D)         USICR         USISIE         USIOIE         USIW1         USIWM0         USICS1         USICNT1         USICNT0         164           0x0C (0x2C)         UDR          UART Data Register (8-bit)         136         137           0x0A (0x2A)         UCSRB         RXCIE         TXCIE         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x0A (0x2A)         UCSRB         RXCIE         TXCIE         UDRIE         RXEN         TXEN         UCSZ2         RXB8         TXB8         138           0x09 (0x29)         UBRL          UBRRH[7:0]         140         140         140           0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167           0x06 (0x26)         PRR <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>·</td> <td></td> <td></td> <td></td>								·			
OXOC (0x2C)         UDR         UART Data Register (8-bit)         136           0x0B (0x2B)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x0A (0x2A)         UCSRB         RXCIE         TXCIE         UDRIE         RXEN         TXEN         UCS22         RXB8         TXB8         138           0x09 (0x29)         UBRRL         UBRRL         UBRRH[7:0]         140           0x06 (0x26)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167           0x07 (0x27)         BODCR         -         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         PRTIM1         PRTIM0         PRUSI         PRUSART         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT13         PCINT12         PCINT11         52           0x04 (0x24)         PCMSK1         -         -         -         -         PCINT10         PCINT9         PCINT8         52	0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF			USICNT2	USICNT1	USICNT0	164
Ox0B (0x2B)         UCSRA         RXC         TXC         UDRE         FE         DOR         UPE         U2X         MPCM         137           0x0A (0x2A)         UCSRB         RXCIE         TXCIE         UDRIE         RXEN         TXEN         UCS22         RXB8         TXB8         138           0x09 (0x29)         UBRRL         UBRRL         UBRRH[7:0]         140           0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167           0x07 (0x27)         BODCR         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         PRTIM1         PRTIM0         PRUSA         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT13         PCINT12         PCINT11         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRRH         -         -         -         -	0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	162
OXA (0x2A)         UCSRB         RXCIE         TXCIE         UDRIE         RXEN         TXEN         UCSZ2         RXB8         TXB8         138           0x09 (0x29)         UBRRL         UBRRL         UBRRH[7:0]         140           0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167           0x07 (0x27)         BODCR         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         PRTIM1         PRTIM0         PRUSI         PRUSART         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT13         PCINT12         PCINT11         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRRH         -         -         -         -         -         -         140           0x01 (0x21)         DIDR         -         -         -         -         -         -				Ι	I			Γ	I	1	
0x09 (0x29)         UBRRL         UBRRH[7:0]         140           0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167           0x07 (0x27)         BODCR         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         PRTIM1         PRTIM0         PRUSI         PRUSART         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT13         PCINT12         PCINT11         52           0x04 (0x24)         PCMSK1         -         -         -         -         PCINT10         PCINT8         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         -         AIN1D         AIN0D         168											
0x08 (0x28)         ACSR         ACD         ACBG         ACO         ACI         ACIE         ACIC         ACIS1         ACIS0         167           0x07 (0x27)         BODCR         -         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         -         PRTIM1         PRTIM0         PRUSI         PRUSART         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT14         PCINT13         PCINT12         PCINT11         52           0x04 (0x24)         PCMSK1         -         -         -         -         PCINT10         PCINT9         PCINT8         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         -         AIN1D         AIN0D         168			RXCIE	TXCIE	UDRIE			UCSZ2	RXB8	TXB8	
0x07 (0x27)         BODCR         -         -         -         -         -         BODS         BODSE         37           0x06 (0x26)         PRR         -         -         -         PRTIM1         PRTIM0         PRUSI         PRUSART         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT14         PCINT13         PCINT12         PCINT11         52           0x03 (0x24)         PCMSK1         -         -         -         -         PCINT10         PCINT13         PCINT12         PCINT11         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         -         H40           0x01 (0x21)         DIDR         -         -         -         -         AIN1D         AIN0D         168	· · · · · ·		405	4050	400			4010	40104	40100	
0x06 (0x26)         PRR         -         -         -         -         PRTIM1         PRTIM0         PRUSI         PRUSART         36           0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT14         PCINT13         PCINT12         PCINT11         52           0x04 (0x24)         PCMSK1         -         -         -         -         PCINT10         PCINT9         PCINT8         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         UBRRH[11:8]         140           0x01 (0x21)         DIDR         -         -         -         -         -         AIN1D         AIN0D         168	· · · · · ·										
0x05 (0x25)         PCMSK2         -         PCINT17         PCINT16         PCINT15         PCINT14         PCINT13         PCINT12         PCINT11         52           0x04 (0x24)         PCMSK1         -         -         -         -         PCINT10         PCINT12         PCINT11         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         UBRH[11:8]         140           0x01 (0x21)         DIDR         -         -         -         -         -         AIN1D         AIN0D         168											
0x04 (0x24)         PCMSK1         -         -         -         -         -         PCINT0         PCINT9         PCINT8         52           0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCS21         UCS20         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         UBRRH[11:8]         140           0x01 (0x21)         DIDR         -         -         -         -         AIN1D         AIN0D         168	· · · · · ·										
0x03 (0x23)         UCSRC         UMSEL1         UMSEL0         UPM1         UPM0         USBS         UCSZ1         UCSZ0         UCPOL         139           0x02 (0x22)         UBRH         -         -         -         -         UBRH         -         140           0x01 (0x21)         DIDR         -         -         -         -         AIN1D         AIN0D         168	· · · · · ·		_	-	-		-				
0x02 (0x22)         UBRRH         -         -         -         -         UBRRH[11:8]         140           0x01 (0x21)         DIDR         -         -         -         -         -         AIN1D         AIN0D         168			UMSEL1	UMSEL0	UPM1		USBS				
0x01 (0x21) DIDR AIN1D AIN0D 168											
0x00 (0x20)         USIBR         USI Buffer Register         166	· · · · · ·		-	-	-	-	-	_		AIN0D	
	0x00 (0x20)	USIBR				USI Buff	er Register				166

# 4. Register Summary

- Notes: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  - 2. I/O Registers within the address range 0x00 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  - Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
  - 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses.





# 5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND L	OGIC INSTRUCTIONS	5			
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd v Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
BRANCH INSTRUC	TIONS				
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	1	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC $\leftarrow$ PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC $\leftarrow$ PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC $\leftarrow$ PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N $\oplus$ V= 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N $\oplus$ V= 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then PC $\leftarrow$ PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then PC $\leftarrow$ PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BIT AND BIT-TEST		·			·
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
CBI	1 1 C				
CBI LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z.C.N.V	1
LSL LSR	Rd Rd	Logical Shift Left Logical Shift Right	$\begin{aligned} Rd(n+1) \leftarrow Rd(n),  Rd(0) \leftarrow 0 \\ \\ Rd(n) \leftarrow Rd(n+1),  Rd(7) \leftarrow 0 \end{aligned}$	Z,C,N,V Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=06	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	S	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	S	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	C ← 1	С	1
CLC		Clear Carry	C ← 0	С	1
SEN		Set Negative Flag	N ← 1	Ν	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	← 1	1	1
CLI		Global Interrupt Disable	← 0	1	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET	1	Set T in SREG	T ← 1	T	1
CLT	1	Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	Н	1
CLH		Clear Half Carry Flag in SREG	H ← 0	Н	1
DATA TRANSFER	INSTRUCTIONS				
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Post-Inc.	$X \leftarrow (X), X \leftarrow X + 1$ $X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$\frac{1}{Rd \leftarrow (Y)}$	None	2
LD				None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$		2
LDD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1$ , $(Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q,Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL IN	STRUCTIONS				
NOP		No Operation		None	1
		Sleep	(see specific descr. for Sleep function)	None	1
SLEEP		Gleep	(bee openine decent for eleop function)		
SLEEP WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1





# 6. Ordering Information

# 6.1 ATtiny2313A

Speed (MHz) <sup>(1)</sup>	Supply Voltage (V)	Temperature Range	Package <sup>(2)</sup>	Ordering Code <sup>(3)</sup>
		Industrial (-40°C to +85°C) <sup>(4)</sup>	20P3	ATtiny2313A-PU
			205	ATtiny2313A-SU
20	1.8 – 5.5		20\$	ATtiny2313A-SUR
			00144	ATtiny2313A-MU
			20M1	ATtiny2313A-MUR
			20M2 <sup>(5)(6)</sup>	ATtiny2313A-MMH
			201412 (3)(4)	ATtiny2313A-MMHR

Notes: 1. For speed vs. supply voltage, see section 22.3 "Speed" on page 199.

2. All packages are Pb-free, halide-free and fully green, and they comply with the European directive for Restriction of Hazardous Substances (RoHS).

- 3. Code indicators:
- H: NiPdAu lead finish
- U or N: matte tin
- R: tape & reel

4. Can also be supplied in wafer form. Contact your local Atmel sales office for ordering information and minimum quantities.

- 5. NiPdAu finish
- 6. Topside markings :
- 1st Line: T2313
- 2nd Line: Axx
- 3rd Line: xxx

	Package Type				
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)				
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)				
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead / Micro Lead Frame Package (MLF)				
20M2	20-pad, 3 x 3 x 0.85 mm Body, Very Thin Quad Flat No Lead Package (VQFN)				

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### 6.2 ATtiny4313

Speed (MHz) <sup>(1)</sup>	Supply Voltage (V)	Temperature Range	Package <sup>(2)</sup>	Ordering Code <sup>(3)</sup>
		Industrial (-40°C to +85°C) <sup>(4)</sup>	20P3	ATtiny4313-PU
			200	ATtiny4313-SU
	1.8 – 5.5		20S	ATtiny4313-SUR
20			00144	ATtiny4313-MU
			20M1 -	ATtiny4313-MUR
			(5)(6)	ATtiny4313-MMH
			20M2 <sup>(5)(6)</sup>	ATtiny4313-MMHR

Notes: 1. For speed vs. supply voltage, see section 22.3 "Speed" on page 199.

- 2. All packages are Pb-free, halide-free and fully green, and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
- 3. Code indicators:
- H: NiPdAu lead finish
- U or N: matte tin
- R: tape & reel
- 4. Can also be supplied in wafer form. Contact your local Atmel sales office for ordering information and minimum quantities.
- 5. NiPdAu finish
- 6. Topside markings:
- 1st Line: T4313
- 2nd Line: Axx
- 3rd Line: xxx

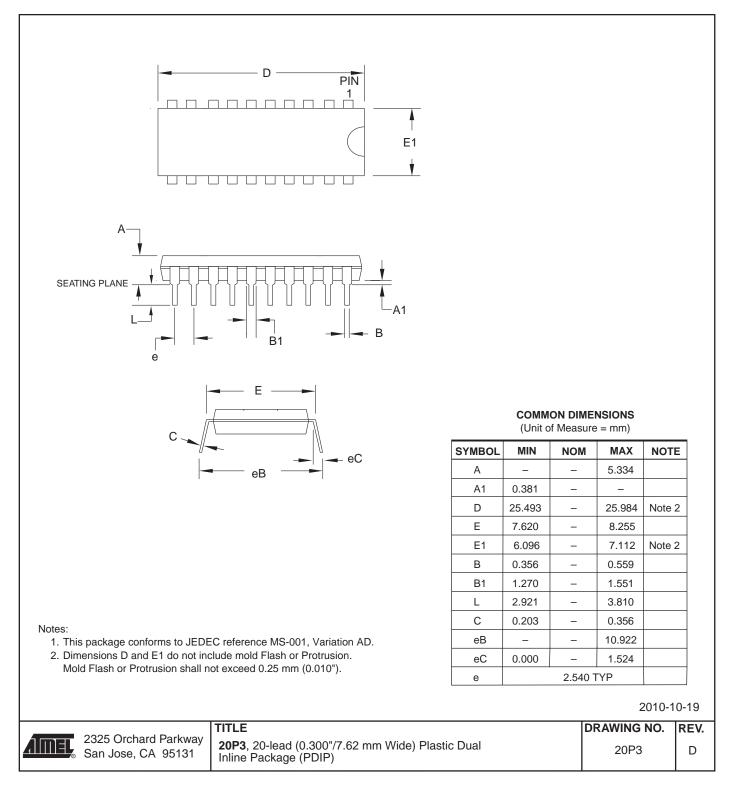
	Package Type				
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)				
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)				
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (MLF)				
20M2	20-pad, 3 x 3 x 0.85 mm Body, Very Thin Quad Flat No Lead Package (VQFN)				





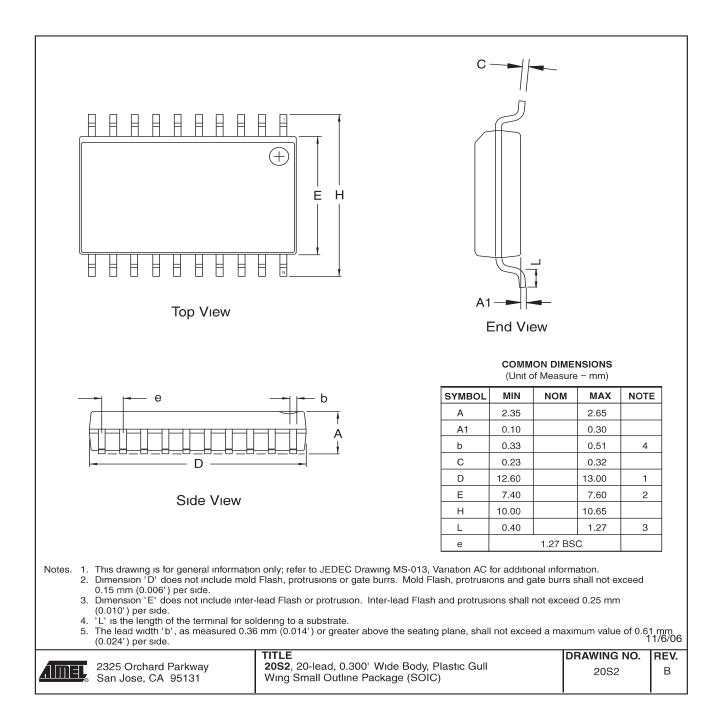
# 7. Packaging Information

## 7.1 20P3



# 14 ATtiny2313A/4313

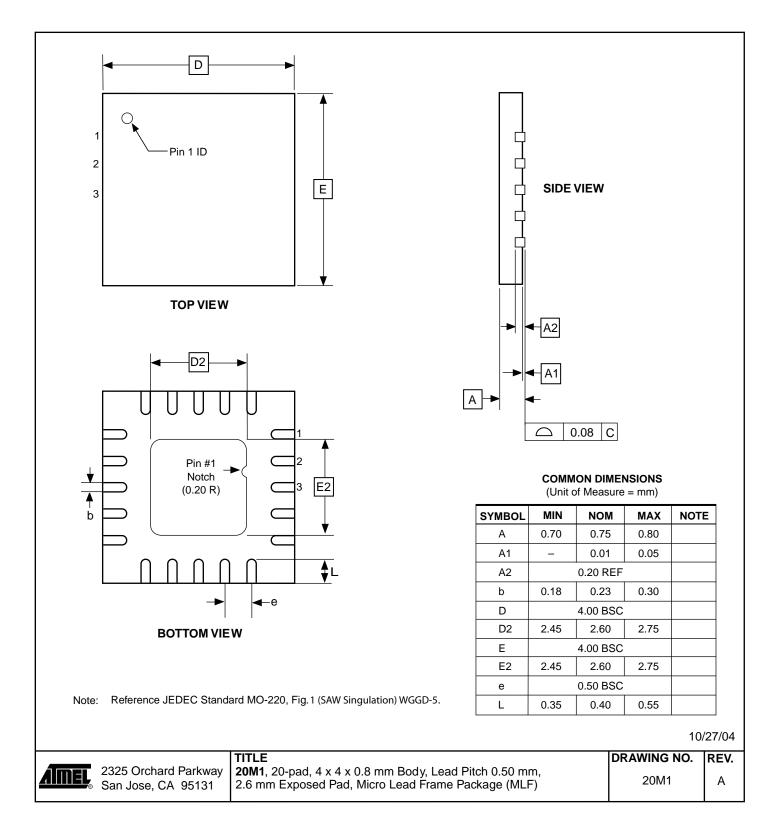
## 7.2 20S



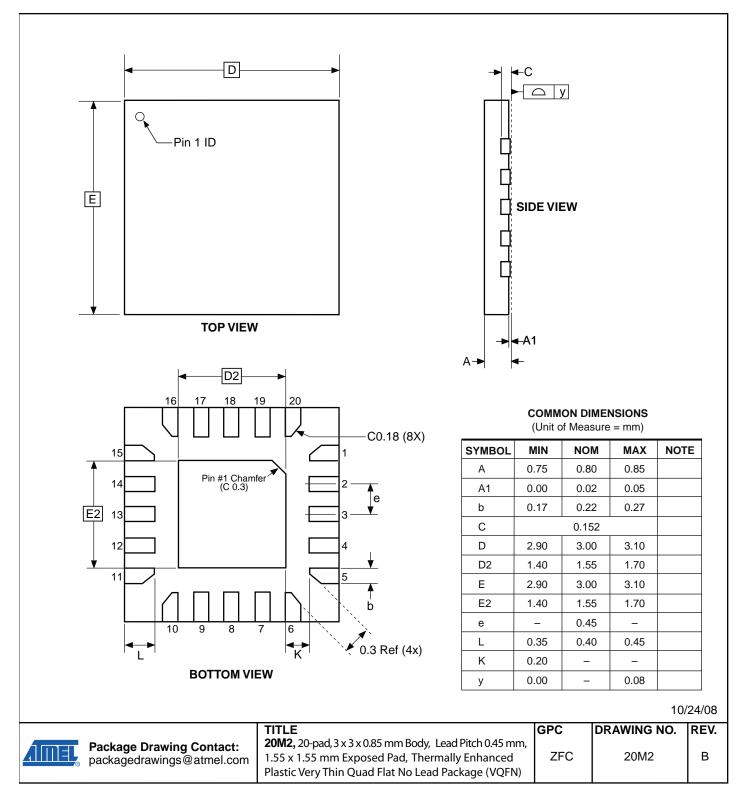




## 7.3 20M1



## 7.4 20M2







# 8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny2313A/4313 device.

## 8.1 ATtiny2313A

8.1.1 Rev. D

No known errata.

8.1.2 Rev. A – C These device revisions were referred to as ATtiny2313/ATtiny2313V.

## 8.2 ATtiny4313

### 8.2.1 Rev. A

No known errata.

# 9. Datasheet Revision History

### 9.1 Rev. 8246B - 10/11

- 1. Updated device status from Preliminary to Final.
- 2. Updated document template.
- 3. Added order codes for tape&reel devices, on page 259 and page 260
- 4. Updated figures:
  - Figure 23-33 on page 223
  - Figure 23-44 on page 228
  - Figure 23-81 on page 247
  - Figure 23-92 on page 252
- 5. Updated sections:
  - Section 5. "Memories" on page 15
  - Section 19. "Self-Programming" on page 172
  - Section 20. "Lock Bits, Fuse Bits and Device Signature" on page 177
  - Section 21. "External Programming" on page 183
  - Section 26. "Ordering Information" on page 259

### 9.2 Rev. 8246A – 11/09

- 1. Initial revision. Created from document 2543\_t2313.
- 2. Updated datasheet template.
- 3. Added VQFN in the Pinout Figure 1-1 on page 2.
- 4. Added Section 7.2 "Software BOD Disable" on page 34.
- 5. Added Section 7.3 "Power Reduction Register" on page 34.
- 6. Updated Table 7-2, "Sleep Mode Select," on page 36.
- 7. Added Section 7.5.3 "BODCR Brown-Out Detector Control Register" on page 37.
- 8. Added reset disable function in Figure 8-1 on page 38.
- 9. Added pin change interrupts PCINT1 and PCINT2 in Table 9-1 on page 47.
- 10. Added PCINT17..8 and PCMSK2..1 in Section 9.2 "External Interrupts" on page 48.
- 11. Added Section 9.3.4 "PCMSK2 Pin Change Mask Register 2" on page 52.
- 12. Added Section 9.3.5 "PCMSK1 Pin Change Mask Register 1" on page 52.
- 13. Updated Section 10.2.1 "Alternate Functions of Port A" on page 61.
- 14. Updated Section 10.2.2 "Alternate Functions of Port B" on page 62.
- 15. Updated Section 10.2.3 "Alternate Functions of Port D" on page 66.
- Added UMSEL1 and UMSEL0 in Section 14.10.4 "UCSRC USART Control and Status Register C" on page 139.
- 17. Added Section 15. "USART in SPI Mode" on page 145.
- Added USI Buffer Register (USIBR) in Section 16.2 "Overview" on page 155 and in Figure 16-1 on page 155.
- 19. Added Section 16.5.4 "USIBR USI Buffer Register" on page 166.
- 20. Updated Section 19.6.3 "Reading Device Signature Imprint Table from Firmware" on page 175.





- 21. Updated Section 19.7.1 "SPMCSR Store Program Memory Control and Status Register" on page 175.
- 22. Added Section 20.3 "Device Signature Imprint Table" on page 179.
- 23. Updated Section 20.3.1 "Calibration Byte" on page 180.
- 24. Changed BS to BS1 in Section 20.6.13 "Reading the Signature Bytes" on page 189.
- 25. Updated Section 22.2 "DC Characteristics" on page 198.
- 26. Added Section 23.1 "Effect of Power Reduction" on page 206.
- 27. Updated characteristic plots in Section 23. "Typical Characteristics" for ATtiny2313A (pages 207 230), and added plots for ATtiny4313 (pages 231 254).
- 28. Updated Section 24. "Register Summary" on page 255.
- 29. Updated Section 26. "Ordering Information" on page 259, added the package type 20M2 and the ordering code -MMH (VQFN), and added the topside marking note.





#### Headquarters

*Atmel Corporation* 2325 Orchard Parkway San Jose, CA 95131 USA Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

#### International

Atmel Asia Limited Unit 01-5 & 16, 19/F BEA Tower, Millennium City 5 418 Kwun Tong Road Kwun Tong, Kowloon HONG KONG Tel: (852) 2245-6100 Fax: (852) 2722-1369 Atmel Munich GmbH Business Campus Parkring 4 D-85748 Garching b. Munich GERMANY Tel: (+49) 89-31970-0 Fax: (+49) 89-3194621

#### Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 JAPAN Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

#### **Product Contact**

Web Site www.atmel.com

Technical Support avr@atmel.com Sales Contact www.atmel.com/contacts

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