

## Features

- Low capacitance for high speed interfaces
- Ultra low leakage: nA level
- Low operating voltage: 3.3V
- Ultra low clamping voltage
- Protects two lines in common and differential mode
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge:  $\pm 30\text{kV}$
    - Contact discharge:  $\pm 30\text{kV}$
  - IEC61000-4-5 (Lightning) 55A (8/20  $\mu\text{s}$ )
- RoHS Compliant
- Reference: LC03-3.3BTG, LC03-3.3.TBT

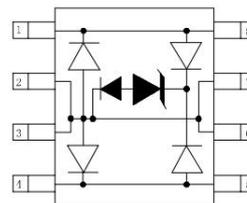
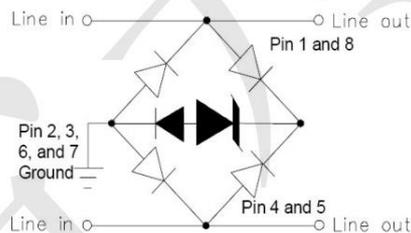
## Mechanical Characteristics

- Package: SO-8
- Lead Finish: Matte Tin
- Case Material: "Green" Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below
- Shipping Qty :2500pcs/7Inch Tape & Reel

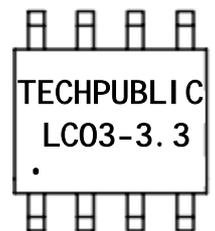
## Applications

- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- Set Top Box
- ISDN Interfaces
- Low Voltage Interfaces

## Dimensions and Pin Configuration



Marking:



**Absolute Maximum Ratings** (Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20μs)	Ppk	1500	W
Peak Pulse Current(8/20μs)	I <sub>PP</sub>	55	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V <sub>ESD</sub>	±30 ±30	kV
Operating Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

**Electrical Characteristics** (TA=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V <sub>RWM</sub>			3.3	V	
Punch-Through Voltage	V <sub>P</sub>	3.5			V	I <sub>T</sub> = 2μA
Snap-Back Voltage	V <sub>SB</sub>	2.8			V	I <sub>T</sub> = 50mA
Reverse Leakage Current	I <sub>R</sub>			0.5	μA	V <sub>RWM</sub> = 3.3V
Clamping Voltage	V <sub>C</sub>			7	V	I <sub>PP</sub> = 1A (8 x 20μs pulse), any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			22	V	I <sub>PP</sub> = 50A (8 x 20μs pulse), between I/O pins
Clamping Voltage	V <sub>C</sub>			25	V	I <sub>PP</sub> = 55A (8 x 20μs pulse), any I/O pin to ground
Junction Capacitance	C <sub>J</sub>		3	5	pF	V <sub>R</sub> = 0V, f = 1MHz, between I/O pins and ground
Junction Capacitance	C <sub>J</sub>		1.5	2.5	pF	V <sub>R</sub> = 0V, f = 1MHz, between I/O pins

**Typical Performance Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise Specified)**

Fig1. 8/20 $\mu\text{s}$  Pulse Waveform

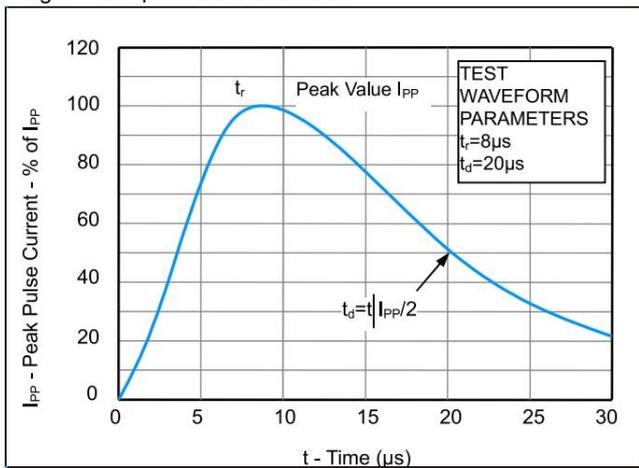


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

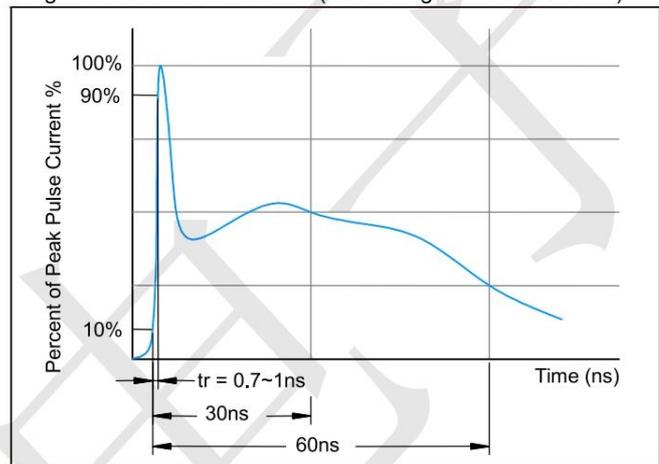
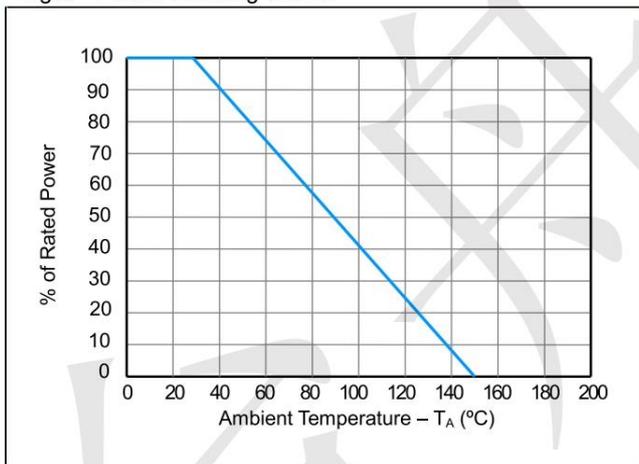
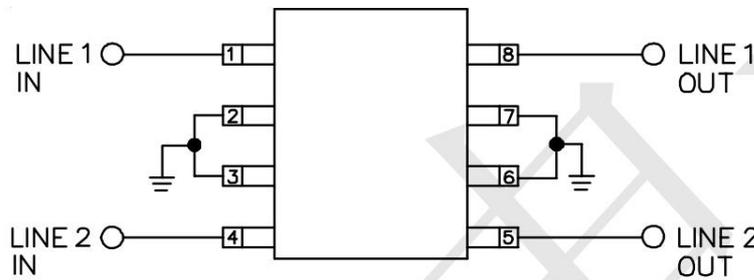


Fig3. Power Derating Curve

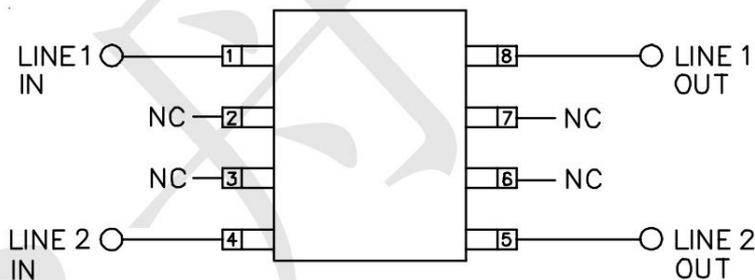


**Typical Application**

The LC03-3.3 is designed to protect two high speed data lines (one differential pair) from transient over - voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.



**Connection for differential (Line to Line) and common mode protection (Line to Ground)**



**Connection for differential protection (Line to Line)**

