

## Features

- Wide Range of Digital and Analog Signal Levels
  - Digital ..... 3V to 20V
  - Analog .....  $\leq 20V_{P-P}$
- Low ON Resistance, 125 $\Omega$  (Typ) Over 15V<sub>P-P</sub> Signal Input Range for  $V_{DD}-V_{EE} = 18V$
- High OFF Resistance, Channel Leakage of  $\pm 100pA$  (Typ) at  $V_{DD}-V_{EE} = 18V$
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V ( $V_{DD}-V_{SS} = 3V$  to 20V) to Switch Analog Signals to 20V<sub>P-P</sub> ( $V_{DD}-V_{EE} = 20V$ )
- Matched Switch Characteristics,  $r_{ON} = 5\Omega$  (Typ) for  $V_{DD}-V_{EE} = 15V$
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 $\mu W$  (Typ) at  $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V$
- Binary Address Decoding on Chip
- 5V, 10V, and 15V Parametric Ratings
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1 $\mu A$  at 18V Over Full Package Temperature Range, 100nA at 18V and 25 $^{\circ}C$
- Break-Before-Make Switching Eliminates Channel Overlap

## Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

## CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V<sub>P-P</sub> can be achieved by digital signal amplitudes of 4.5V to 20V (if  $V_{DD}-V_{SS} = 3V$ , a  $V_{DD}-V_{EE}$  of up to 13V can be controlled; for  $V_{DD}-V_{EE}$  level differences above 13V, a  $V_{DD}-V_{SS}$  of at least 4.5V is required). For example, if  $V_{DD} = +4.5V$ ,  $V_{SS} = 0V$ , and  $V_{EE} = -13.5V$ , analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD}-V_{SS}$  and  $V_{DD}-V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

## Ordering Information

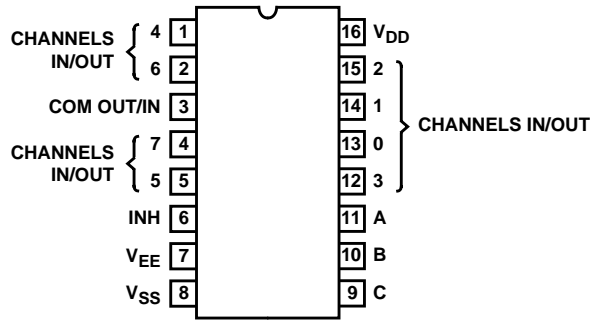
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4051BF3A, CD4052BF3A, CD4053BF3A	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BMT, CD4051BM96 CD4052BM, CD4052BMT, CD4052BM96 CD4053BM, CD4053BMT, CD4053BM96	-55 to 125	16 Ld SOIC
CD4051BNSR, CD4052BNSR, CD4053BNSR	-55 to 125	16 Ld SOP
CD4051BPW, CD4051BPWR, CD4052BPW, CD4052BPWR, CD4053BPW, CD4053BPWR	-55 to 125	16 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

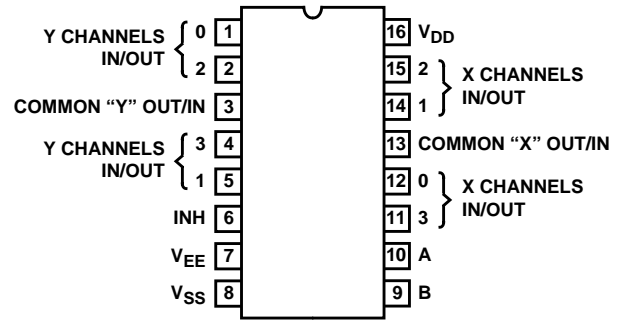
# CD4051B, CD4052B, CD4053B

## Pinouts

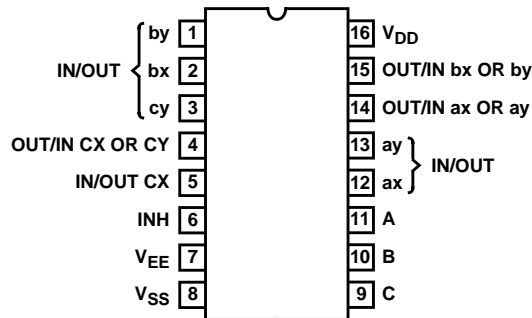
CD4051B (PDIP, CDIP, SOIC, SOP, TSSOP)  
TOP VIEW



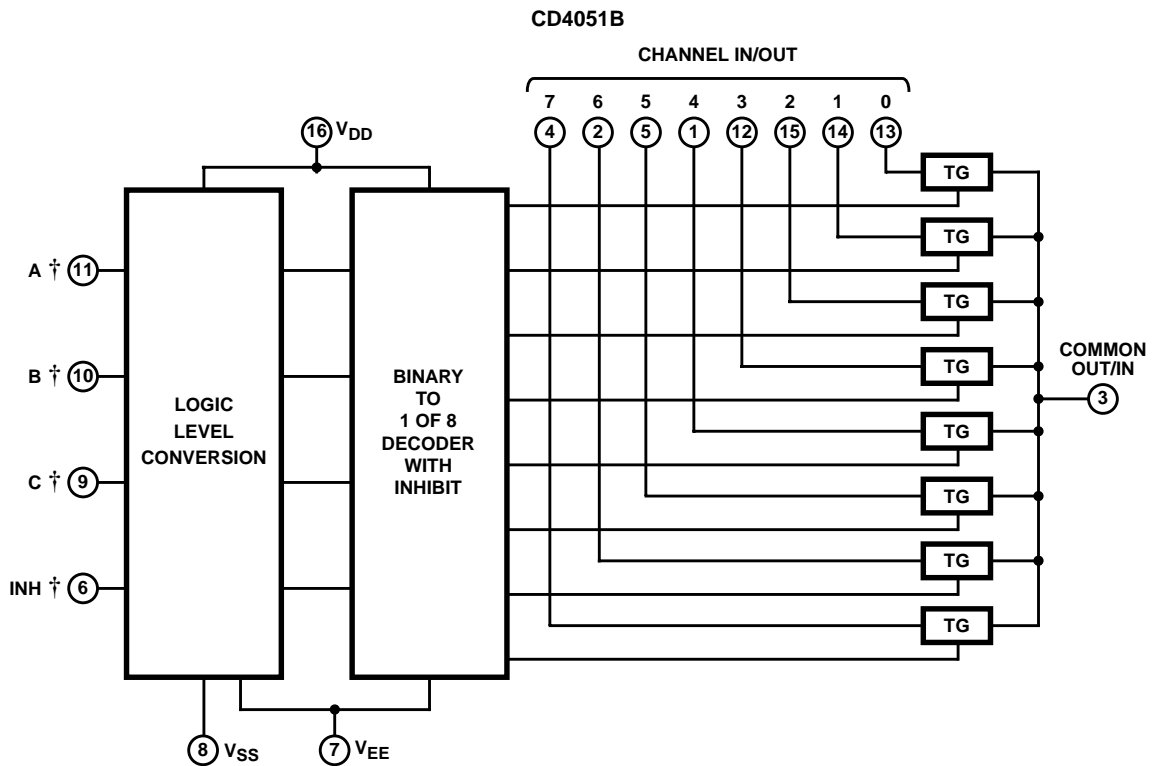
CD4052B (PDIP, CDIP, SOP, TSSOP)  
TOP VIEW



CD4053B (PDIP, CDIP, SOP, TSSOP)  
TOP VIEW



## Functional Block Diagrams

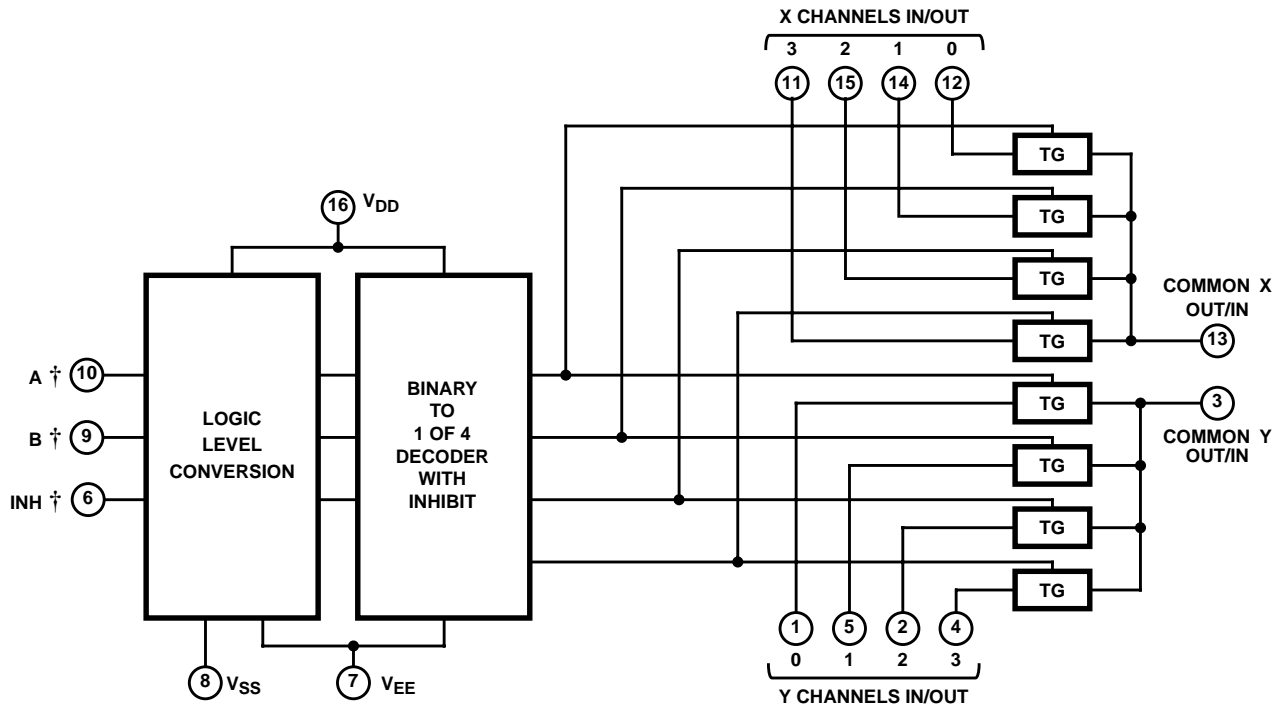


† All inputs are protected by standard CMOS protection network.

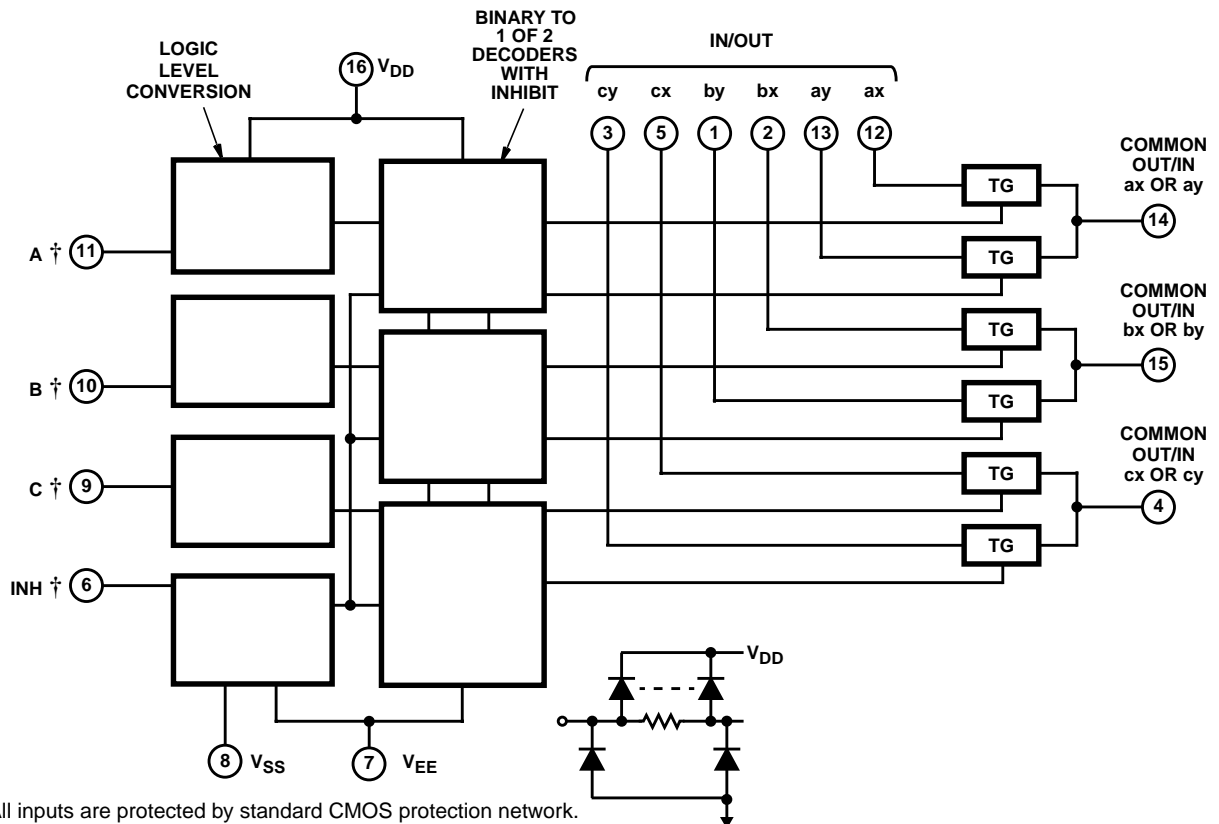
CD4051B, CD4052B, CD4053B

Functional Block Diagrams (Continued)

CD4052B



CD4053B



† All inputs are protected by standard CMOS protection network.

**CD4051B, CD4052B, CD4053B**

**TRUTH TABLES**

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
<b>CD4051B</b>				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
<b>CD4052B</b>				
INHIBIT	B		A	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
<b>CD4053B</b>				
INHIBIT	A OR B OR C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

X = Don't Care

# CD4051B, CD4052B, CD4053B

## Absolute Maximum Ratings

### Supply Voltage (V+ to V-)

Voltages Referenced to V<sub>SS</sub> Terminal . . . . . -0.5V to 20V  
 DC Input Voltage Range . . . . . -0.5V to V<sub>DD</sub> +0.5V  
 DC Input Current, Any One Input. . . . . ±10mA

## Operating Conditions

Temperature Range . . . . . -55°C to 125°C

## Thermal Information

### Package Thermal Impedance, θ<sub>JA</sub> (see Note 1):

E (PDIP) package. . . . . 67°C/W  
 M (SOIC) package . . . . . 73°C/W  
 NS (SOP) package. . . . . 64°C/W  
 PW (TSSOP) package . . . . . 108°C/W  
 Maximum Junction Temperature (Ceramic Package) . . . . . 175°C  
 Maximum Junction Temperature (Plastic Package) . . . . . 150°C  
 Maximum Storage Temperature Range. . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 265°C  
 (SOIC - Lead Tips Only)


*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Specifications

Common Conditions Here: If Whole Table is For the Full Temp. Range, V<sub>SUPPLY</sub> = ±5V, A<sub>V</sub> = +1, R<sub>L</sub> = 100Ω, Unless Otherwise Specified (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS												
	V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	-55	-40	85	125	25															
									MIN	TYP	MAX													
<b>SIGNAL INPUTS (V<sub>IS</sub>) AND OUTPUTS (V<sub>OS</sub>)</b>																								
Quiescent Device Current, I <sub>DD</sub> Max	-	-	-	5	5	5	150	150	-	0.04	5	μA												
	-	-	-	10	10	10	300	300	-	0.04	10	μA												
	-	-	-	15	20	20	600	600	-	0.04	20	μA												
	-	-	-	20	100	100	3000	3000	-	0.08	100	μA												
Drain to Source ON Resistance r <sub>ON</sub> Max 0 ≤ V <sub>IS</sub> ≤ V <sub>DD</sub>	-	0	0	5	800	850	1200	1300	-	470	1050	Ω												
	-	0	0	10	310	330	520	550	-	180	400	Ω												
	-	0	0	15	200	210	300	320	-	125	240	Ω												
Change in ON Resistance (Between Any Two Channels), Δr <sub>ON</sub>	-	0	0	5	-	-	-	-	-	15	-	Ω												
	-	0	0	10	-	-	-	-	-	10	-	Ω												
	-	0	0	15	-	-	-	-	-	5	-	Ω												
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)	-	0	0	18	±100 (Note 2)		±1000 (Note 2)		-	±0.01	±100 (Note 2)	nA												
Capacitance:	-	-5	5-	5																				
Input, C <sub>IS</sub>													-	-	-	-	-	5	-	pF				
Output, C <sub>OS</sub>																								
CD4051													-	-	-	-	-	-	-	-	30	-	pF	
CD4052													-	-	-	-	-	-	-	-	18	-	pF	
CD4053	-	-	-	-	-	-	-	-	9	-	pF													
Feedthrough C <sub>IOS</sub>	-	-	-	-	-	-	-	-	-	0.2	-	pF												
Propagation Delay Time (Signal Input to Output)		R <sub>L</sub> = 200kΩ, C <sub>L</sub> = 50pF, t <sub>r</sub> , t <sub>f</sub> = 20ns	5	-	-	-	-	-	-	30	60	ns												
			10	-	-	-	-	-	-	15	30	ns												
			15	-	-	-	-	-	-	10	20	ns												

## CD4051B, CD4052B, CD4053B

**Electrical Specifications** Common Conditions Here: If Whole Table is For the Full Temp. Range,  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_L = 100\Omega$ , Unless Otherwise Specified **(Continued)** (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	-55	-40	85	125	25			
									MIN	TYP	MAX	
<b>CONTROL (ADDRESS OR INHIBIT), <math>V_C</math></b>												
Input Low Voltage, $V_{IL}$ , Max	$V_{IL} = V_{DD}$ through 1k $\Omega$ ; $V_{IH} = V_{DD}$ through 1k $\Omega$	$V_{EE} = V_{SS}$ , $R_L = 1k\Omega$ to $V_{SS}$ , $I_{IS} < 2\mu A$ on All OFF Channels	5	1.5	1.5	1.5	1.5	-	-	1.5	V	
			10	3	3	3	3	-	-	3	V	
			15	4	4	4	4	-	-	4	V	
Input High Voltage, $V_{IH}$ , Min	$V_{IL} = V_{DD}$ through 1k $\Omega$ ; $V_{IH} = V_{DD}$ through 1k $\Omega$	$V_{EE} = V_{SS}$ , $R_L = 1k\Omega$ to $V_{SS}$ , $I_{IS} < 2\mu A$ on All OFF Channels	5	3.5	3.5	3.5	3.5	3.5	-	-	V	
			10	7	7	7	7	7	-	-	V	
			15	11	11	11	11	11	-	-	V	
Input Current, $I_{IN}$ (Max)	$V_{IN} = 0, 18$		18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$	
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figures 10, 11, 14	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	450	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-5	0	5	-	-	-	-	-	225	450	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 1k\Omega$	0	0	5	-	-	-	-	-	400	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-10	0	5	-	-	-	-	-	200	400	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	200	450	ns
		0	0	10	-	-	-	-	-	90	210	ns
		0	0	15	-	-	-	-	-	70	160	ns
		-10	0	5	-	-	-	-	-	130	300	ns
Input Capacitance, $C_{IN}$ (Any Address or Inhibit Input)				-	-	-	-	-	5	7.5	pF	

NOTE:

- Determined by minimum feasible leakage measurement for automatic testing.

### Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS		UNITS	
	$V_{IS}$ (V)	$V_{DD}$ (V)	$R_L$ (k $\Omega$ )	TYP			
Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)	5 (Note 3)	10	1	$V_{OS}$ at Common OUT/IN	CD4053	30	MHz
					CD4052	25	MHz
					CD4051	20	MHz
				$V_{EE} = V_{SS}$ , $20\text{Log} \frac{V_{OS}}{V_{IS}} = -3\text{dB}$	$V_{OS}$ at Any Channel	60	MHz

Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS			
	V <sub>IS</sub> (V)	V <sub>DD</sub> (V)	R <sub>L</sub> (kΩ)	TYP	UNITS		
Total Harmonic Distortion, THD	2 (Note 3)	5	10	0.3	%		
	3 (Note 3)	10		0.2	%		
	5 (Note 3)	15		0.12	%		
	V <sub>EE</sub> = V <sub>SS</sub> , f <sub>IS</sub> = 1kHz Sine Wave				%		
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V <sub>OS</sub> at Common OUT/IN	CD4053	8	MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$					CD4052	10
						CD4051	12
				V <sub>OS</sub> at Any Channel		8	MHz
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels		3	MHz
	V <sub>EE</sub> = V <sub>SS</sub> , 20Log $\frac{V_{OS}}{V_{IS}} = -40\text{dB}$			Between Sections, CD4052 Only	Measured on Common	6	MHz
					Measured on Any Channel	10	MHz
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	MHz
					In Pin 15, Out Pin 14	6	MHz
Address-or-Inhibit-to-Signal Crosstalk	-	10	10 (Note 4)			65	mV <sub>PEAK</sub>
	V <sub>EE</sub> = 0, V <sub>SS</sub> = 0, t <sub>r</sub> , t <sub>f</sub> = 20ns, V <sub>CC</sub> = V <sub>DD</sub> - V <sub>SS</sub> (Square Wave)					65	mV <sub>PEAK</sub>

NOTES:

- Peak-to-Peak voltage symmetrical about  $\frac{V_{DD} - V_{EE}}{2}$
- Both ends of channel.

Typical Performance Curves

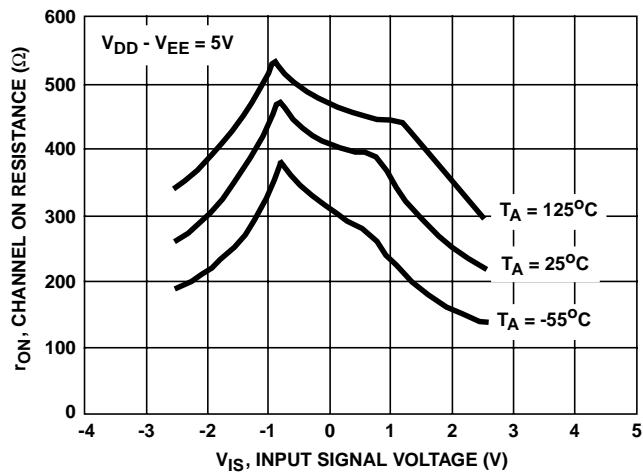


FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

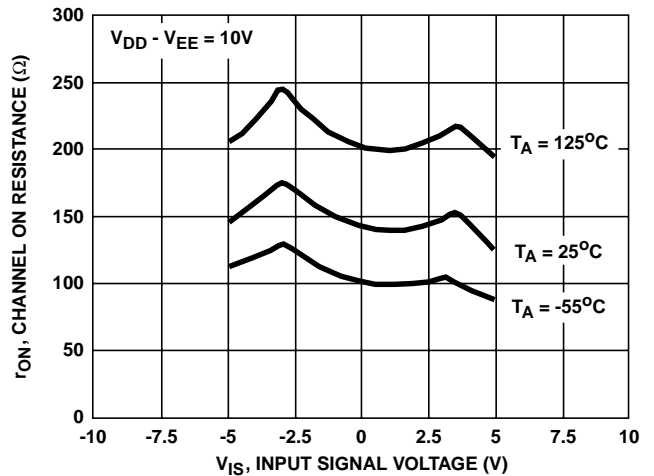


FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Curves (Continued)

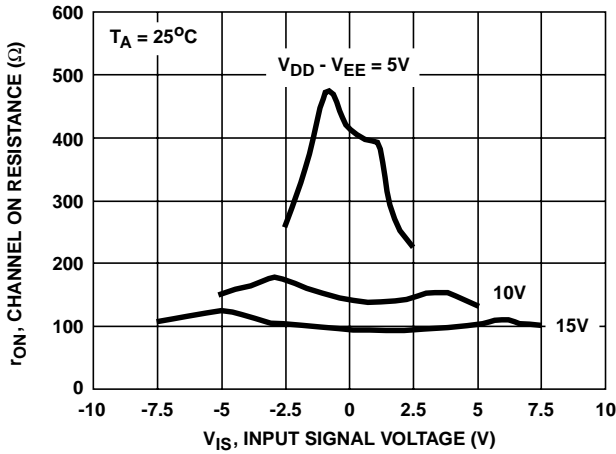


FIGURE 3. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

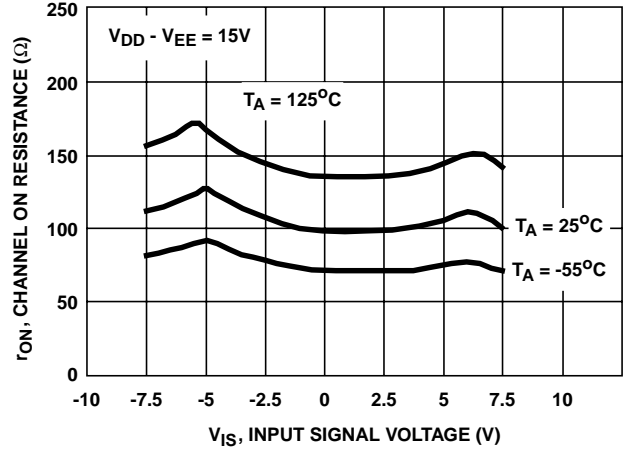


FIGURE 4. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

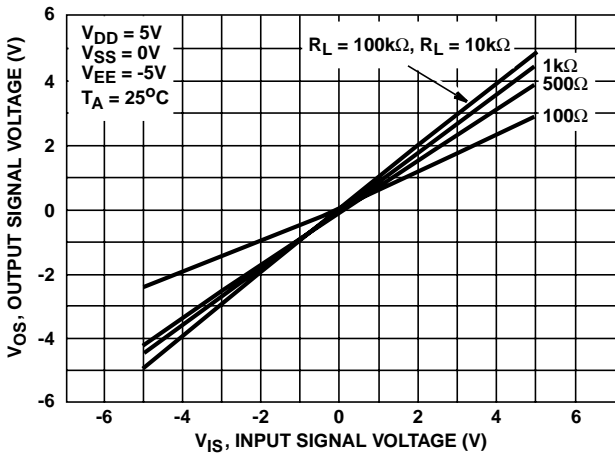


FIGURE 5. ON CHARACTERISTICS FOR 1 OF 8 CHANNELS (CD4051B)

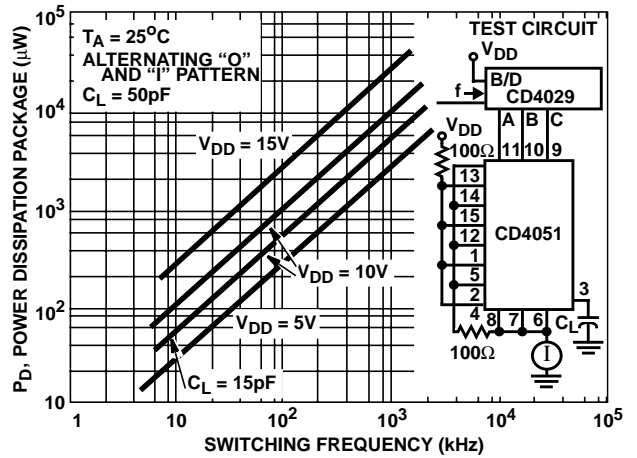


FIGURE 6. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4051B)

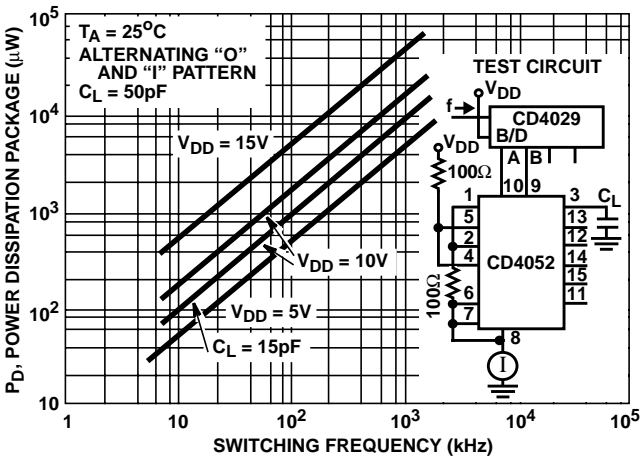


FIGURE 7. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4052B)

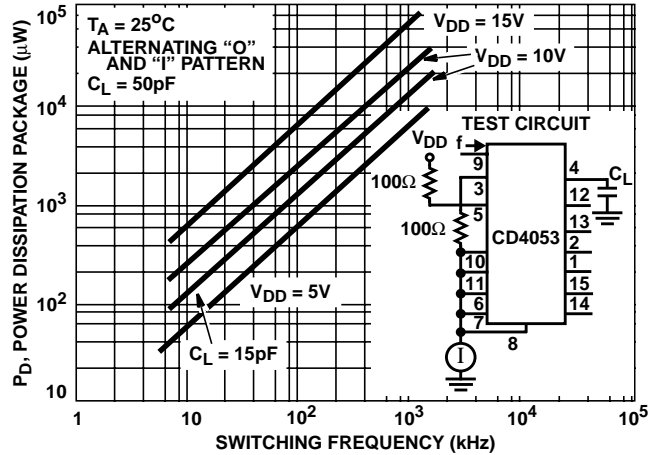
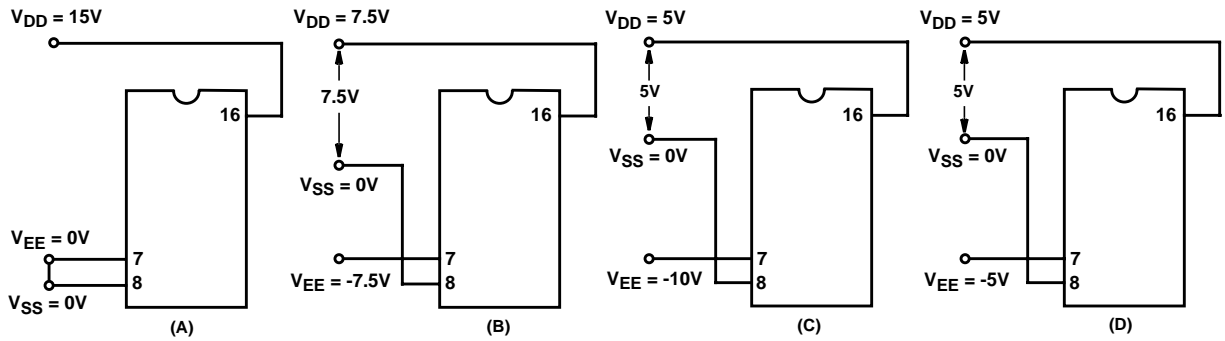


FIGURE 8. DYNAMIC POWER DISSIPATION vs SWITCHING FREQUENCY (CD4053B)



Test Circuits and Waveforms



NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" =  $V_{SS}$  and "1" =  $V_{DD}$ . The analog signal (through the TG) may swing from  $V_{EE}$  to  $V_{DD}$ .

FIGURE 9. TYPICAL BIAS VOLTAGES

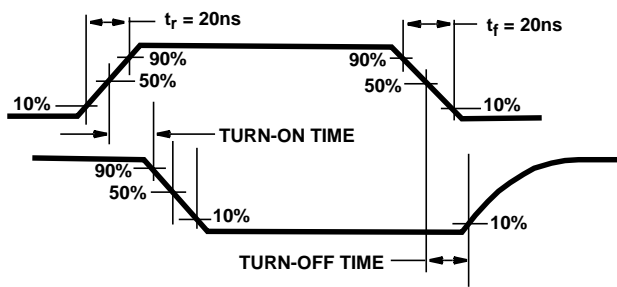


FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON ( $R_L = 1k\Omega$ )

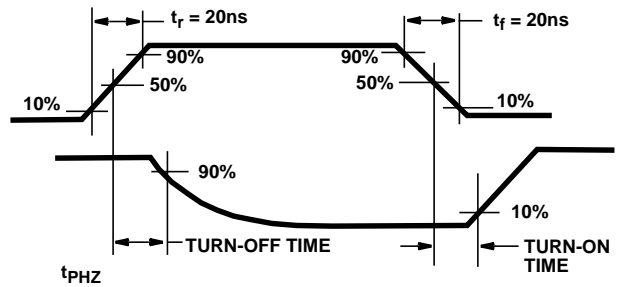


FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF ( $R_L = 1k\Omega$ )

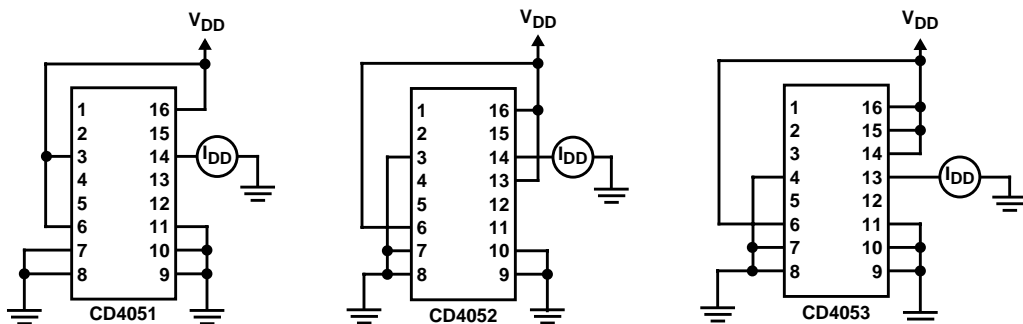


FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

Test Circuits and Waveforms (Continued)

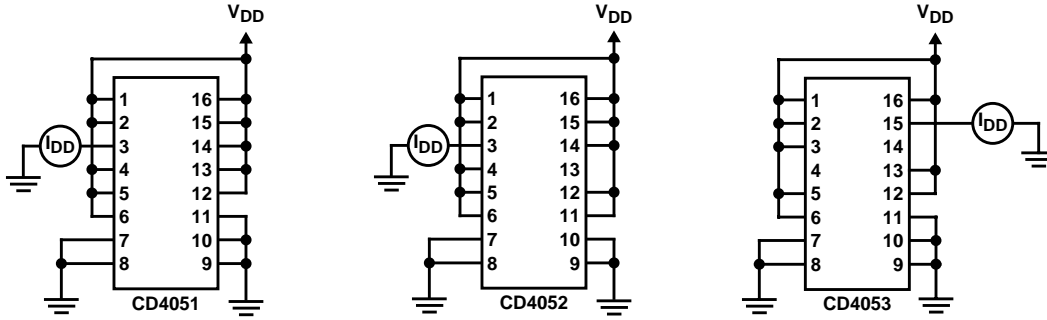


FIGURE 13. OFF CHANNEL LEAKAGE CURRENT - ALL CHANNELS OFF

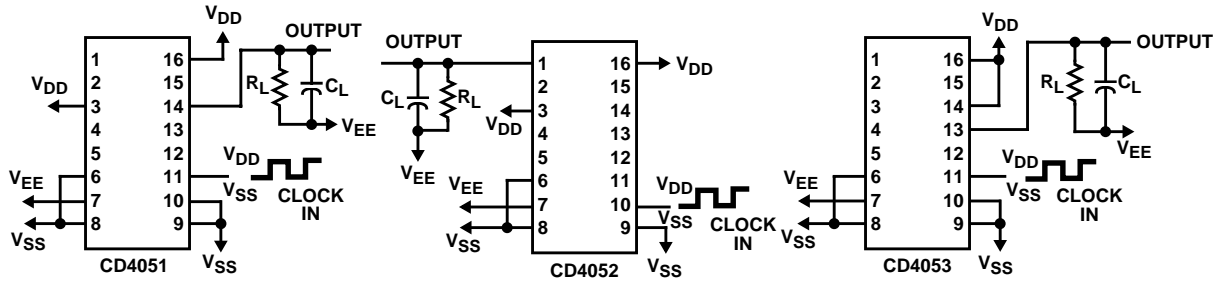


FIGURE 14. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT

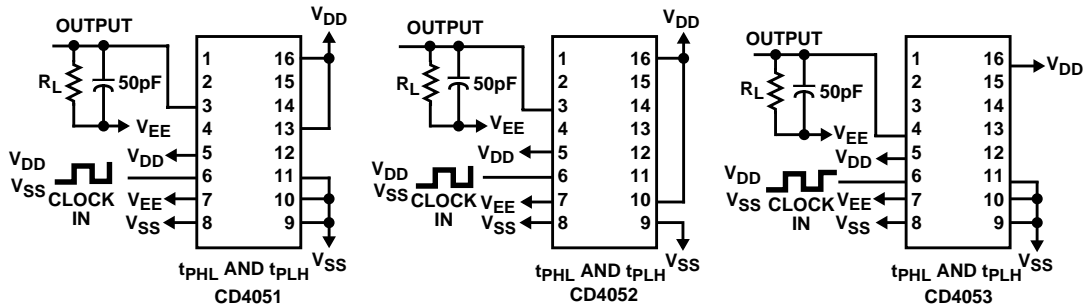
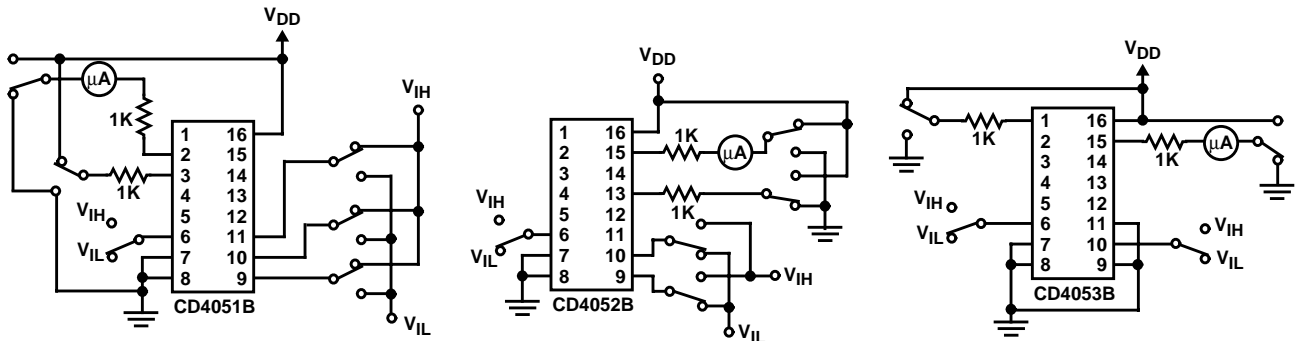


FIGURE 15. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT



MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 6)

MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL 2x)

MEASURE  $< 2\mu\text{A}$  ON ALL "OFF" CHANNELS (e.g., CHANNEL by)

FIGURE 16. INPUT VOLTAGE TEST CIRCUITS (NOISE IMMUNITY)

Test Circuits and Waveforms (Continued)

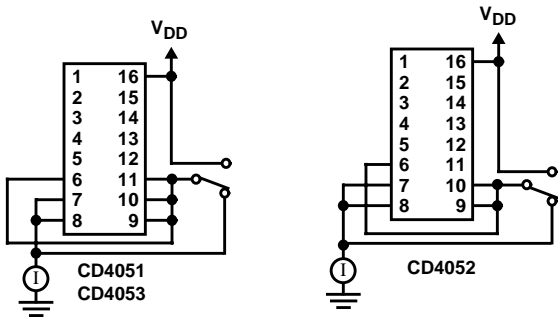


FIGURE 17. QUIESCENT DEVICE CURRENT

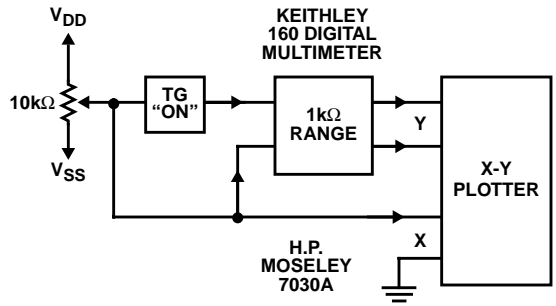


FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT

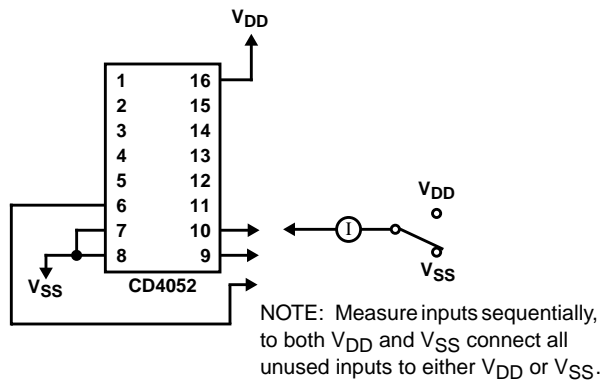
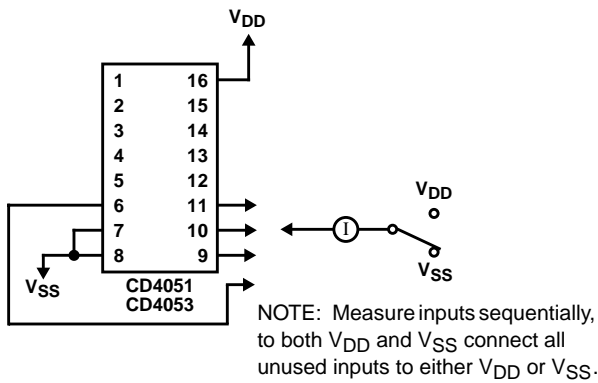


FIGURE 19. INPUT CURRENT

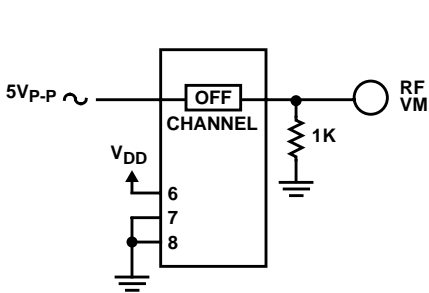


FIGURE 20. FEEDTHROUGH (ALL TYPES)

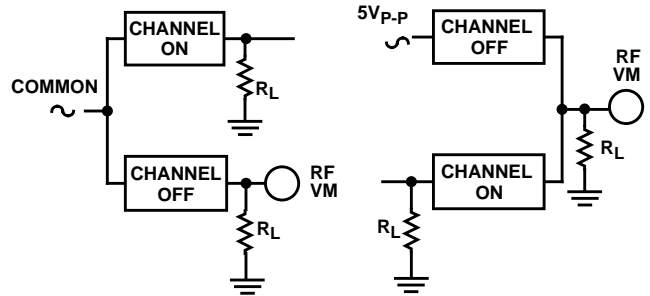


FIGURE 21. CROSSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)

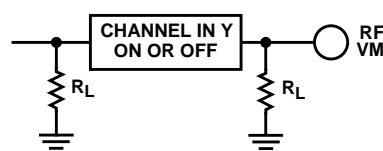
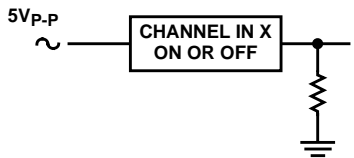


FIGURE 22. CROSSTALK BETWEEN DUALS OR TRIPLETS (CD4052B, CD4053B)

Test Circuits and Waveforms (Continued)

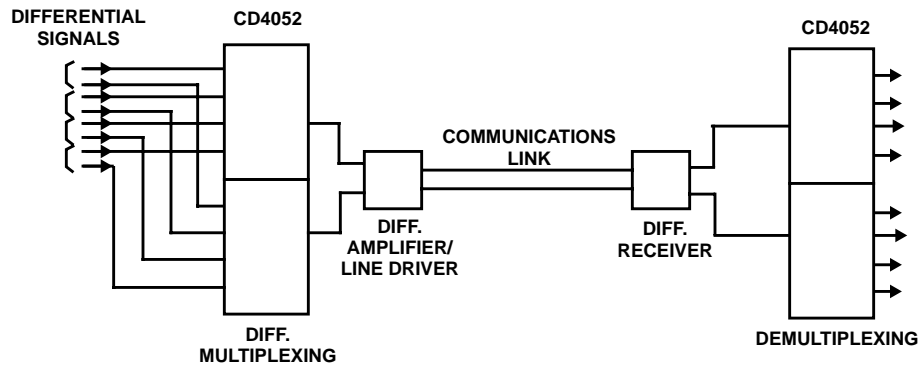


FIGURE 23. TYPICAL TIME-DIVISION APPLICATION OF THE CD4052B

**Special Considerations**

In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

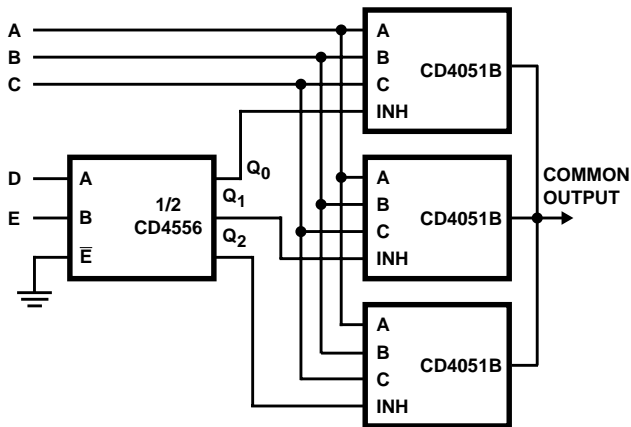


FIGURE 24. 24-TO-1 MUX ADDRESSING

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7901502EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	<a href="#">Samples</a>
8101801EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	<a href="#">Samples</a>
CD4051BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU   CU SN	N / A for Pkg Type	-55 to 125	CD4051BE	<a href="#">Samples</a>
CD4051BEE3	PREVIEW	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	CD4051BE	
CD4051BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4051BE	<a href="#">Samples</a>
CD4051BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4051BF	<a href="#">Samples</a>
CD4051BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4051BF3A	<a href="#">Samples</a>
CD4051BF3AS2283	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI			
CD4051BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BM96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B	<a href="#">Samples</a>
CD4051BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B	<a href="#">Samples</a>
CD4051BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	<a href="#">Samples</a>
CD4051BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4051BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	<a href="#">Samples</a>
CD4051BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	CM051B	<a href="#">Samples</a>
CD4051BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	<a href="#">Samples</a>
CD4052BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	<a href="#">Samples</a>
CD4052BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	<a href="#">Samples</a>
CD4052BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4052BF	<a href="#">Samples</a>
CD4052BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	<a href="#">Samples</a>
CD4052BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BM96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B	<a href="#">Samples</a>
CD4052BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B	<a href="#">Samples</a>
CD4052BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	<a href="#">Samples</a>
CD4052BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4052BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	CM052B	<a href="#">Samples</a>
CD4052BPWRG3	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	CM052B	<a href="#">Samples</a>
CD4052BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	<a href="#">Samples</a>
CD4053BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	<a href="#">Samples</a>
CD4053BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	<a href="#">Samples</a>
CD4053BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4053BF	<a href="#">Samples</a>
CD4053BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	<a href="#">Samples</a>
CD4053BF3AS2283	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI			
CD4053BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BM96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	<a href="#">Samples</a>
CD4053BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053B	<a href="#">Samples</a>
CD4053BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	<a href="#">Samples</a>
CD4053BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4053BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	CM053B	<a href="#">Samples</a>
CD4053BPWRG3	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	CM053B	<a href="#">Samples</a>
CD4053BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD4051B, CD4051B-MIL, CD4052B, CD4052B-MIL, CD4053B, CD4053B-MIL :**

- Catalog: [CD4051B](#), [CD4052B](#), [CD4053B](#)
  
- Automotive: [CD4051B-Q1](#), [CD4051B-Q1](#), [CD4053B-Q1](#), [CD4053B-Q1](#)
  
- Military: [CD4051B-MIL](#), [CD4052B-MIL](#), [CD4053B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



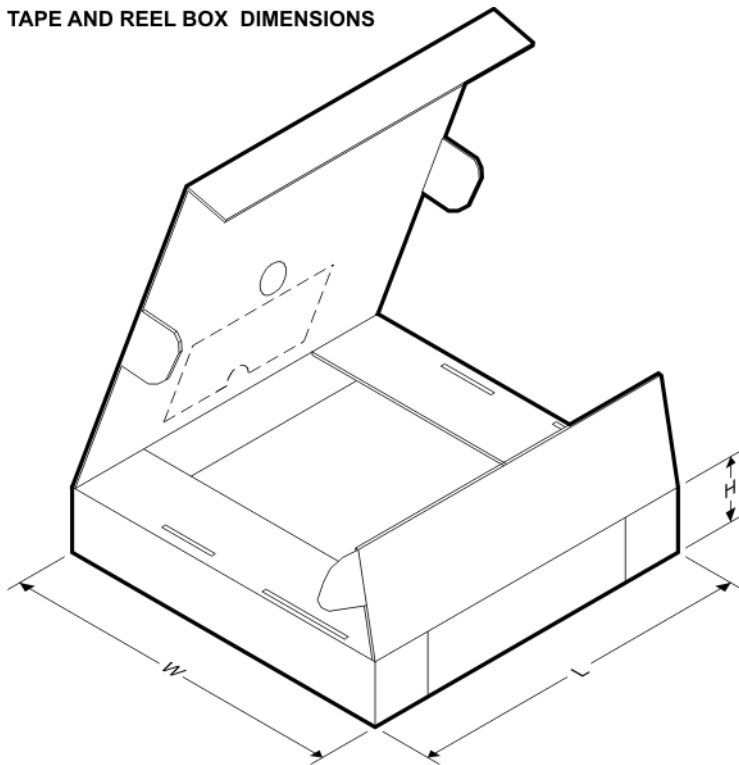
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4051BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4053BM96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BM96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4051BM96	SOIC	D	16	2500	364.0	364.0	27.0
CD4051BM96	SOIC	D	16	2500	367.0	367.0	38.0
CD4051BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4051BM96G4	SOIC	D	16	2500	367.0	367.0	38.0
CD4051BM96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD4051BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4051BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4052BM96	SOIC	D	16	2500	364.0	364.0	27.0
CD4052BM96G3	SOIC	D	16	2500	364.0	364.0	27.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4052BM96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD4052BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4052BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BPWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4052BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4053BM96	SOIC	D	16	2500	364.0	364.0	27.0
CD4053BM96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD4053BM96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD4053BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4053BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BPWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
CD4053BPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

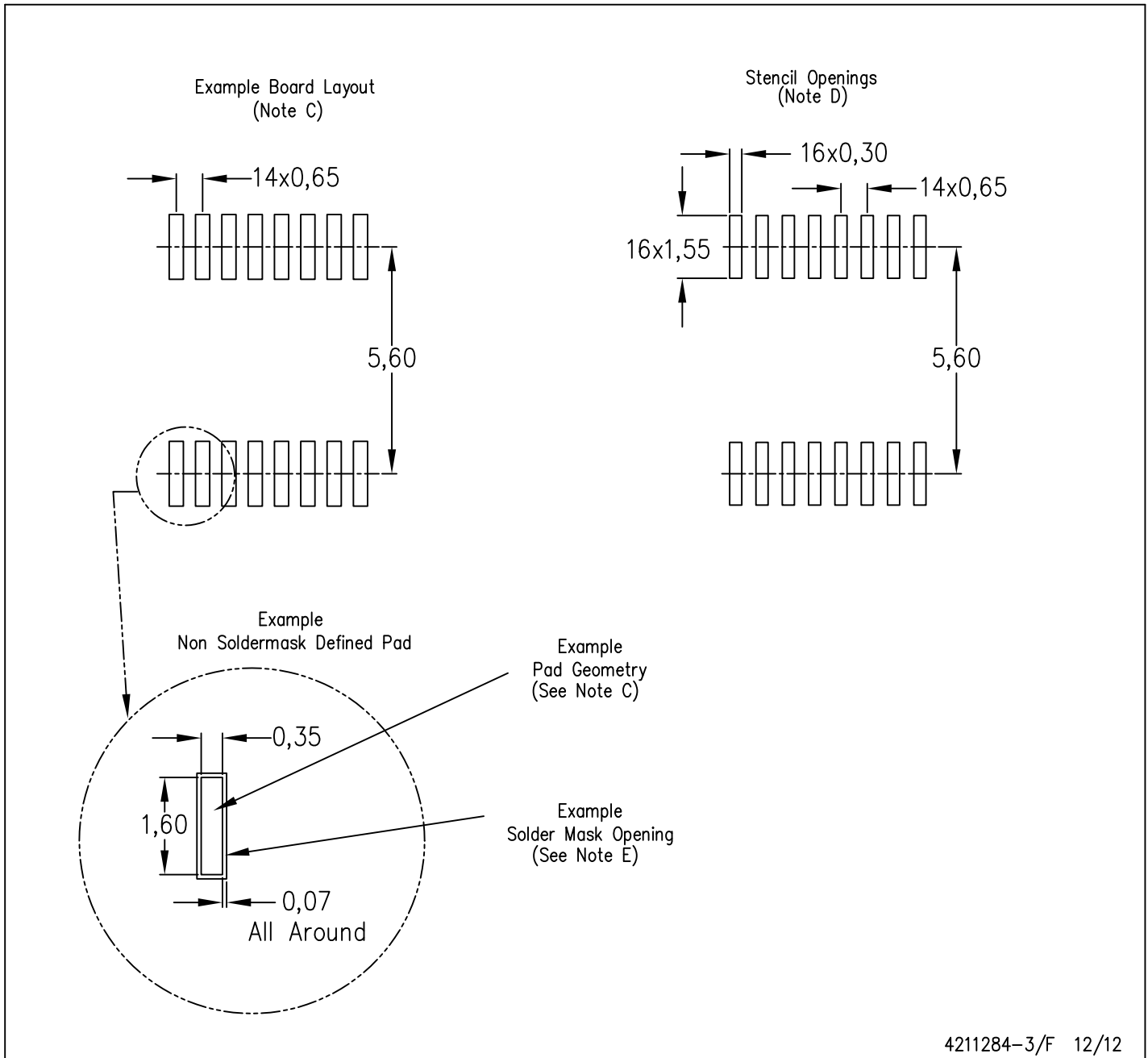


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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