TL594 Pulse-Width-Modulation Control Circuit

Check for Samples: TL594

FEATURES

- **Complete PWM Power-Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture Allows Easy Synchronization**
- **Undervoltage Lockout for Low-V_{CC} Conditions**

DESCRIPTION

The TL594 device incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. Designed primarily for power-supply control, this device offers the systems engineer the flexibility to tailor the power-supply control circuitry to a specific application.

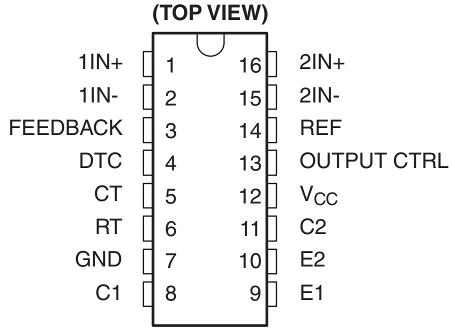
The TL594 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5-V regulator with a precision of 1%, an undervoltage lockout control circuit, and output control circuitry.

The error amplifiers have a common-mode voltage range of –0.3 V to V_{CC} – 2 V. The DTC comparator has a fixed offset that provides approximately 5% dead time. The on-chip oscillator can be bypassed by terminating RT to the reference output and providing a sawtooth input to CT, or it can be used to drive the common circuitry in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation, with selection by means of the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation. The undervoltage lockout control circuit locks the outputs off until the internal circuitry is operational.

The TL594C device is characterized for operation from 0°C to 70°C. The TL594I device is characterized for operation from –40°C to 85°C.

D, N, NS, OR PW PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

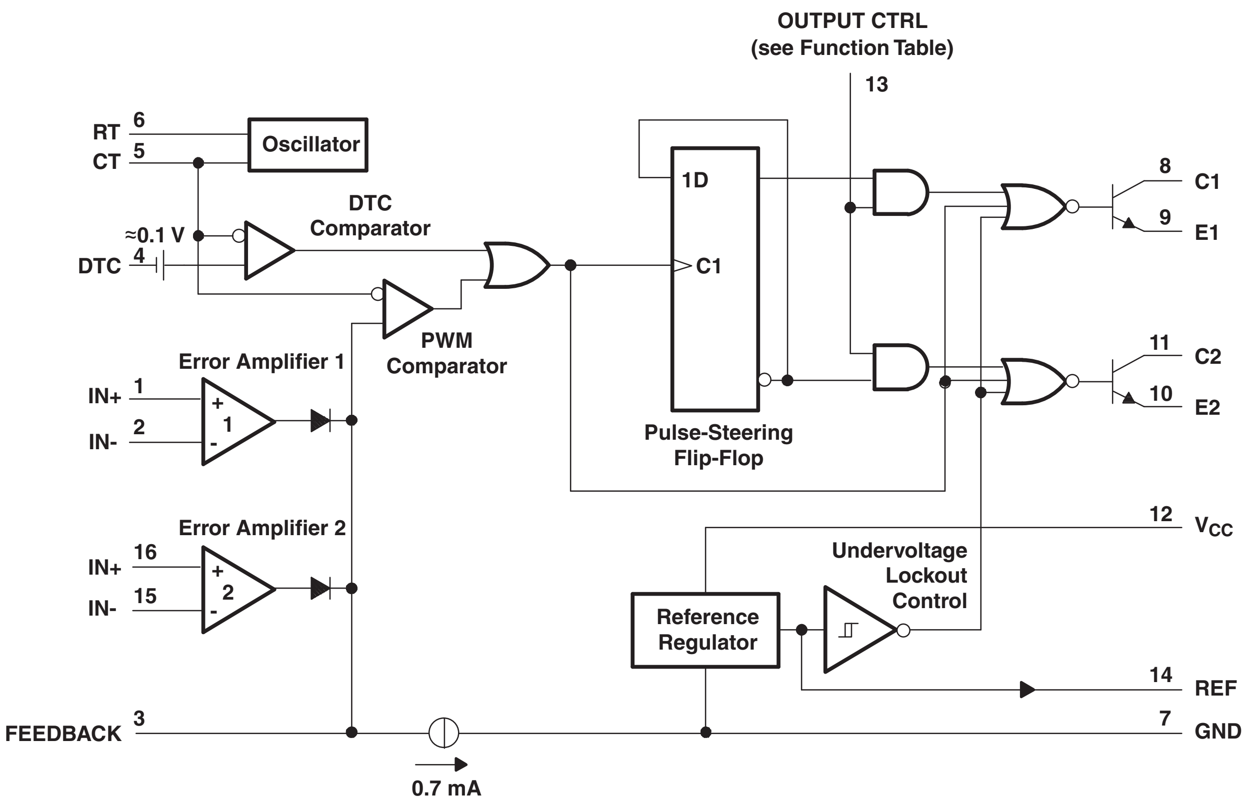
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Function Table

INPUT OUTPUT CTRL	OUTPUT FUNCTION
$V_I = 0$	Single-ended or parallel output
$V_I = V_{ref}$	Normal push-pull operation

Functional Block Diagram



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{CC}	Supply voltage[2]		41	V
	Amplifier input voltage		V_{CC} + 0.3	V
	Collector output voltage		41	V
	Collector output current		250	mA
θ_{JA}	Package thermal impedance[3][4]	D package	73	°C/W
		N package	67	
		NS package	64	
		PW package	108	
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		7	40	V
V_I	Amplifier input voltage		–0.3	V_{CC} – 2	V
V_O	Collector output voltage			40	V
	Collector output current (each transistor)			200	mA
	Current into FEEDBACK terminal			0.3	mA
C_T	Timing capacitor		0.47	10000	nF
R_T	Timing resistor		1.8	500	kΩ
f_{osc}	Oscillator frequency		1	300	kHz
T_A	Operating free-air temperature	TL594C	0	70	°C
		TL594I	–40	85	

Electrical Characteristics

V_{CC} = 15 V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
Reference Section					
Output voltage (REF)	I_O = 1 mA, T_A = 25°C	4.95	5	5.05	V
Input regulation	V_{CC} = 7 V to 40 V, T_A = 25°C		2	25	mV
Output regulation	I_O = 1 mA to 10 mA, T_A = 25°C		14	35	mV
Output-voltage change with temperature	ΔT_A = MIN to MAX		2	10	mV/V
Short-circuit output current(3)	V_{ref} = 0	10	35	50	mA
Amplifier Section (see Figure 1)					
Input offset voltage, error amplifier	FEEDBACK = 2.5 V		2	10	mV
Input offset current	FEEDBACK = 2.5 V		25	250	nA
Input bias current	FEEDBACK = 2.5 V		0.2	1	μA
Common-mode input voltage range, error amplifier	V_{CC} = 7 V to 40 V	0.3 to V_{CC} – 2			V
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V, T_A = 25°C	65	80		dB
Output sink current, FEEDBACK	V_{ID} = –15 mV to –5 V, FEEDBACK = 0.5 V	0.3	0.7		mA
Output source current, FEEDBACK	V_{ID} = 15 mV to 5 V, FEEDBACK = 3.5 V	–2			mA
Oscillator Section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 2)					
Frequency			10		kHz
Standard deviation of frequency(4)	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature(5)	ΔT_A = MIN to MAX			50	Hz/kHz
Dead-Time Control Section (see Figure 2)					
Input bias current	V_I = 0 to 5.25 V		–2	–10	μA
Maximum duty cycle, each output	DTC = 0 V	0.45			
Input threshold voltage	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			
Output Section					
Collector off-state current	V_C = 40 V, V_E = 0 V, V_{CC} = 40 V		2	100	μA
	DTC and OUTPUT CTRL = 0 V, V_C = 15 V, V_E = 0 V, V_{CC} = 1 V to 3 V		4	200	
Emitter off-state current	V_{CC} = V_C = 40 V, V_E = 0			–100	μA
Collector-emitter saturation voltage	Common emitter, V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower, V_C = 15 V, I_E = –200 mA		1.5	2.5	
Output control input current	V_I = V_{ref}			3.5	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values, except for parameter changes with temperature, are at T_A = 25°C.
(3) Duration of the short circuit should not exceed one second.
(4) Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N}(x_n - \overline{X})^2}{N - 1}}$$

(5) Temperature coefficient of timing capacitor and timing resistor is not taken into account.

Electrical Characteristics (continued)

V_{CC} = 15 V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
PWM Comparator Section (see Figure 2)						
Input threshold voltage, FEEDBACK	Zero duty cycle			4	4.5	V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V		0.3	0.7		mA
Undervoltage Lockout Section (see Figure 2)						
Threshold voltage	T_A = 25°C				6	V
	ΔT_A = MIN to MAX		3.5		6.9	
Hysteresis[6]			100			mV
Overall Device						
Standby supply current	R_T at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	DTC = 2 V, See Figure 2			12.4		mA

(6) Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

Switching Characteristics

V_{CC} = 15 V, T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output-voltage rise time	Common-emitter configuration (see Figure 3)		100	200	ns
Output-voltage fall time			30	100	ns
Output-voltage rise time	Emitter-follower configuration (see Figure 4)		200	400	ns
Output-voltage fall time			45	100	ns

Parameter Measurement Information

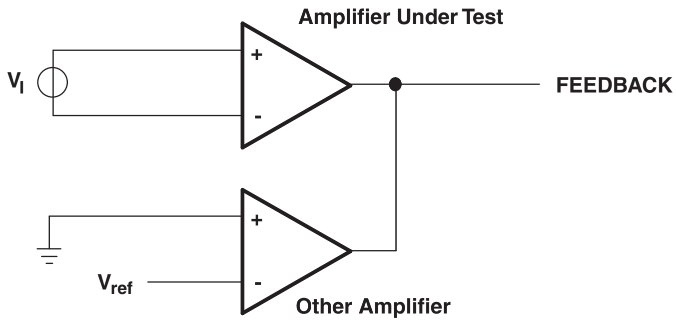
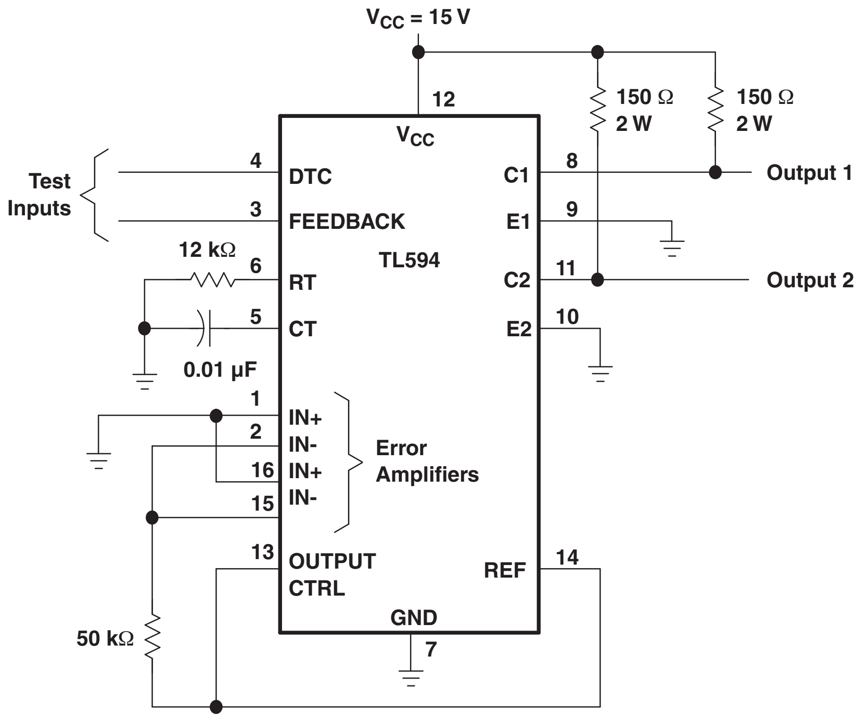
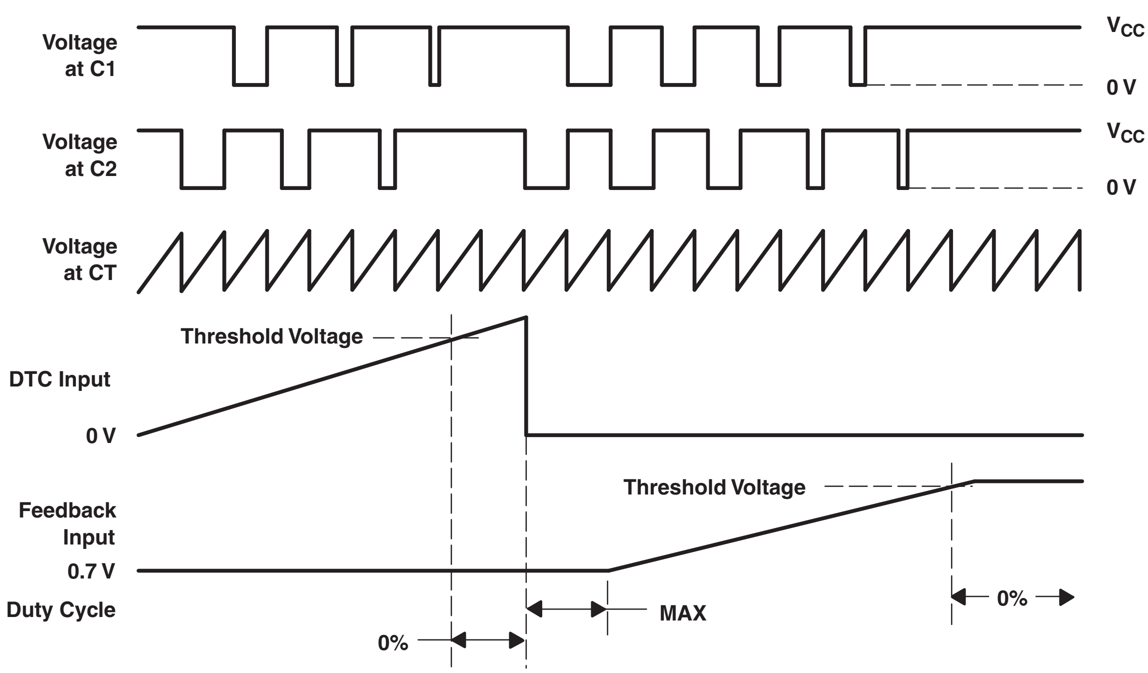


Figure 1. Amplifier-Characteristics Test Circuit

Parameter Measurement Information (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Operational Test Circuit and Waveforms

Parameter Measurement Information (continued)

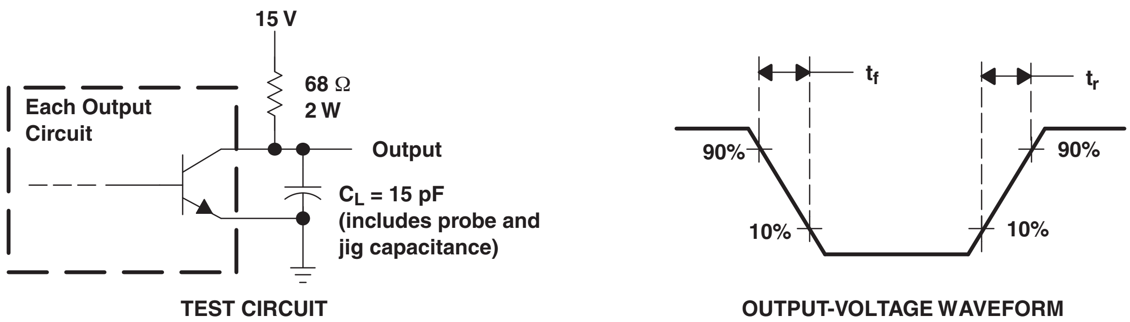


Figure 3. Common-Emitter Configuration

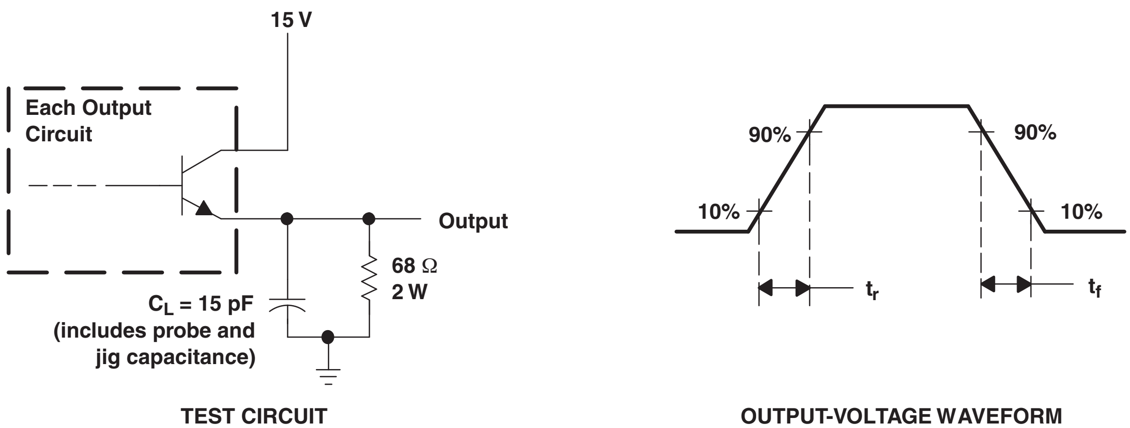
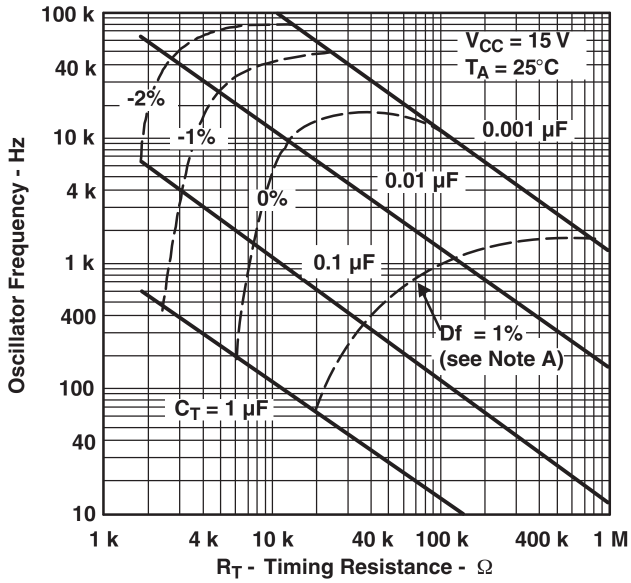


Figure 4. Emitter-Follower Configuration

Typical Characteristics



A. Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5. Oscillator Frequency and Frequency Variation vs Timing Resistance

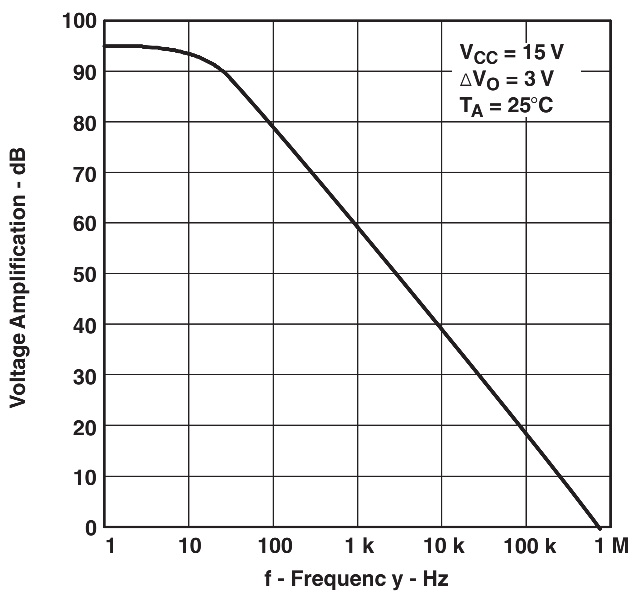


Figure 6. Amplifier Voltage Amplification vs Frequency

APPLICATION INFORMATION

How to Set Dead Time

The primary function of the dead-time control is to control the minimum off time of the output of the TL594 device. The dead-time control input provides control from 5% to 100% dead time. The TL594 device can be tailored to the specific power transistor switches that are used, to ensure that the output transistors never experience a common on-time. The bias circuit for the basic function is shown in Figure 7.

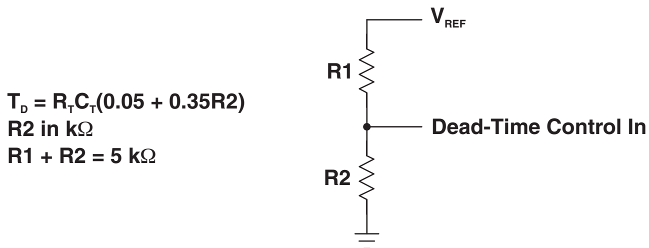


Figure 7. Setting Dead Time

REVISION HISTORY

Changes from Revision G (January 2007) to Revision H	Page
• Updated document to new TI data sheet format - no specification changes.	1
• Added ESD warning.	2
• Removed Ordering Information table.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL594CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594C	Samples
TL594CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594C	Samples
TL594CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594C	Samples
TL594CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	TL594C	Samples
TL594CDRG3	PREVIEW	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	TL594C	
TL594CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594C	Samples
TL594CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL594CN	Samples
TL594CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL594CN	Samples
TL594CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594	Samples
TL594CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594	Samples
TL594CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T594	Samples
TL594CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T594	Samples
TL594CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T594	Samples
TL594ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I	Samples
TL594IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I	Samples
TL594IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I	Samples
TL594IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL594IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL594IN	Samples
TL594INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL594IN	Samples
TL594INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I	Samples
TL594INSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I	Samples
TL594IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z594	Samples
TL594IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z594	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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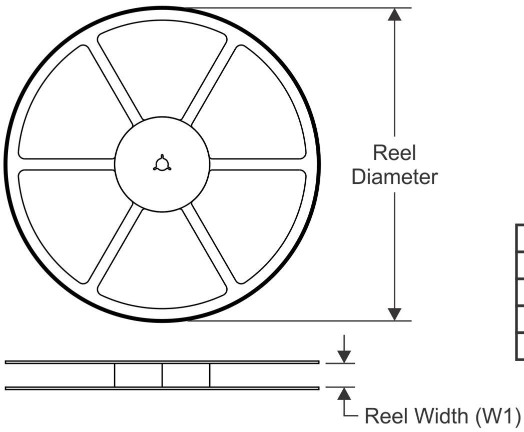
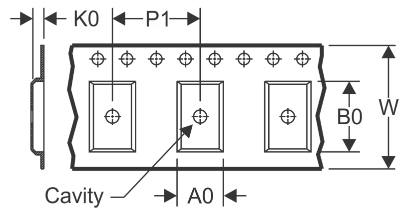
TAPE AND REEL INFORMATION

REEL DIMENSIONS

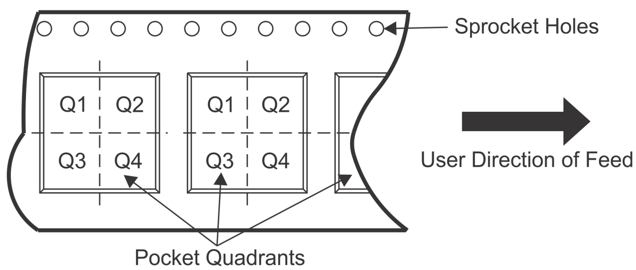


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

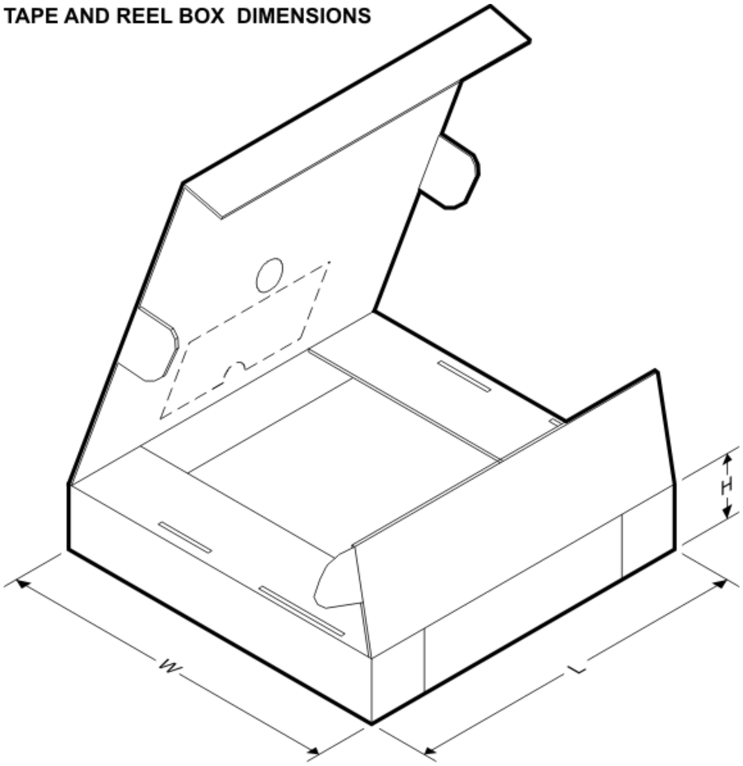
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL594CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL594CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL594CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL594IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL594IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

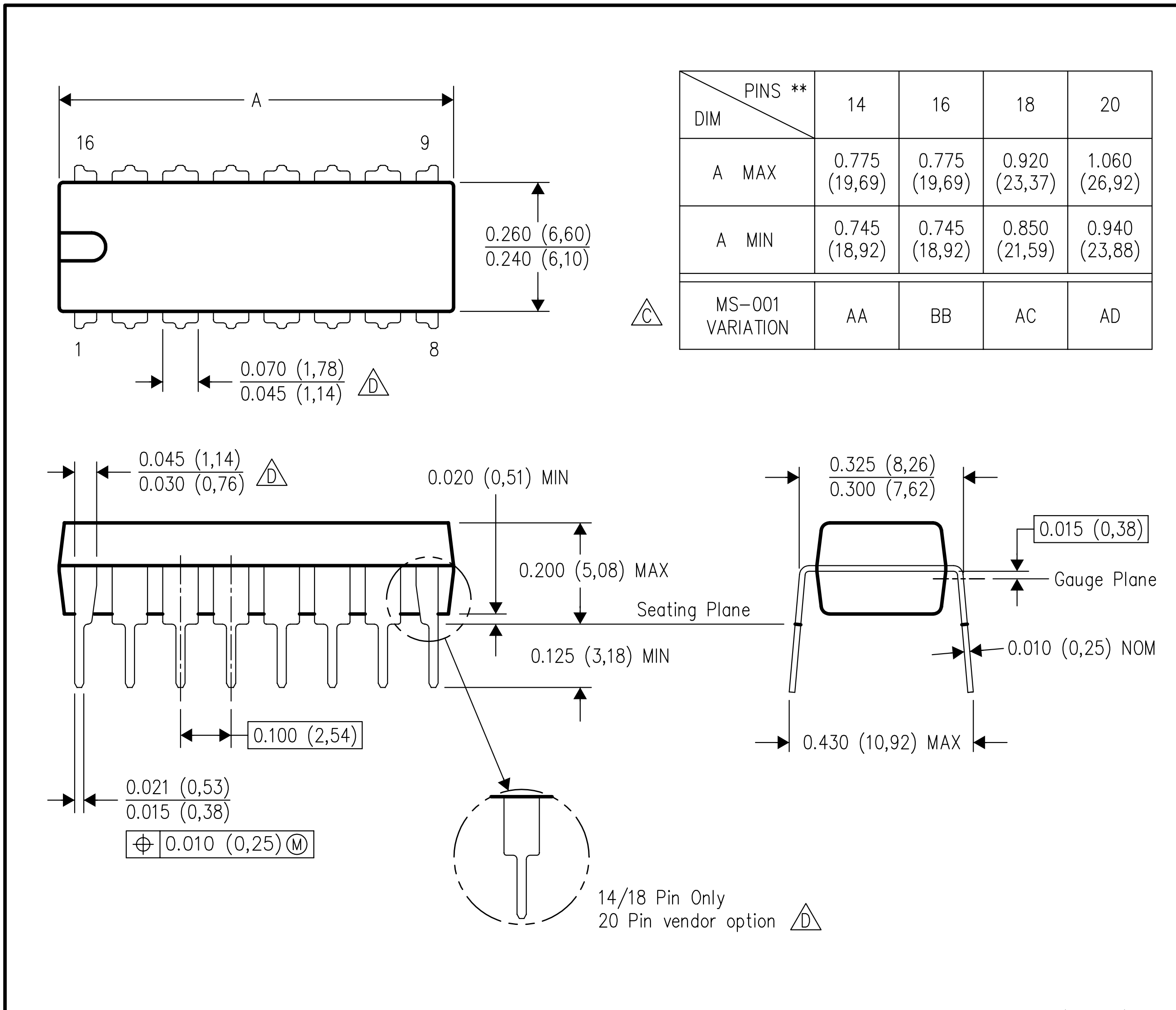


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL594CDR	SOIC	D	16	2500	333.2	345.9	28.6
TL594CDRG4	SOIC	D	16	2500	333.2	345.9	28.6
TL594CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TL594IDR	SOIC	D	16	2500	333.2	345.9	28.6
TL594IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

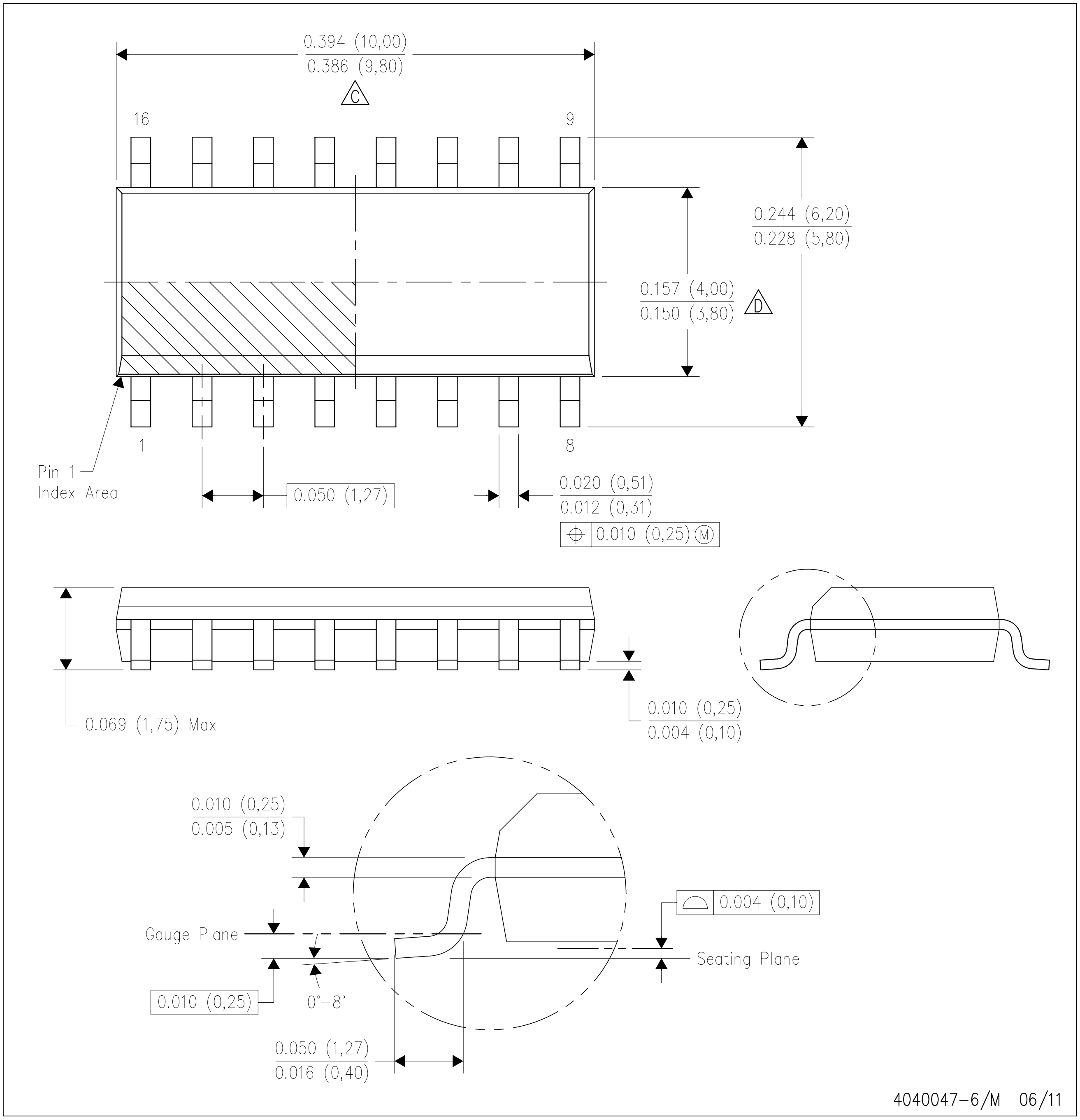


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

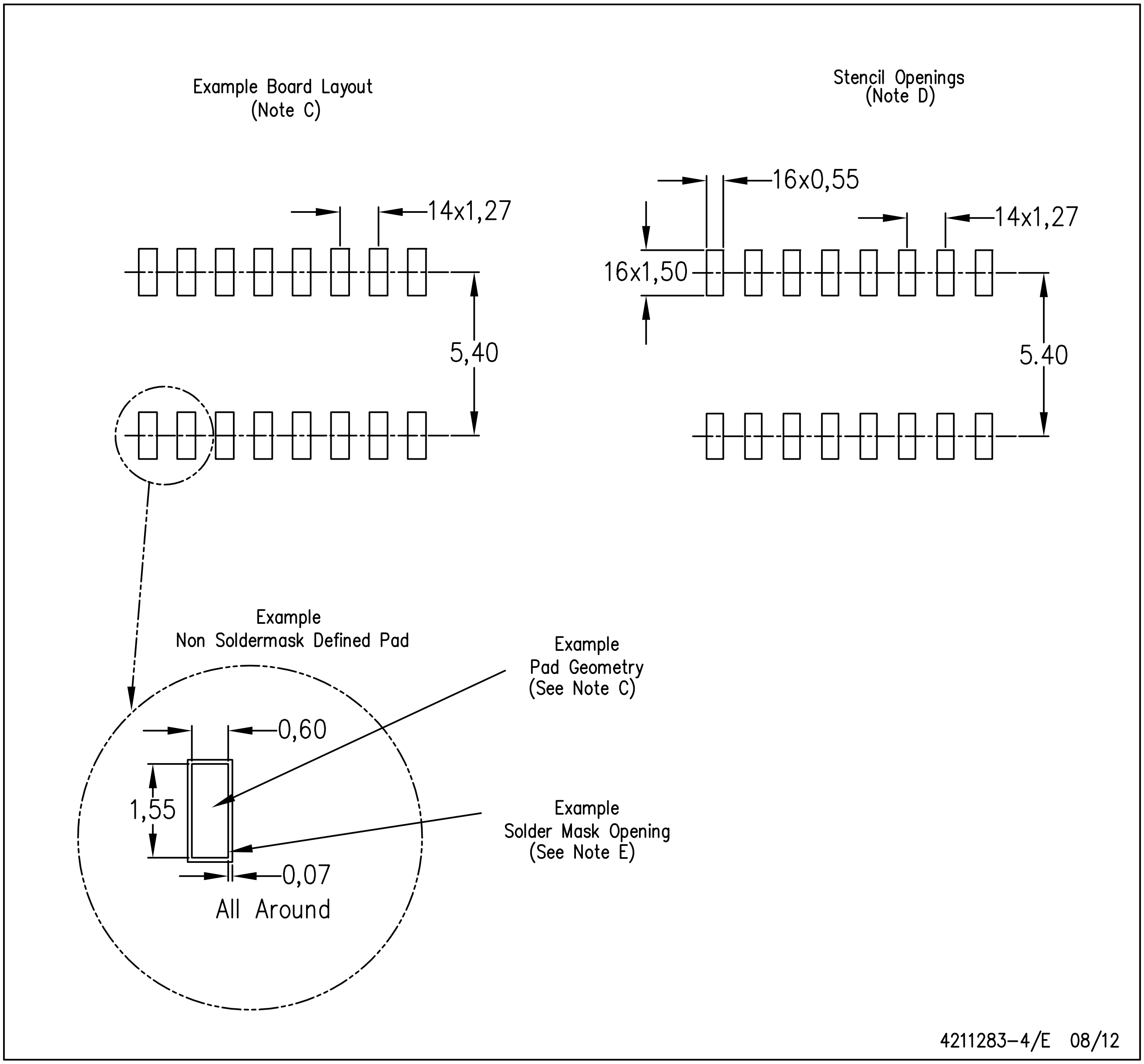
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



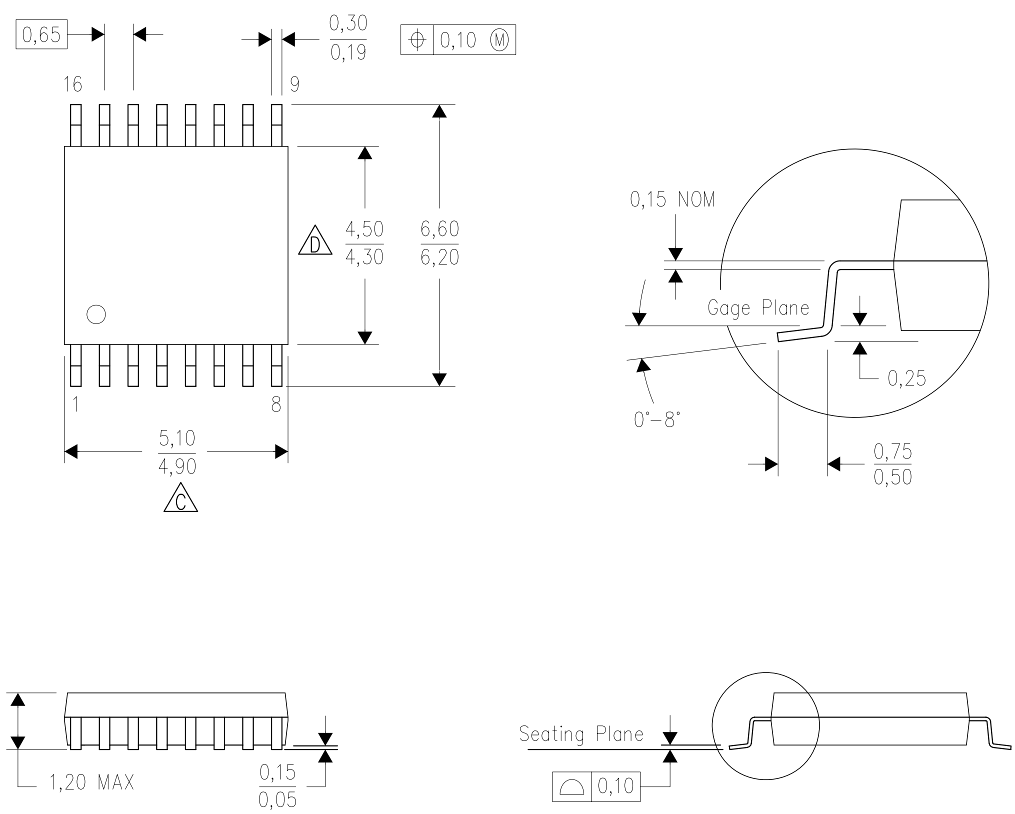
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

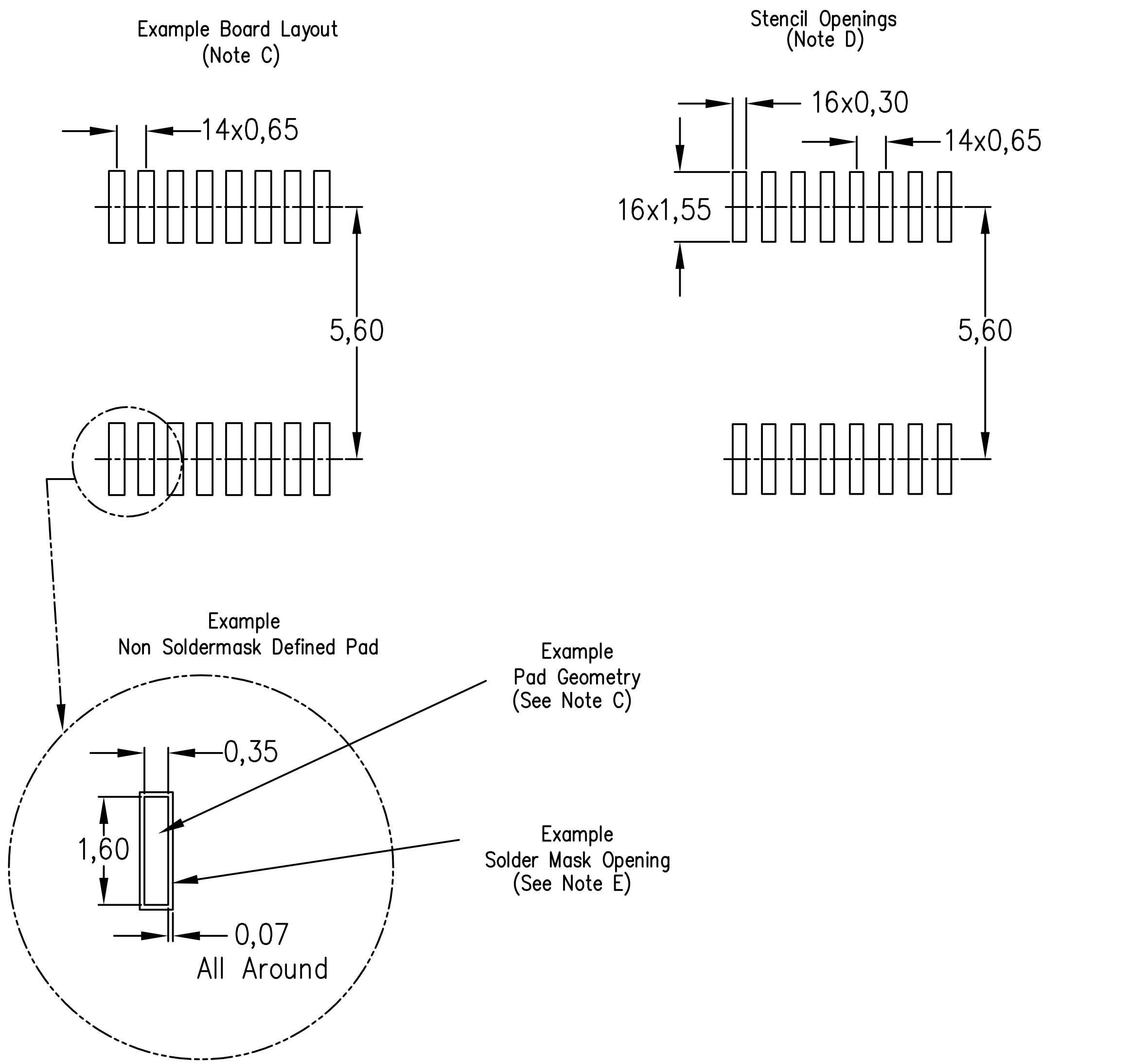
PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE

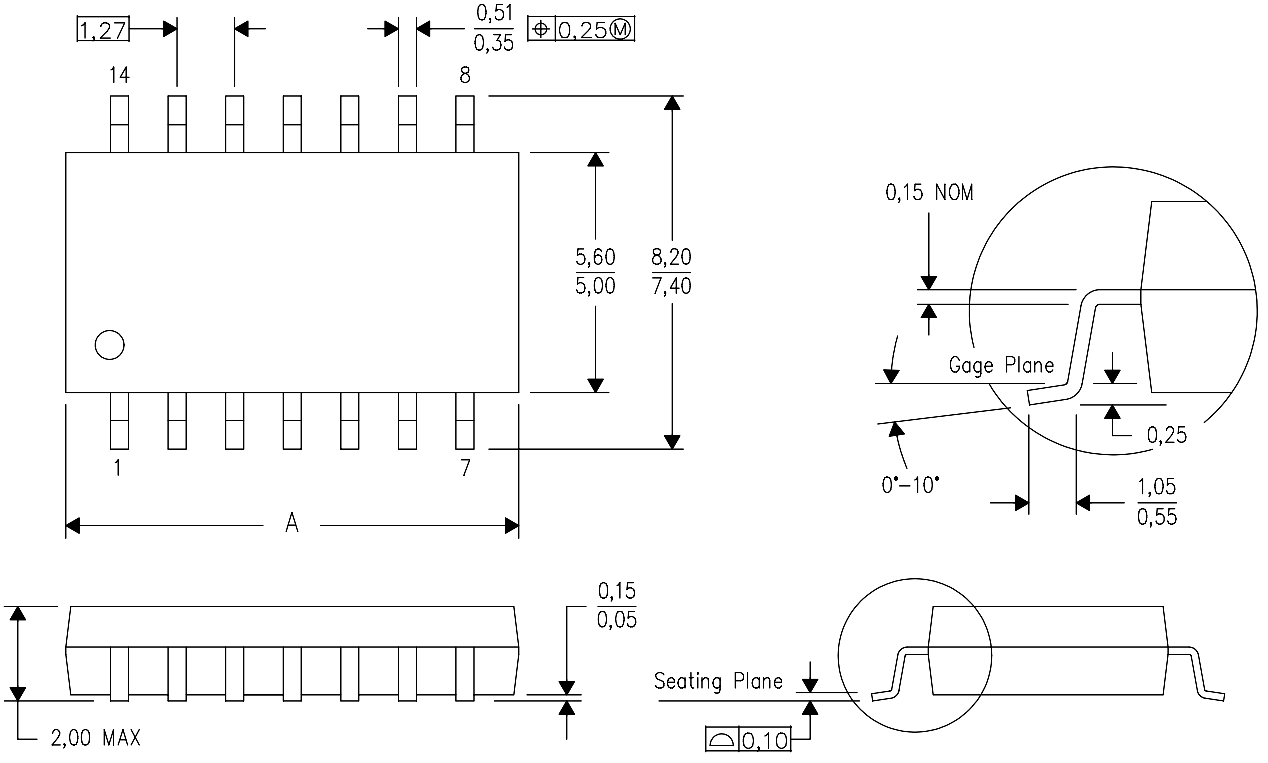


4211284-3/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.