TPS6109x Synchronous Boost Converter With 2-A Switch

1 Features

- Synchronous (96% Efficient) Boost Converter With 500-mA Output Current From 1.8-V Input
- Available in a 16-Pin VQFN 4 x 4 Package
- Device Quiescent Current: 20 µA (Typ)
- Input Voltage Range: 1.8 V to 5.5 V
- Adjustable Output Voltage Up to 5.5 V Fixed Output Voltage Options
- Power Save Mode for Improved Efficiency at Low Output Power
- Low Battery Comparator
- Low EMI-Converter (Integrated Antiringing Switch)
- Load Disconnect During Shutdown
- Over-Temperature Protection

2 Applications

- All Single Cell Li or Dual Cell Battery or USB Powered Operated Products
  - MP3 Player
  - PDAs
  - Other Portable Equipment

3 Description

The TPS6109x devices provide a power supply solution for products powered by either a one-cell Li-Ion or Li-Polymer, or a two-cell alkaline, NiCd or NiMH battery and required supply currents up to or higher than 1 A. The converter generates a stable output voltage that is either adjusted by an external resistor divider or fixed internally on the chip. It provides high efficient power conversion and is capable of delivering output currents up to 0.5 A at 5 V at a supply voltage down to 1.8 V. The implemented boost converter is based on a fixed frequency, pulse-width- modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency. Boost switch and rectifier switch are connected internally to provide the lowest leakage inductance and best EMI behavior possible. The maximum peak current in the boost switch is limited to a value of 2500 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and, in effect, lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode.

The output voltage can be programmed by an external resistor divider or is fixed internally on the chip.

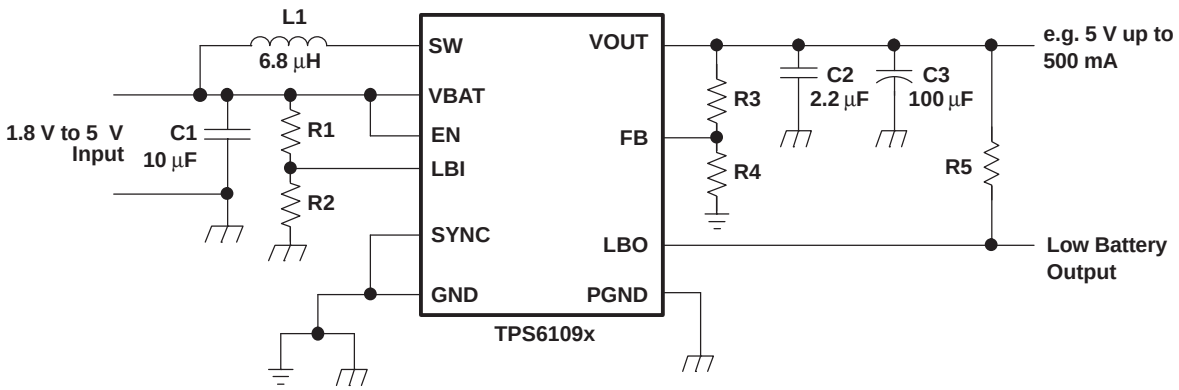
The device is packaged in a 16-pin VQFN 4-mm x 4-mm (16 RSA) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61090	VQFN (10)	4.00 mm × 4.00 mm
TPS61091		
TPS61092		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Schematic



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4 Revision History

Changes from Revision B (April 2005) to Revision C **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

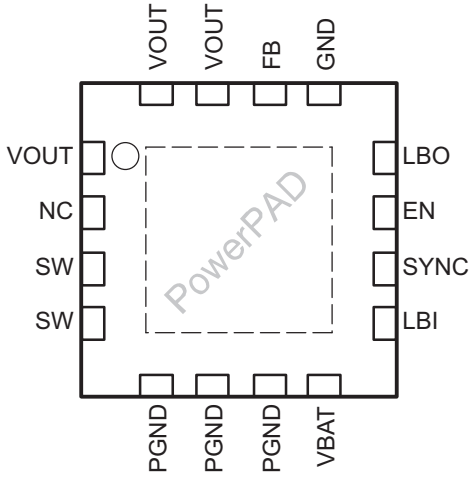
5 Device Comparison Table

T_A	OUTPUT VOLTAGE DC-DC(1)	PACKAGE	PART NUMBER(2)
40°C to 85°C	Adjustable	16-pin VQFN 4 mm × 4 mm	TPS61090RSA
	3.3 V	16-pin VQFN 4 mm × 4 mm	TPS61091RSA
	5 V	16-pin VQFN 4 mm × 4 mm	TPS61092RSA

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) See *Mechanical, Packaging, and Orderable Information* for ordering information and tape and reel options.

6 Pin Configuration and Functions

RSA Package
10 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	11	I	Enable input. (1/VBAT enabled, 0/GND disabled)
FB	14	I	Voltage feedback of adjustable versions
GND	13	I/O	Control/logic ground
LBI	9	I	Low battery comparator input (comparator enabled with EN)
LBO	12	O	Low battery comparator output (open drain)
NC	2		Not connected
PGND	5, 6, 7	I/O	Power ground
PowerPAD™	—	—	Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.
SYNC	10	I	Enable/disable power save mode (1: VBAT disabled, 0: GND enabled, clock signal for synchronization)
SW	3, 4	I	Boost and rectifying switch input
VBAT	8	I	Supply voltage
VOUT	1, 15, 16	O	DC-DC output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Input voltage on LBI	–0.3	3.6	V
	Input voltage on SW, VOUT, LBO, VBAT, SYNC, EN, FB	–0.3	7	V
T_A	Operating free air temperature	–40	85	°C
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Supply voltage at VBAT	1.8		5.5	V
L	Inductance	2.2	6.8		µH
C_i	Input, capacitance		10		µF
C_o	Output capacitance	22	100		
T_A	Operating free air temperature	–40		85	°C
T_J	Operating virtual junction temperature	–40		125	

7.4 Electrical Characteristics

over recommended free-air temperature range and over recommended input voltage range (typical values are at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE						
V_I	Input voltage range		1.8		5.5	V
V_O	TPS61090 output voltage range		1.8		5.5	
V_{FB}	TPS61090 feedback voltage		490	500	510	mV
f	Oscillator frequency		500	600	700	kHz
	Frequency range for synchronization		500		700	
I_{SW}	Switch current limit	VOUT= 5 V	2000	2200	2500	mA
	Start-up current limit			0.4 x I_{SW}		
	Boost switch on resistance	VOUT= 5 V		55		mΩ
	Rectifying switch on resistance	VOUT= 5 V		55		
	Total accuracy		–3%		3%	
	Line regulation				0.6%	
	Load regulation				0.6%	

Electrical Characteristics (continued)

over recommended free-air temperature range and over recommended input voltage range (typical values are at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Quiescent current	into VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT =5 V		10	25	µA
		into VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 5 V		10	20	
	Shutdown current		V_{EN}= 0 V, VBAT = 2.4 V		0.1	1	
CONTROL STAGE							
V_{UVLO}	Under voltage lockout threshold		V_{LBI} voltage decreasing		1.5		V
V_{IL}	LBI voltage threshold		V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis				10		
	LBI input current		EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage		V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current				100		µA
	LBO output leakage current		V_{LBO} = 7 V		0.01	0.1	
V_{IL}	EN, SYNC input low voltage					0.2 × VBAT	V
V_{IH}	EN, SYNC input high voltage			0.8 × VBAT			
	EN, SYNC input current		Clamped on GND or VBAT		0.01	0.1	µA
	Overtemperature protection				140		°C

7.5 Typical Characteristics

Table 1. Table of Graphs

DC-DC Converter		Figure
Maximum output current	vs Input voltage	Figure 1, Figure 2
Efficiency	vs Output current (TPS61090) (V_O = 2.5 V, V_I = 1.8 V, VSYNC = 0 V)	Figure 3
	vs Output current (TPS61091) (V_O = 3.3 V, V_I = 1.8 V, 2.4 V, VSYNC = 0 V)	Figure 4
	vs Output current (TPS61092) (V_O = 5.0 V, V_I = 2.4 V, 3.3 V, VSYNC = 0 V)	Figure 5
	vs Output current (TPS61091) (I_O = 10 mA, 100 mA, 500 mA, VSYNC = 0 V)	Figure 6
	vs Output current (TPS61092) (I_O = 10 mA, 100 mA, 500 mA, VSYNC = 0 V)	Figure 7
Output voltage	vs Output current (TPS61091) (V_I = 2.4 V)	Figure 8
	vs Output current (TPS61092) (V_I = 3.3 V)	Figure 9
No-load supply current into VBAT	Voltage (TPS61092)	Figure 10
No-load supply current into VOUT	vs Input voltage (TPS61092)	Figure 11
Minimum Load Resistance at Start-Up	vs Input Voltage (TPS61092) (V_I = 3.3 V)	Figure 12

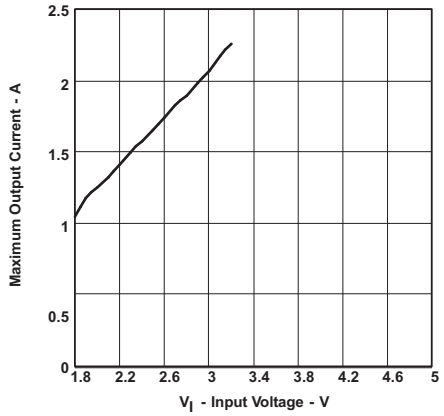


Figure 1. TPS61091 Maximum Output Current vs Input Voltage

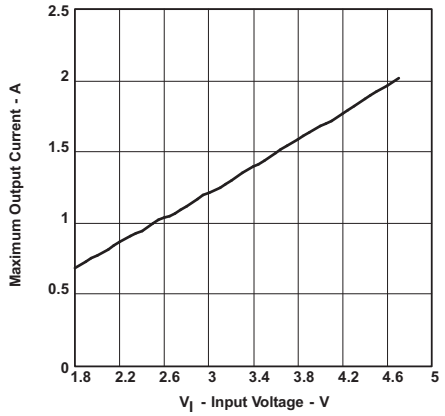


Figure 2. TPS61092 Maximum Output Current vs Input Voltage

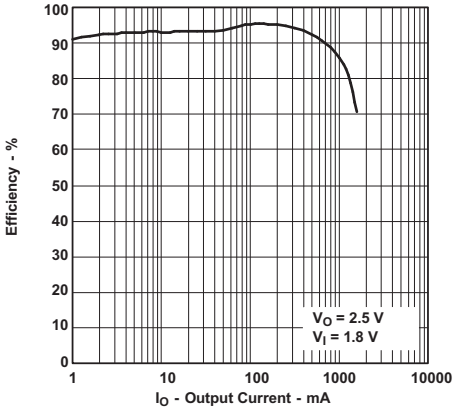


Figure 3. TPS61090 Efficiency vs Output Current

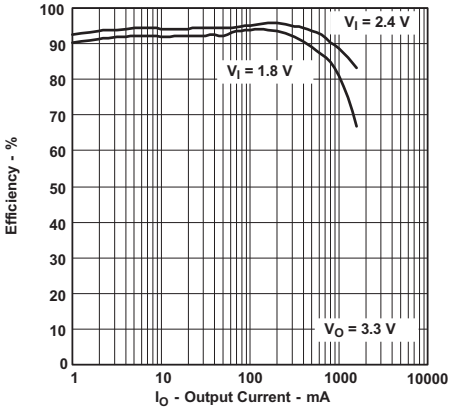


Figure 4. TPS61091 Efficiency vs Output Current

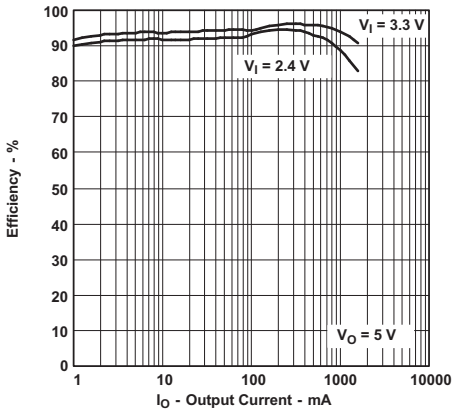


Figure 5. TPS61092 Efficiency vs Output Current

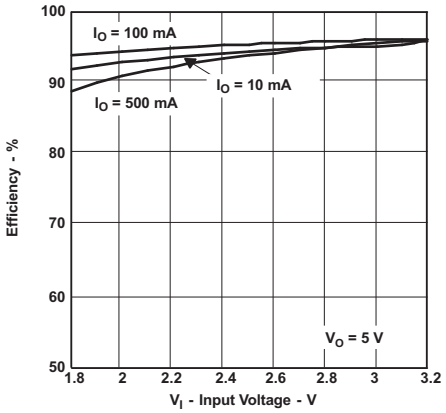


Figure 6. TPS61091 Efficiency vs Output Current

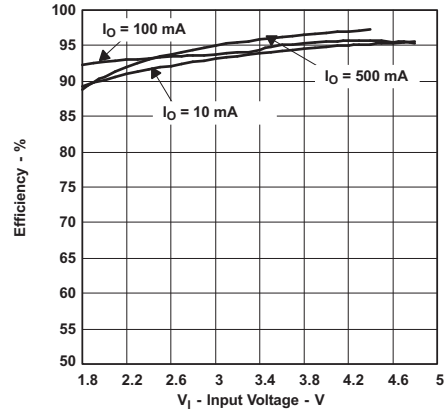


Figure 7. TPS61092 Efficiency vs Output Current

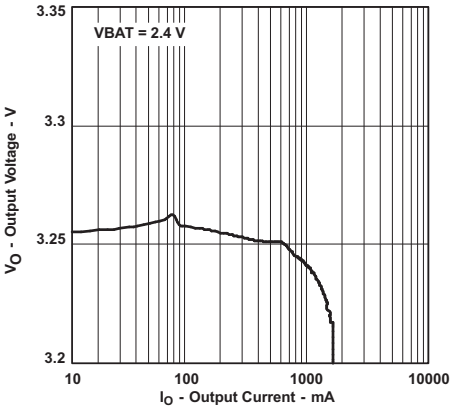


Figure 8. TPS61091 Efficiency vs Output Current

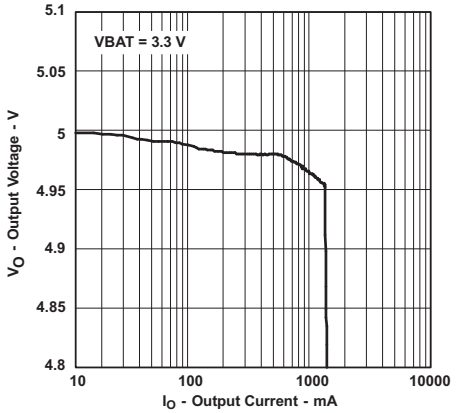


Figure 9. TPS61092 Output Voltage vs Output Current

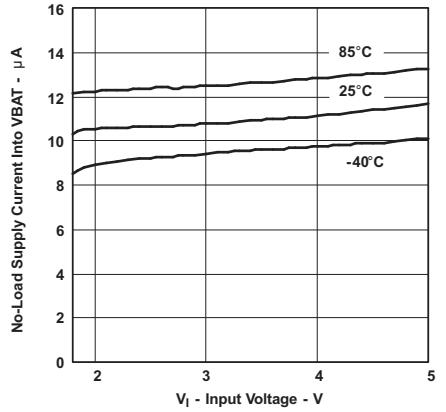


Figure 10. TPS61092 No-Load Supply Current Into VBAT Voltage

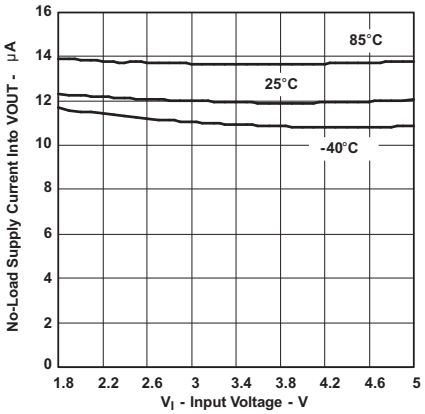


Figure 11. TPS61092 No-Load Supply Current Into VOUT vs Input Voltage

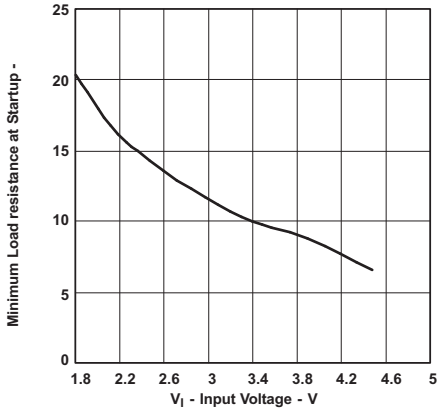


Figure 12. Minimum Load Resistance at Start-Up vs Input Voltage

8 Parameter Measurement Information

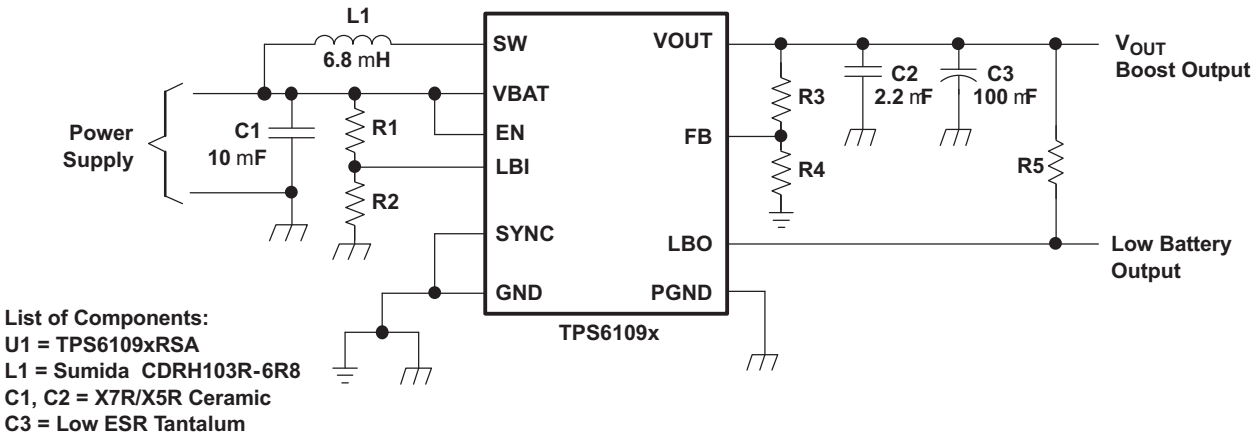


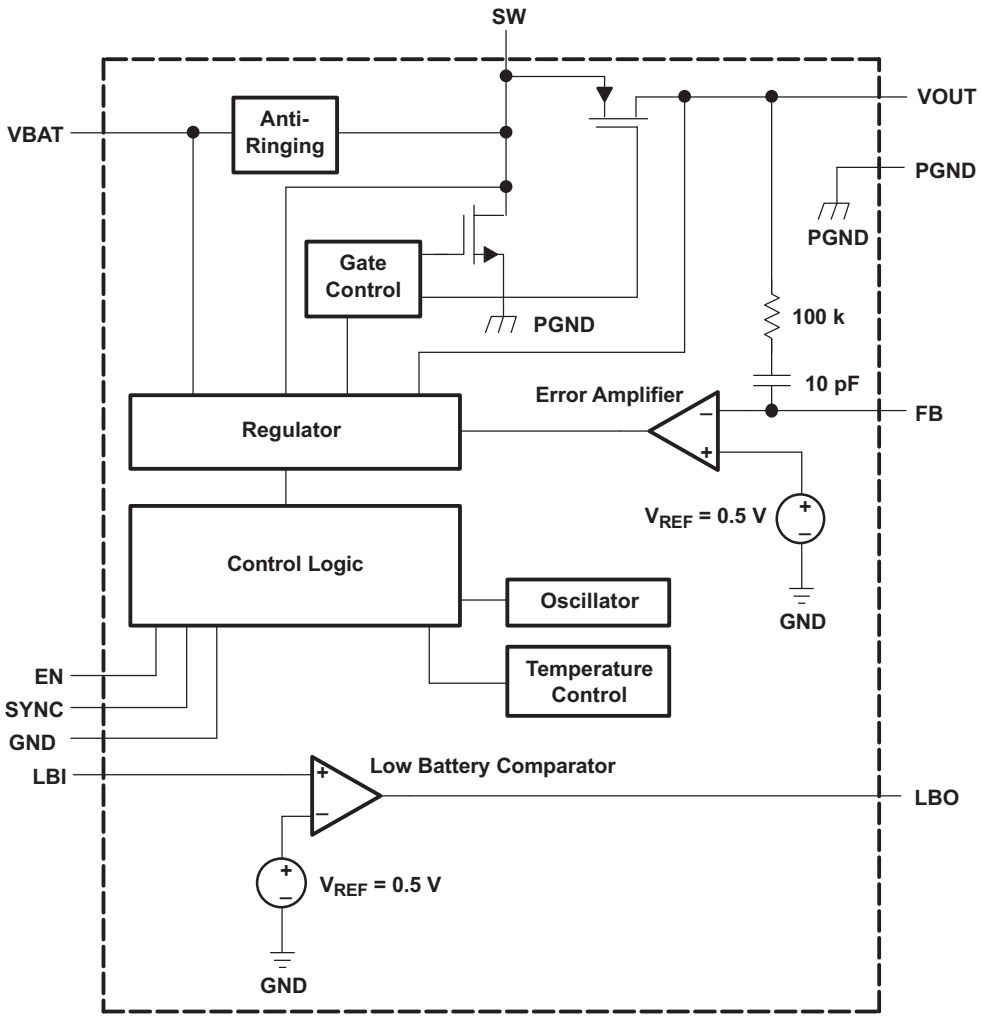
Figure 13. Parameter Schematic

9 Detailed Description

9.1 Overview

The TPS6109x synchronous step-up converter typically operates at a 600-kHz frequency pulse width modulation (PWM) at moderate to heavy load currents. The converter enters power save mode at low load currents to maintain a high efficiency over a wide load. The power save mode can also be disabled, forcing the converter to operate at a fixed switching frequency. The TPS6109x family is based on a fixed frequency with multiple feed forward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. It can also operate synchronized to an external clock signal that is applied to the SYNC pin. Additionally, TPS6109x integrated the low-battery detector circuit typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 96%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device however uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

9.3.2 Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 2200 mA.

An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

9.3.3 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

9.3.4 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than typically 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

9.3.5 Softstart

When the device enables the internal startup cycle starts with the first step, the precharge phase. During precharge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch current is limited in that phase. This also limits the output current under short-circuit conditions at the output. After charging the output capacitor to the input voltage the device starts switching. Until the output voltage is reached, the boost switch current limit is set to 40% of its nominal value to avoid high peak currents at the battery during startup. When the output voltage is reached, the regulator takes control and the switch current limit is set back to 100%.

Feature Description (continued)

9.3.6 Power Save Mode and Synchronization

The SYNC pin can be used to select different operation modes. To enable power save, SYNC must be set low. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SYNC to VBAT.

Applying an external clock with a duty cycle between 30% and 70% at the SYNC pin forces the converter to operate at the applied clock frequency. The external frequency has to be in the range of about ±20% of the nominal internal frequency. Detailed values are shown in the electrical characteristic section of the data sheet.

9.3.7 Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

9.3.8 Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

9.4 Device Functional Modes

Table 2. TPS61090 Operation Mode

MODE	DESCRIPTION	CONDITION
PWM	Boost in normal switching operation	SYNC pin is high, across whole load SYNC pin is low, medium to heavy load.
PFM	Boost in power save operation	SYNC pin is low, light load.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The devices are designed to operate from an input voltage supply range between 1.8 V and 5.5 V with a maximum switch current limit up to 2500 mA. The SYNC pin can be used to select different operation modes. To enable power save, SYNC must be set low. The devices operate in PWM mode from the medium to heavy load conditions and in power save mode at light load condition. In PWM mode, the TPS6109x converter operates with the nominal switching frequency of 600 kHz. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. The power save mode can be disabled by setting the SYNC to VBAT, TPS6109x converter always operates with the nominal switching frequency of 600 kHz across the whole load range. Applying an external clock with a duty cycle at the SYNC pin forces the converter to operate at the applied clock frequency.

10.2 Typical Applications

10.2.1 Typical Application Circuit for Adjustable Output Voltage Option

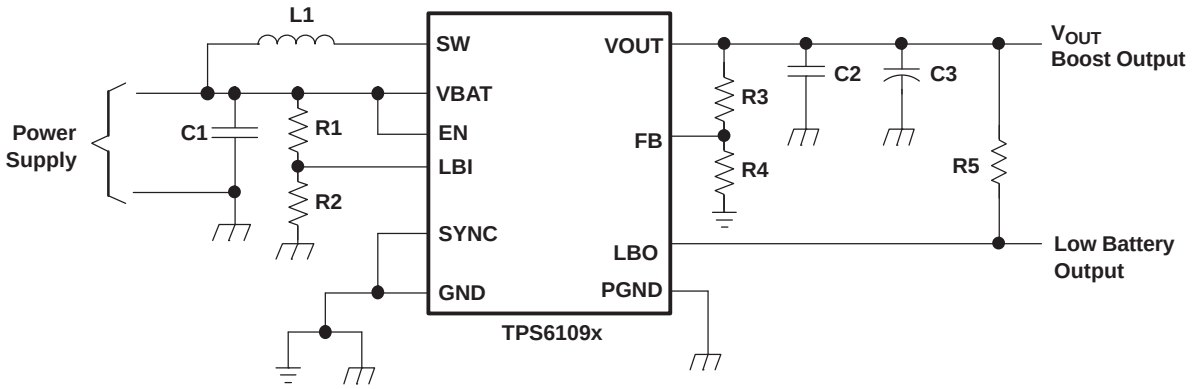


Figure 14. Typical Application Circuit for Adjustable Output Voltage Option Schematic

10.2.1.1 Design Requirements

Table 3. TPS6109x 5 V Output Design Parameters

DESIGN PARAMETERS	TYPICAL VALUES
Input Voltage Range	1.8 V to 5.0 V
Output Voltage	5.0 V
Output Voltage Ripple	±3% VOUT
Transient Response	±10% VOUT
Input Voltage Ripple	±200 mV
Output Current Rating	500 mA
Operating Frequency	600 kHz

10.2.1.2 Detailed Design Procedure

The TPS6109x DC-DC converters are intended for systems powered by a dual or triple cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li-Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6109x is used.

10.2.1.2.1 Programming the Output Voltage

The output voltage of the TPS61090 DC-DC converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across R4 is typically 500 mV. Based on those two values, the recommended value for R4 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using Equation 1:

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 200\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (1)$$

If as an example, an output voltage of 5.0 V is needed, a 1.8-MΩ resistor should be chosen for R3. If for any reason the value for R4 is chosen significantly lower than 200 kΩ additional capacitance in parallel to R3 is recommended. The required capacitance value can be easily calculated using Equation 2

$$C_{parR3} = 10\ pF \times \left(\frac{200\ k\Omega}{R4} - 1\right) \quad (2)$$

10.2.1.2.2 Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 µA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using Equation 3.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1\right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1\right) \quad (3)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the DC-DC converter. If not used, the LBO pin can be left floating or tied to GND.

10.2.1.2.3 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6109x's switch is 2500 mA at an output voltage of 5 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 4:

$$I_L = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (4)$$

For example, for an output current of 500 mA at 5 V, at least 1750 mA of average current flows through the inductor at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using Equation 5:

$$L = \frac{V_{BAT} \times \left(V_{OUT} - V_{BAT}\right)}{\Delta I_L \times f \times V_{OUT}} \quad (5)$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 20% × I_L. In this example, the desired inductor has the value of 5.5 µH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 4. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been used with the TPS6109x converters:

Table 4. List of Inductors

VENDOR	INDUCTOR SERIES
Sumida	CDRH6D28
	CDRH6D38
	CDRH103R
Wurth Elektronik	WE-PD type L
	WE-PD type XL
EPCOS	B82464G

10.2.1.2.4 Capacitor Selection

10.2.1.2.4.1 Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

10.2.1.2.4.2 Output Capacitor DC-DC Converter

The major parameter necessary to define the minimum value of the output capacitor is the maximum allowed output voltage ripple in steady state operation of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using equation Equation 6:

$$C_{min} = \frac{I_{OUT} \times \left(V_{OUT} - V_{BAT}\right)}{f \times \Delta V \times V_{OUT}} \quad (6)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10 mV, a minimum capacitance of 53 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

An additional ripple of 40 mV is the result of using a tantalum capacitor with a low ESR of 80 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 50 mV. Additional ripple is caused by load transients. This means that the output capacitance needs to be larger than calculated above to meet the total ripple requirements. The output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 53 µF and load transient considerations, a reasonable output capacitance value is in a 100 µF range. For economical reasons this usually is a tantalum capacitor. Because of this the control loop has been optimized for using output capacitors with an ESR of above 30 mΩ.

10.2.1.2.4.3 Small Signal Stability

When using output capacitors with lower ESR, like ceramics, it is recommended to use the adjustable voltage version. The missing ESR can be easily compensated there in the feedback divider. Typically a capacitor in the range of 10 pF in parallel to R3 helps to obtain small signal stability with lowest ESR output capacitors. For more detailed analysis the small signal transfer function of the error amplifier and regulator, which is given is Equation 8, can be used.

$$A_{REG} = \frac{d}{V_{FB}} \qquad A_{REG} = \frac{d5(R3 + R4)}{R4 \times (1 + i \times \omega \times 2.3\ \mu s)} \tag{8}$$

10.2.1.3 Application Curves

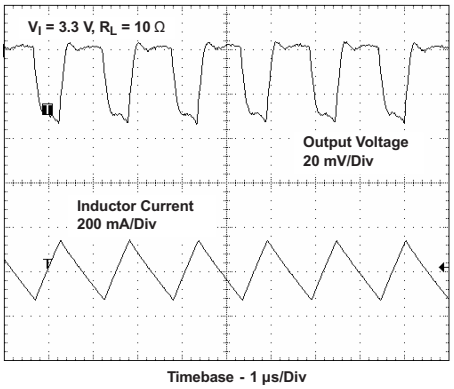


Figure 15. Output Voltage in Continuous Mode

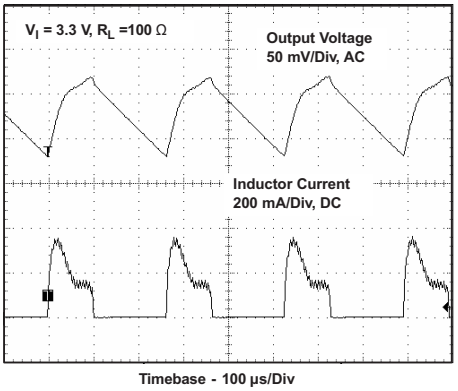


Figure 16. Output Voltage in Power Save Mode

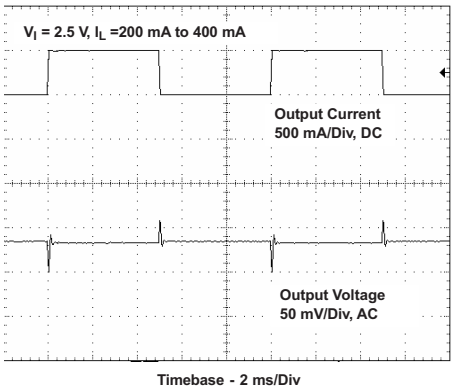


Figure 17. Load Transient Response

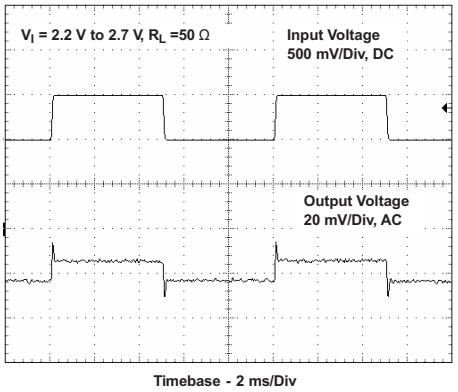


Figure 18. Line Transient Response

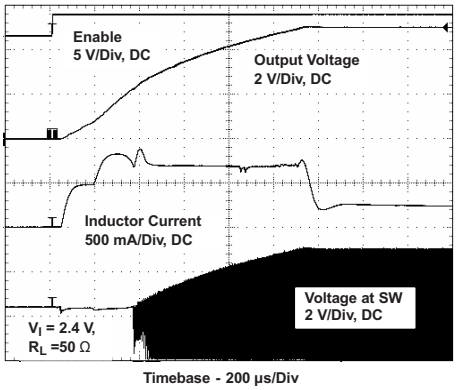
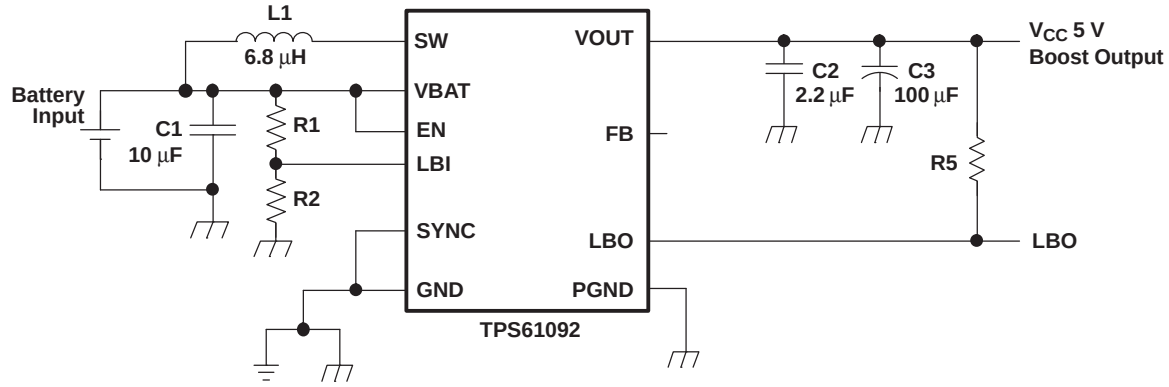


Figure 19. DC-DC Converter Start-Up After Enable

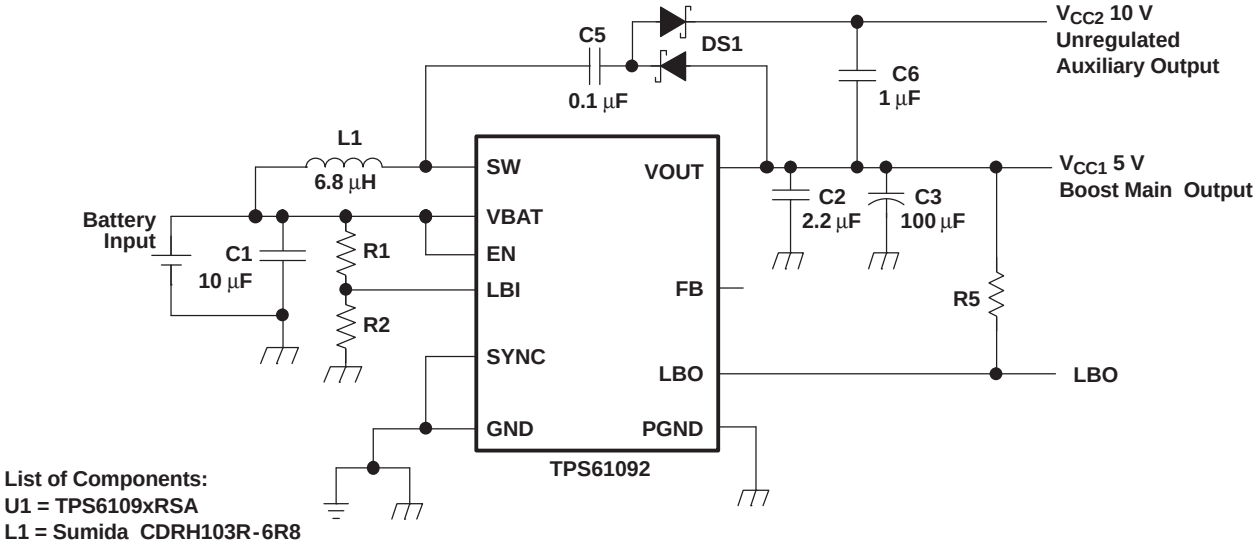
10.2.2 TPS6109x Application Schematic of 5 V_{out} With Maximum Output Power



List of Components:
U1 = TPS6109xRSA
L1 = Sumida CDRH103R-6R8
C1, C2 = X7R,X5R Ceramic
C3 = Low ESR Tantalum

Figure 20. Power Supply Solution for Maximum Output Power Schematic

10.2.3 TPS6109x Application Schematic of 5 V_{out} and Auxiliary 10 V_{out} With Charge Pump



List of Components:
U1 = TPS6109xRSA
L1 = Sumida CDRH103R-6R8
C1, C2, C5, C6, = X7R,X5R Ceramic
C3 = Low ESR Tantalum
DS1 = BAT54S

Figure 21. Power Supply Solution With Auxiliary Positive Output Voltage Schematic

10.2.4 TPS6109x Application Schematic of 5 V_{out} and Auxiliary -5 V_{out} With Charge Pump

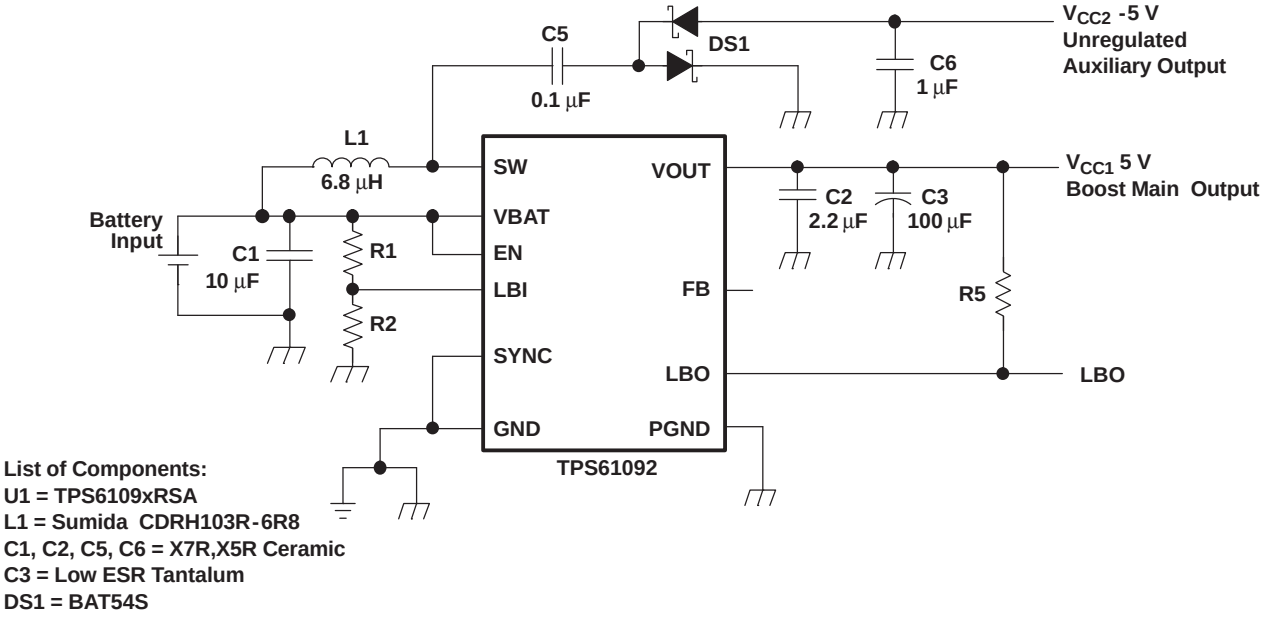


Figure 22. Power Supply Solution With Auxiliary Negative Output Voltage Schematic

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

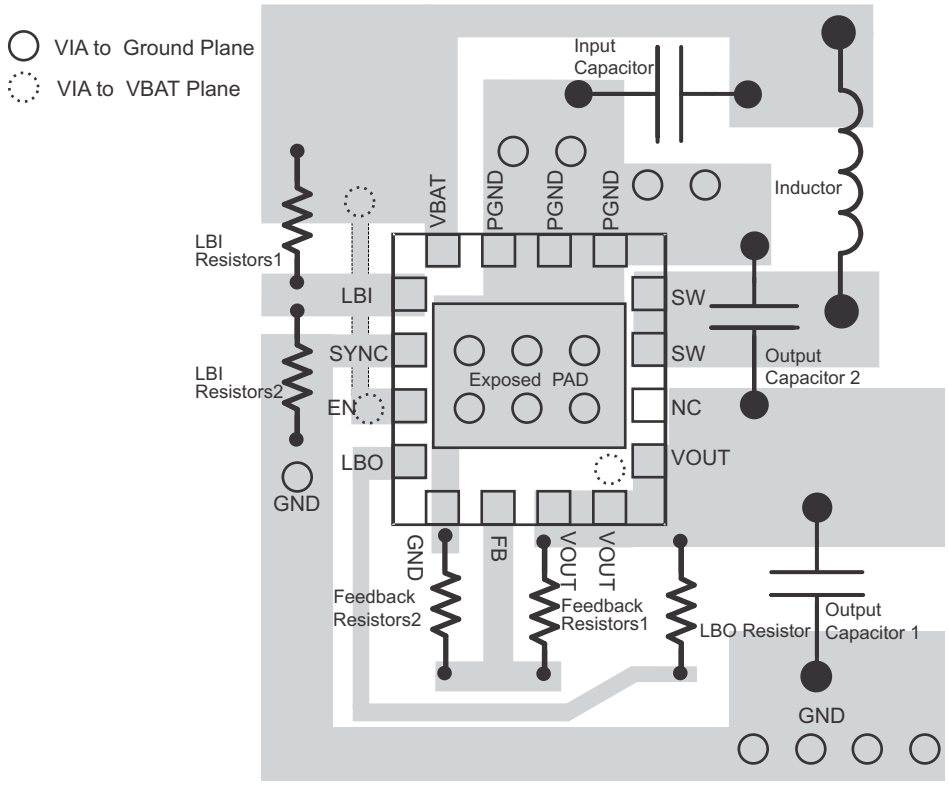


Figure 23. Layout Example Schematic

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the TPS6109x devices is 150°C. The thermal resistance of the 16-pin QFN PowerPAD package (RSA) is$R_{\Theta JA}$ = 38.1 °C/W, if the PowerPAD is soldered and the board layout is optimized. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 1700 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{150°C - 85°C}{38.1\ k/W} = 1700\ mW \quad (9)$$

If designing for a lower junction temperature of 125°C, which is recommended, maximum heat dissipation is lower. Using the above equation (8) results in 1050 mW power dissipation.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61090	Click here	Click here	Click here	Click here	Click here
TPS61091	Click here	Click here	Click here	Click here	Click here
TPS61092	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

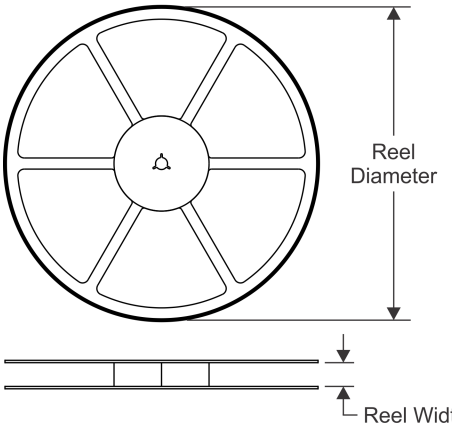
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

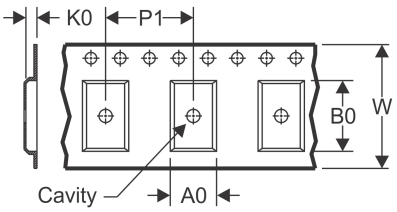
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

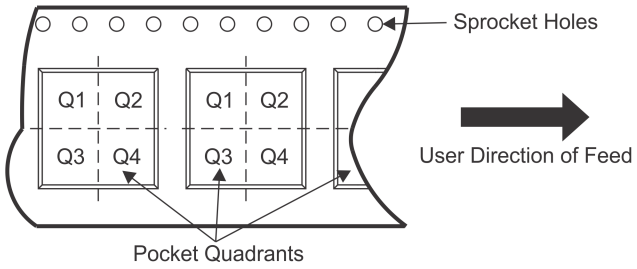


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

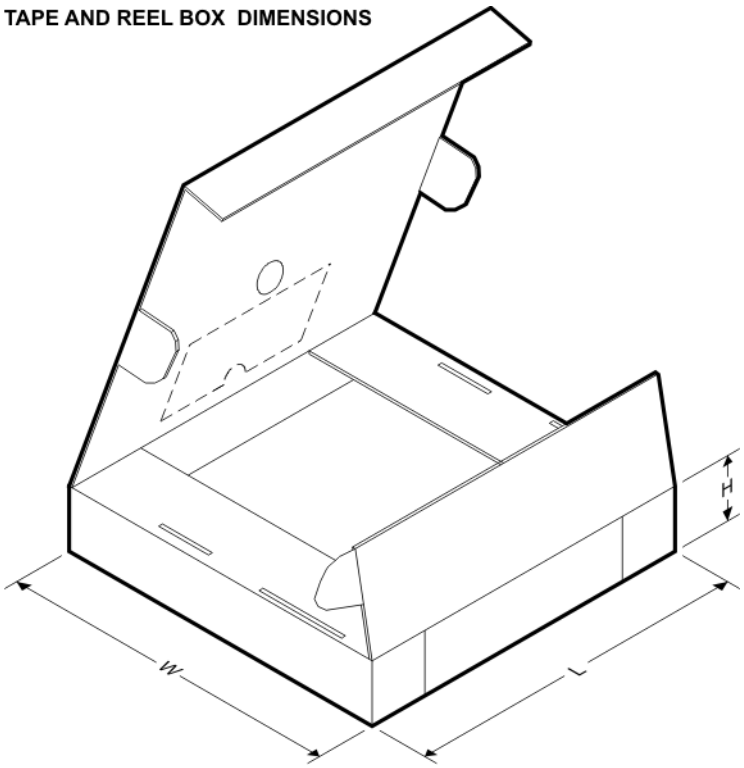
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61090RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS61091RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS61092RSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

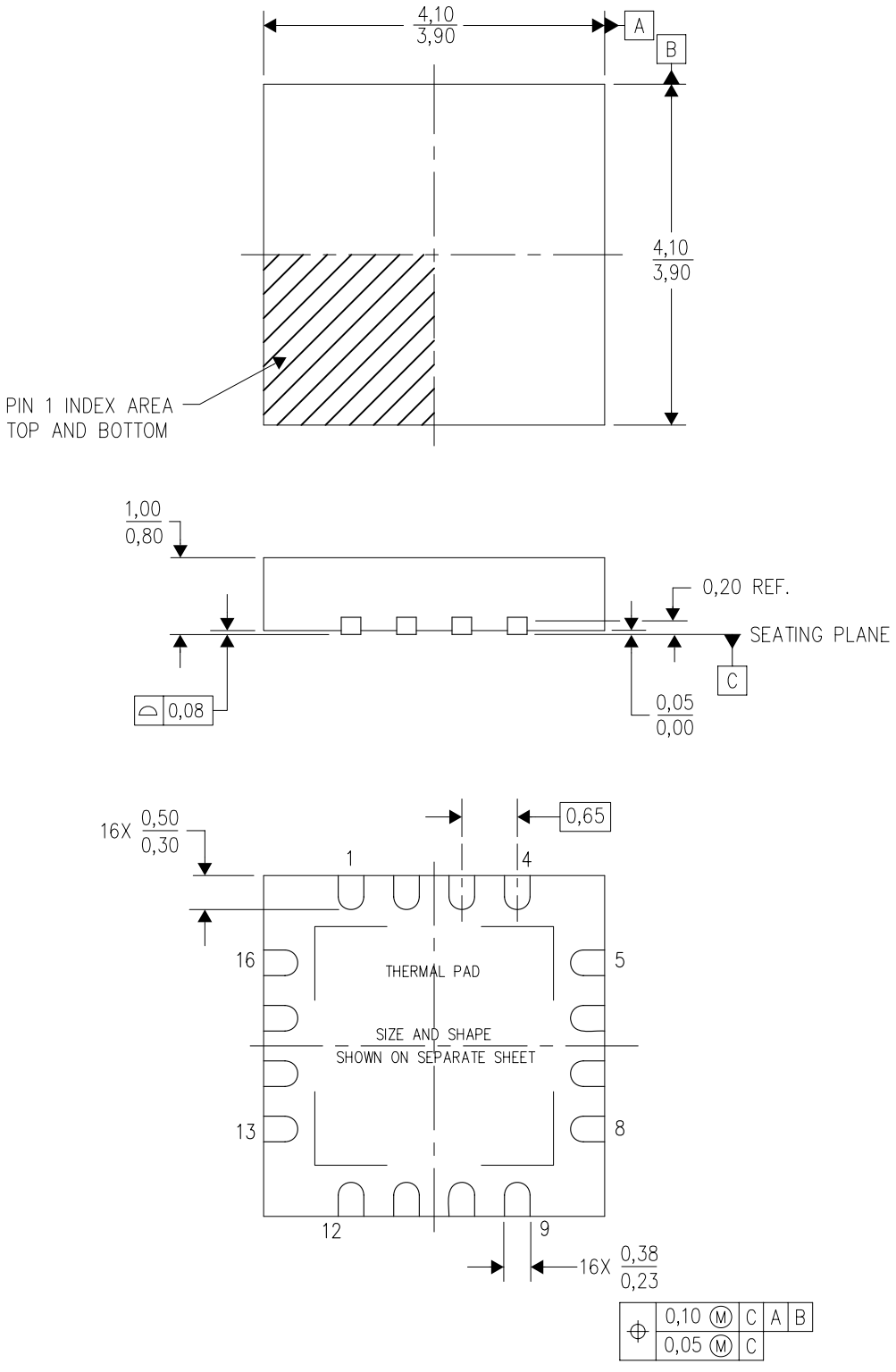
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61090RSAR	QFN	RSA	16	3000	336.6	336.6	28.6
TPS61091RSAR	QFN	RSA	16	3000	336.6	336.6	28.6
TPS61092RSAR	QFN	RSA	16	3000	336.6	336.6	28.6

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

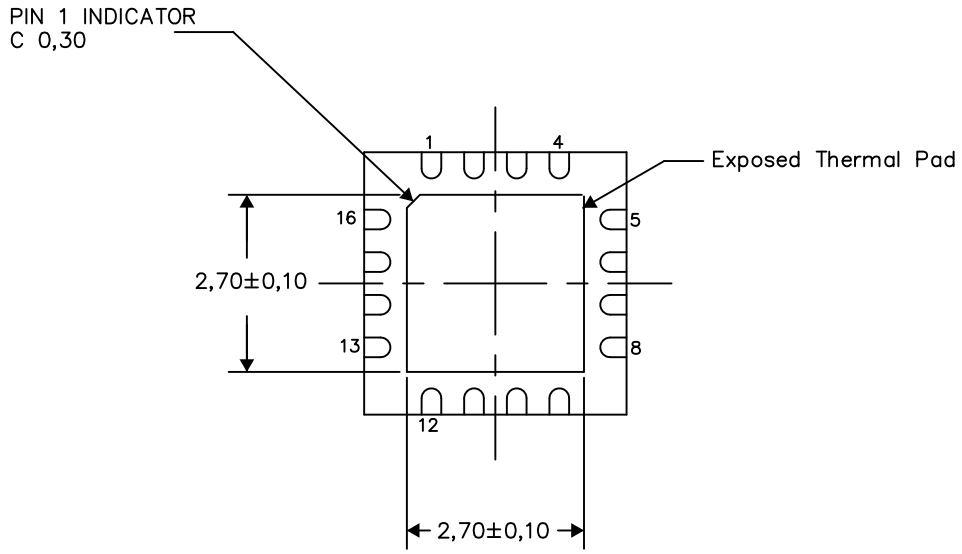
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



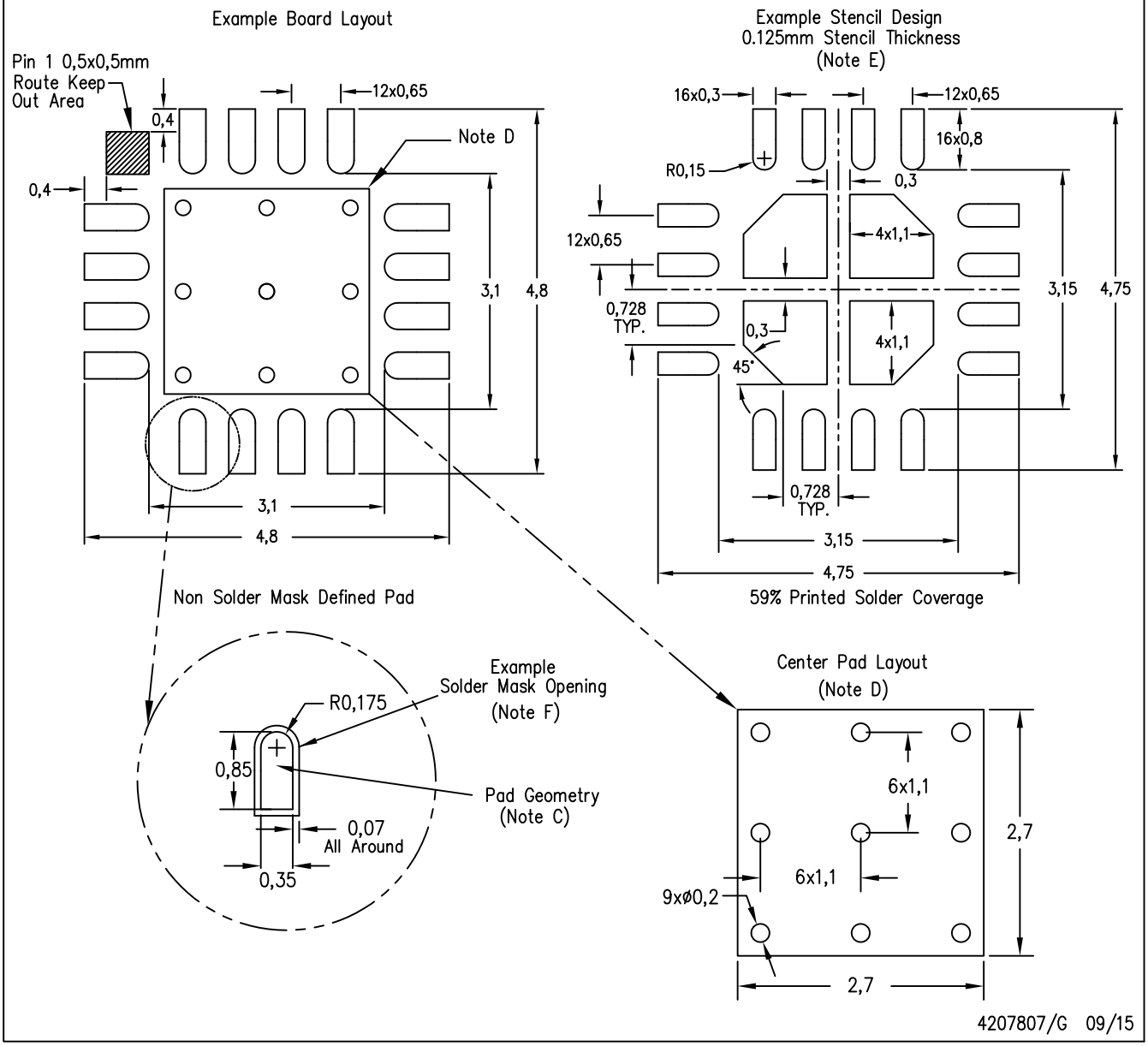
Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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