

LM397 Single General-Purpose Voltage Comparator

1 Features

- $T_A = 25^\circ\text{C}$. Typical Values Unless Otherwise Specified.
- 5-Pin SOT-23 Package
- Industrial Operating Range -40°C to $+85^\circ\text{C}$
- Single or Dual Power Supplies
- Wide Supply Voltage Range 5 V to 30 V
- Low Supply Current 300 μA
- Low Input Bias Current 7 nA
- Low Input Offset Current ± 1 nA
- Low Input Offset Voltage ± 2 mV
- Response Time 440 ns (50-mV Overdrive)
- Input Common-Mode Voltage 0 to $V_S - 1.5$ V

2 Applications

- A/D Converters
- Pulse, Square-Wave Generators
- Peak Detector
- Industrial Applications

3 Description

The LM397 device is a single voltage comparator with an input common mode that includes ground. The LM397 is designed to operate from a single 5-V to 30-V power supply or a split power supply. Its low supply current is virtually independent of the magnitude of the supply voltage.

The LM397 features an open-collector output stage. This allows the connection of an external resistor at the output. The output can directly interface with TTL, CMOS and other logic levels, by tying the resistor to different voltage levels (level translator).

The LM397 is available in the space-saving 5-Pin SOT-23 package and is pin-compatible to TI's TL331, a single differential comparator.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM397	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit

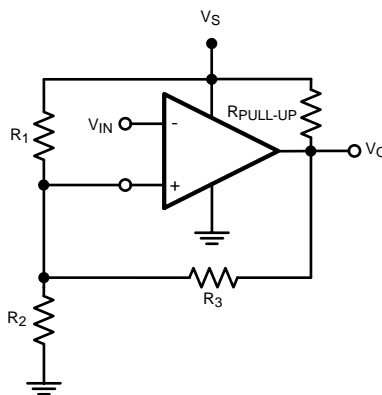


Table of Contents

1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Pin Configuration and Functions 3 6 Specifications 4 6.1 Absolute Maximum Ratings 4 6.2 ESD Ratings..... 4 6.3 Recommended Operating Conditions 4 6.4 Thermal Information 4 6.5 Electrical Characteristics..... 5 6.6 Typical Characteristics 6 7 Detailed Description 7 7.1 Overview 7 7.2 Functional Block Diagram 7	7.3 Feature Description..... 7 7.4 Device Functional Modes..... 8 8 Application and Implementation 9 8.1 Application Information..... 9 8.2 Typical Application 9 9 Power Supply Recommendations 11 10 Layout 11 10.1 Layout Guidelines 11 10.2 Layout Example 11 11 Device and Documentation Support 12 11.1 Community Resources..... 12 11.2 Trademarks 12 11.3 Electrostatic Discharge Caution..... 12 11.4 Glossary 12 12 Mechanical, Packaging, and Orderable Information 12
--	--

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2015) to Revision F	Page
---	-------------

- | | |
|--|----------|
| • Changed incorrect Pin Functions table entries. Pins 4 and 5 were swapped. | 3 |
|--|----------|

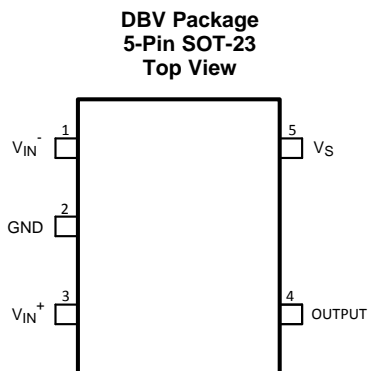
Changes from Revision D (March 2013) to Revision E	Page
---	-------------

- | | |
|---|----------|
| • Added <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. | 1 |
|---|----------|

Changes from Revision C (March 2013) to Revision D	Page
---	-------------

- | | |
|--|----------|
| • Changed layout of National Data Sheet to TI format | 8 |
|--|----------|

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	P	Ground
OUTPUT	4	O	Output
V_{IN+}	3	I	Noninverting Input
V_{IN-}	1	I	Inverting Input
V_S	5	P	Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{IN} differential		30	30	V
Supply voltages		±15	30	V
Voltage at input pins		-0.3	30	V
Junction temperature ⁽³⁾			150	°C
Soldering information	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	°C
Storage Temperature, T _{stg}		-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾⁽²⁾	±2000	V
	Machine Model ⁽¹⁾⁽²⁾	±200	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage, V _S		5	30	V
Temperature ⁽¹⁾		-40	85	°C

- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM397	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾	186	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	92.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	38.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	5.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	38.4	°C/W

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} – T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

6.5 Electrical Characteristics

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V^- = 0\text{ V}$, $V_{\text{CM}} = V^+/2 = V_O$.

PARAMETER		TEST CONDITIONS		MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
V_{OS}	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$, $V_O = 1.4\text{ V}$, $V_{\text{CM}} = 0\text{ V}$	$T_A = 25^\circ\text{C}$	2	7	mV	
			At the temperature extremes		10		
I_{OS}	Input offset current	$V_O = 1.4\text{ V}$, $V_{\text{CM}} = 0\text{ V}$	$T_A = 25^\circ\text{C}$	1.6	50	nA	
			At the temperature extremes		250		
I_B	Input bias current	$V_O = 1.4\text{ V}$, $V_{\text{CM}} = 0\text{ V}$	$T_A = 25^\circ\text{C}$	10	250	nA	
			At the temperature extremes		400		
I_S	Supply current	$R_L = \text{open}$, $V_S = 5\text{ V}$		0.25	0.7	mA	
		$R_L = \text{open}$, $V_S = 30\text{ V}$		0.3	2		
I_O	Output sink current	$V_{\text{IN}^+} = 1\text{ V}$, $V_{\text{IN}^-} = 0\text{ V}$, $V_O = 1.5\text{ V}$		6	13	mA	
I_{LEAKAGE}	Output leakage current	$V_{\text{IN}^+} = 1\text{ V}$, $V_{\text{IN}^-} = 0\text{ V}$, $V_O = 5\text{ V}$			0.1	nA	
		$V_{\text{IN}^+} = 1\text{ V}$, $V_{\text{IN}^-} = 0\text{ V}$, $V_O = 30\text{ V}$			1	μA	
V_{OL}	Output voltage low	$I_O = -4\text{ mA}$, $V_{\text{IN}^+} = 0\text{ V}$, $V_{\text{IN}^-} = 1\text{ V}$	$T_A = 25^\circ\text{C}$	180	400	mV	
			At the temperature extremes		700		
V_{CM}	Common-mode input voltage range	$V_S = 5\text{ V to }30\text{ V}^{(3)}$	$T_A = 25^\circ\text{C}$	0	$V_S - 1.5$	V	
			At the temperature extremes	0	$V_S - 2$		
A_V	Voltage gain	$V_S = 15\text{ V}$, $V_O = 1.4\text{ V to }11.4\text{ V}$, $R_L > = 15\text{ k}\Omega$ connected to V_S		120		V/mV	
t_{PHL}	Propagation delay (high to low)	Input overdrive = 5 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$		900		ns	
			Input overdrive = 50 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$		250		
t_{PLH}	Propagation delay (low to high)	Input Overdrive = 5 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$		940		μs	
			Input overdrive = 50 mV $R_L = 5.1\text{ k}\Omega$ connected to 5 V, $C_L = 15\text{ pF}$		440		

(1) All limits are specified by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(3) The input common-mode voltage of either input should not be permitted to go below the negative rail by more than 0.3V. The upper end of the common-mode voltage range is $V_S - 1.5\text{ V}$ at 25°C .

LM397

SNOS977F –MAY 2001–REVISED MAY 2016

www.ti.com

6.6 Typical Characteristics

T_A = 25°C. Unless otherwise specified.

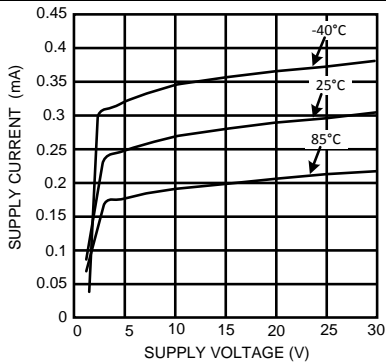


Figure 1. Supply Current vs Supply Voltage

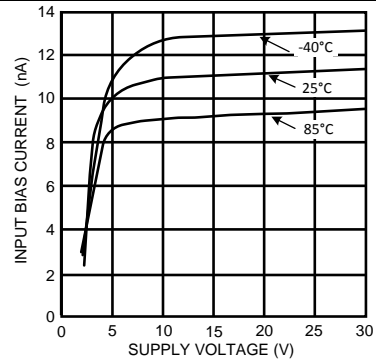


Figure 2. Input Bias Current vs Supply Current

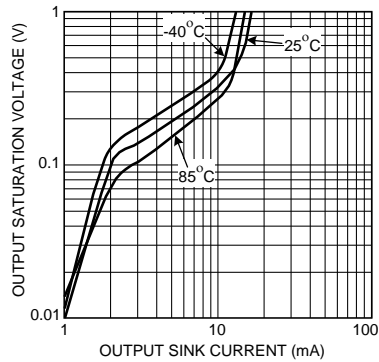


Figure 3. Output Saturation Voltage vs Output Sink Current

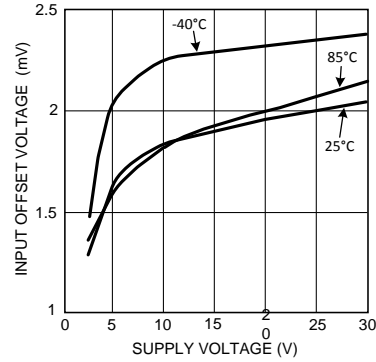


Figure 4. Input Offset Voltage vs Supply Voltage

7 Detailed Description

7.1 Overview

A comparator is often used to convert an analog signal to a digital signal. The comparator compares an input voltage (V_{IN}) at the noninverting pin to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF} the output (V_O) is low (V_{OL}). However, if V_{IN} is greater than V_{REF} , the output voltage (V_O) is high (V_{OH}). Refer to [Figure 6](#).

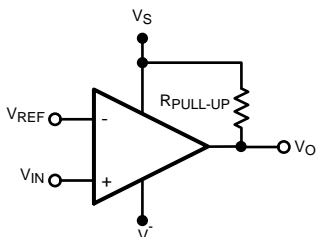


Figure 5. Basic Comparator

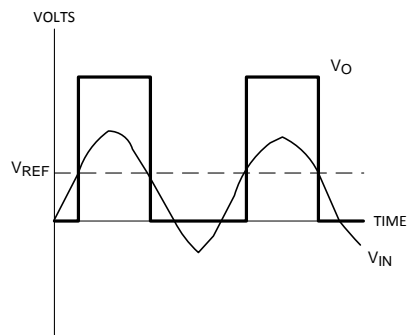
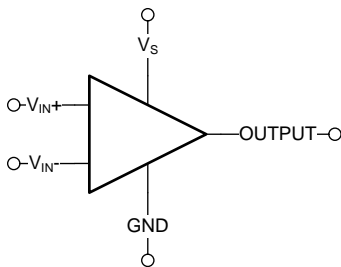


Figure 6. Basic Comparator Output

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stage

The LM397 has a bipolar input stage. The input common-mode voltage range is from 0 to $(V_S - 1.5 \text{ V})$.

7.3.2 Output Stage

The LM397 has an open-collector grounded-emitter NPN output transistor for the output stage. This requires an external pullup resistor connected between the positive supply voltage and the output. The external pullup resistor should be high enough resistance so to avoid excessive power dissipation. In addition, the pullup resistor should be low enough resistance to enable the comparator to switch with the load circuitry connected. Because it is an open-collector output stage, several comparator outputs can be connected together to create an OR'ing function output. With an open collector, the output can be used as a simple SPST switch to ground. The amount of current which the output can sink is approximately 10 mA. When the maximum current limit is reached, the output transistor will saturate and the output will rise rapidly ([Figure 7](#)).

Feature Description (continued)

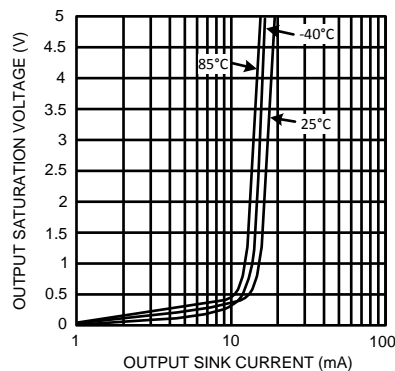


Figure 7. Output Saturation Voltage vs Output Sink Current

7.4 Device Functional Modes

7.4.1 Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the input offset voltage of the comparator. This tends to occur when the voltage on the input is equal or very close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input to effectively move quickly pass the other. Thus, effectively moving the input out of region that oscillation may occur.

For an inverting configured comparator, hysteresis can be added with a three resistor network and positive feedback. When input voltage (V_{IN}) at the inverting node is less than non-inverting node (V_T), the output is high. The equivalent circuit for the three resistor network is R_1 in parallel with R_3 and in series with R_2 . The lower threshold voltage V_{T1} is calculated by Equation 1:

$$V_{T1} = ((V_S R_2) / (((R_1 R_3) / (R_1 + R_3)) + R_2)) \tag{1}$$

When V_{IN} is greater than V_T , the output voltage is low. The equivalent circuit for the three resistor network is R_2 in parallel with R_3 and in series with R_1 . The upper threshold voltage V_{T2} is calculated by Equation 2:

$$V_{T2} = V_S ((R_2 R_3) / (R_2 + R_3)) / (R_1 + ((R_2 R_3) / (R_2 + R_3))) \tag{2}$$

The hysteresis is defined in Equation 3:

$$\Delta V_{IN} = V_{T1} - V_{T2} \tag{3}$$

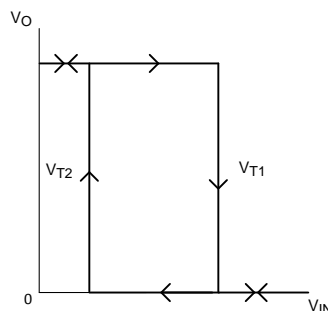


Figure 8. Inverting Configured Comparator - LM397

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LM397 will typically be used to compare a single signal to a reference or two signals against each other.

8.2 Typical Application

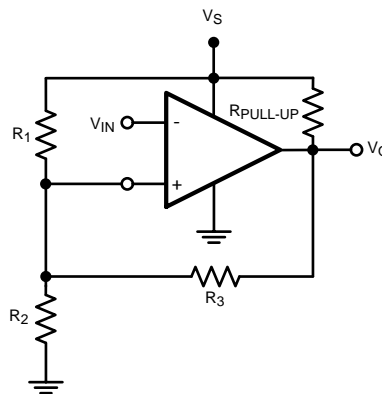


Figure 9. Inverting Comparator With Hysteresis

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0 V to $V_S - 1.5$ V
Supply voltage	5 V to 30 V
Logic supply voltage (R_{PULLUP} voltage)	5 V to 30 V
Output current (V_{LOGIC}/R_{PULLUP})	1 μ A to 20 mA
Input overdrive voltage	100 mV
Reference voltage	5.5 V

8.2.2 Detailed Design Procedure

When using TL331 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{CM}) must be taken in to account. If temperature operation is above or below 25°C the V_{CM} can range from 0 V to $V_S - 1.5$ V. This limits the input voltage range to as high as $V_S - 1.5$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN– and IN+ are both within the common mode range:
 - (a) If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - (b) If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN– and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage. To make an accurate comparison; the overdrive voltage should be higher than the input offset voltage. Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive.

8.2.2.3 Output and Drive Current

Output current is determined by the pullup resistance (R_{PULLUP}) and V_S voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use [Figure 3](#) to determine V_{OL} based on the output current. The output current can also effect the transient response.

8.2.3 Application Curves

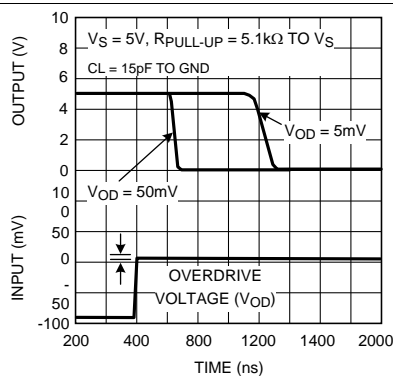


Figure 10. Response Time for Various Input Overdrives – t_{PHL}

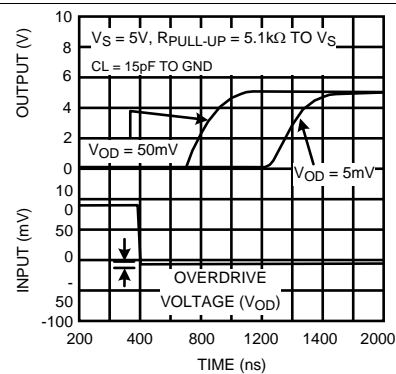


Figure 11. Response Time for Various Input Overdrives – t_{PLH}

9 Power Supply Recommendations

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement; see the [Layout Guidelines](#) section.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit-board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the LM397.
- To minimize supply noise, place a decoupling capacitor (0.1- μF ceramic, surface-mount capacitor) as close as possible to V_S as shown in [Figure 12](#).
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the top-side ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

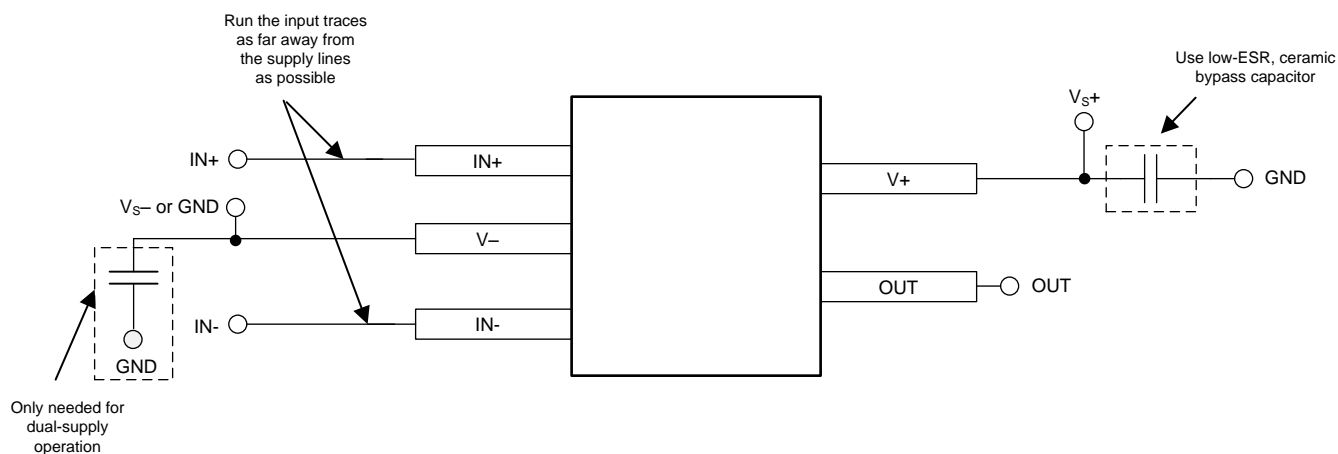


Figure 12. Comparator Board Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM397MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C397	
LM397MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C397	Samples
LM397MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C397	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

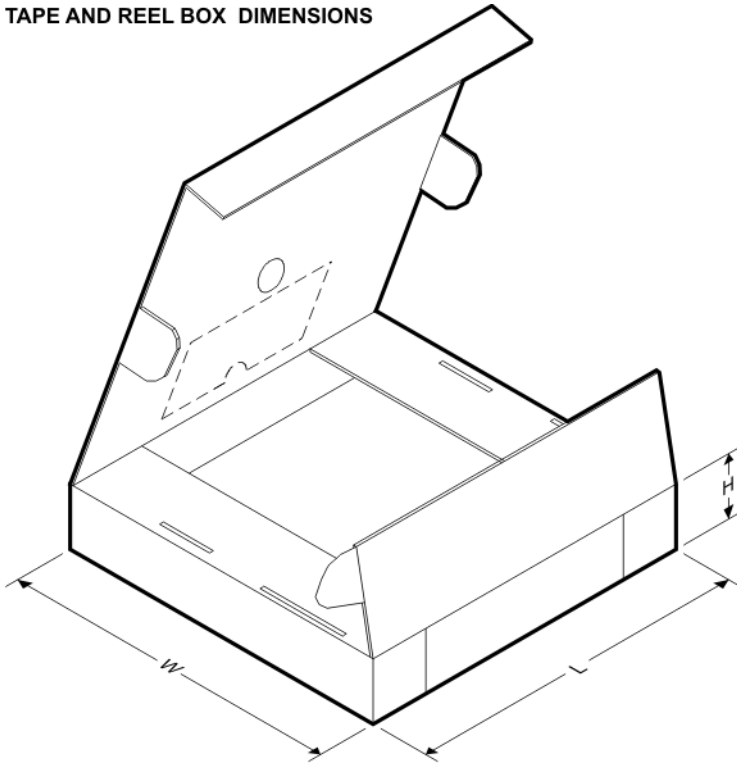
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM397MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM397MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM397MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

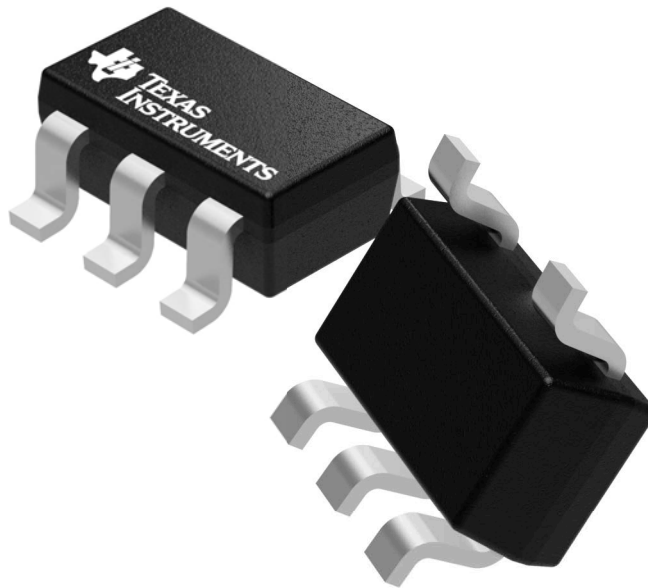
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM397MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM397MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM397MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073253/P

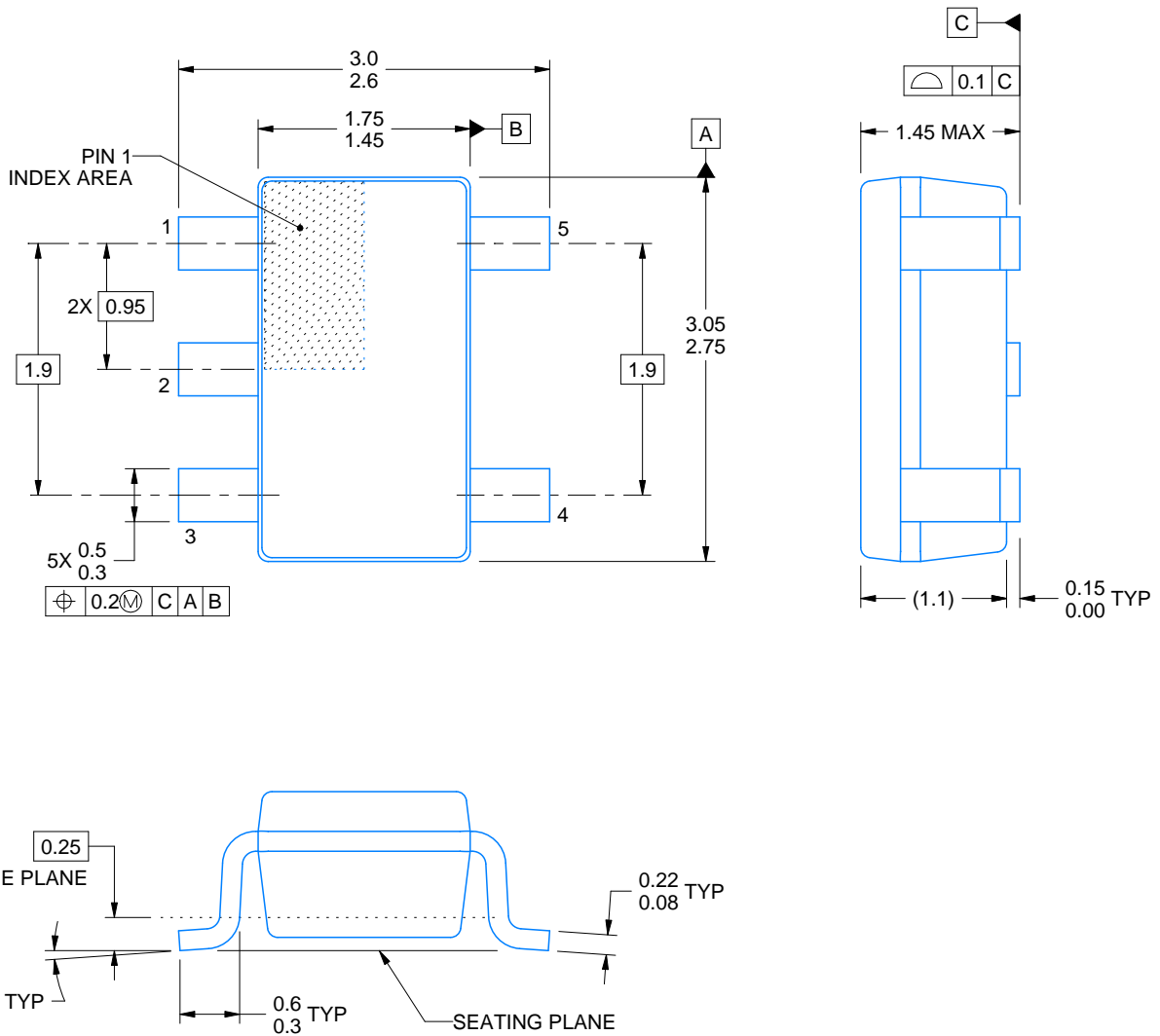
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

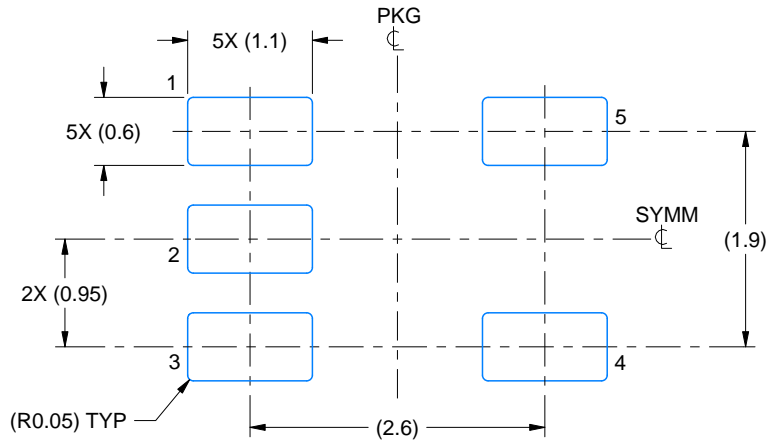
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

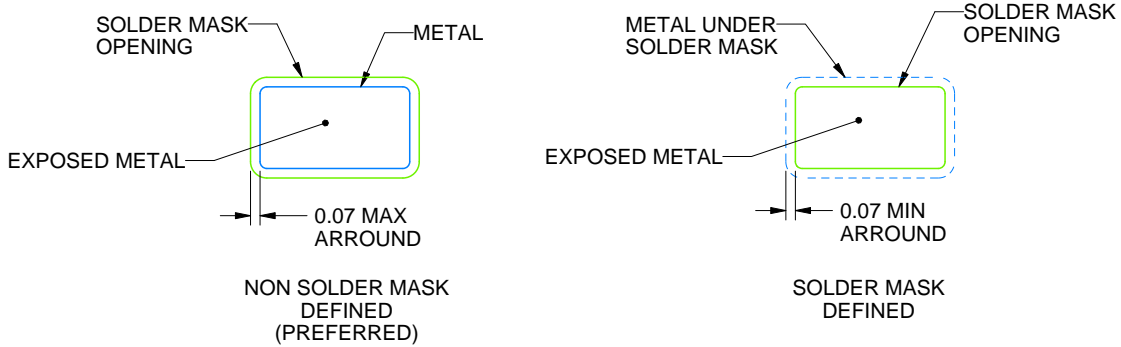
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

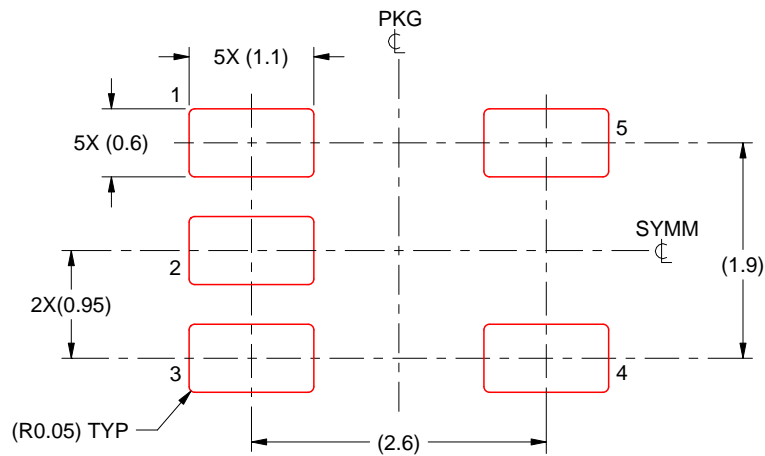
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

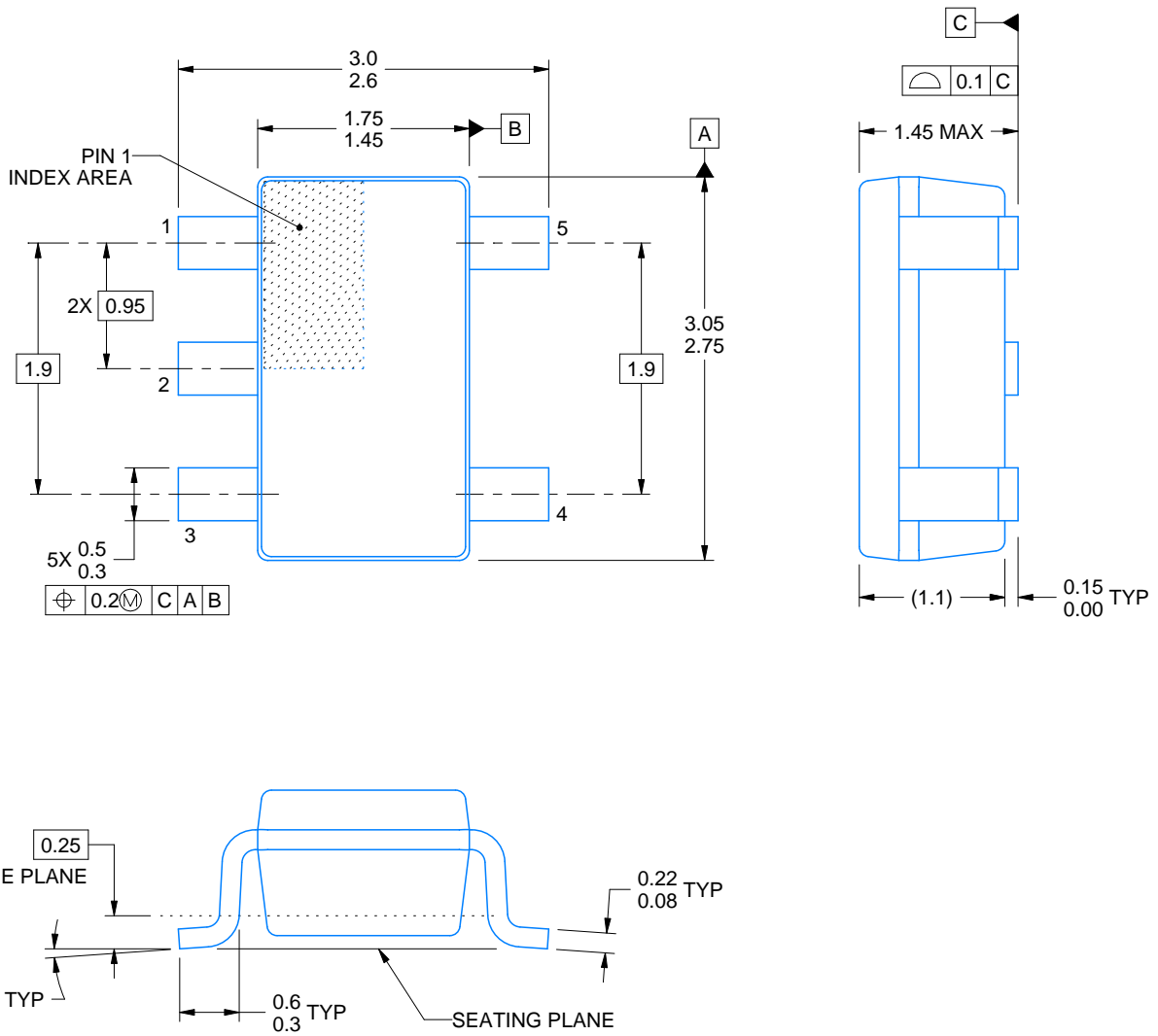
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

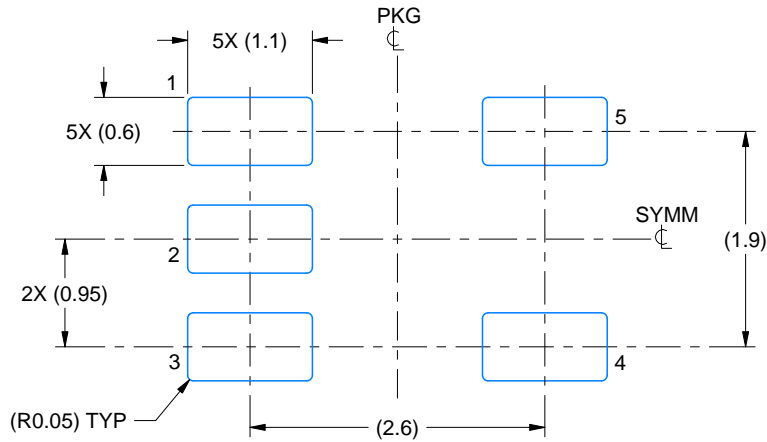
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

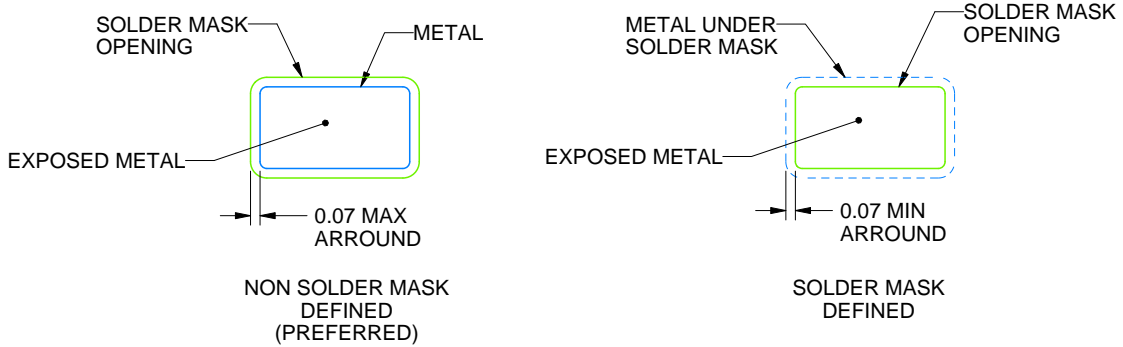
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

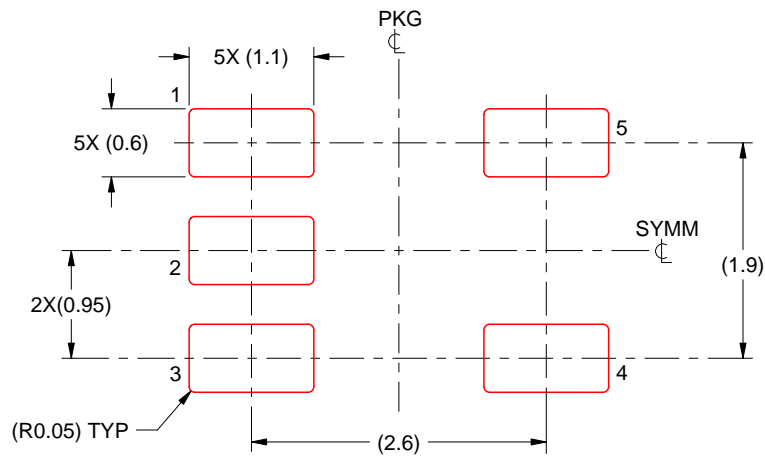
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.