
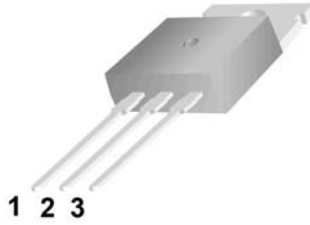
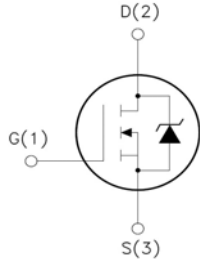


<p>Features:</p> <ul style="list-style-type: none"> <input type="checkbox"/> Low Intrinsic Capacitances. <input type="checkbox"/> Excellent Switching Characteristics. <input type="checkbox"/> Extended Safe Operating Area. <input type="checkbox"/> Unrivalled Gate Charge :Qg= 50nC (Typ.). <input type="checkbox"/> BVDSS=60V, I_D=53A <input type="checkbox"/> R_{DS(on)} : 0.015 Ω (Max) @ V_G=10V <input type="checkbox"/> 100% Avalanche Tested 	<div style="text-align: right;">  </div> <p style="text-align: center;">TO-220</p>  <div style="text-align: center;">  </div> <div style="text-align: right; margin-top: 10px;"> <p>1.Gate (G)</p> <p>2.Drain (D)</p> <p>3.Source (S)</p> </div>
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Absolute Maximum Ratings* (T_c=25°C Unless otherwise noted)

Symbol	PARAMETER	Value	Unit
V _{DSS}	Drain-Source Voltage	60	V
I _D	Drain Current	T _C =25°C	53
		T _C =100°C	35.4
V _{GSS}	Gate Threshold Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy (note1)	300	mJ
I _{AR}	Avalanche Current (note2)	50	A
P _D	Power Dissipation (T _c =25°C)	85	W
T _j	Junction Temperature(MAX)	175	°C
T _{stg}	Storage Temperature	-55~+175	°C
TL	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	PARAMETER	Typ.	MAX.	Unit
R _{θJC}	Thermal Resistance, Junction to Case	-	1.8	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	-	-	°C/W
R _{θCS}	Thermal Resistance, Case to Sink	-	110	°C/W

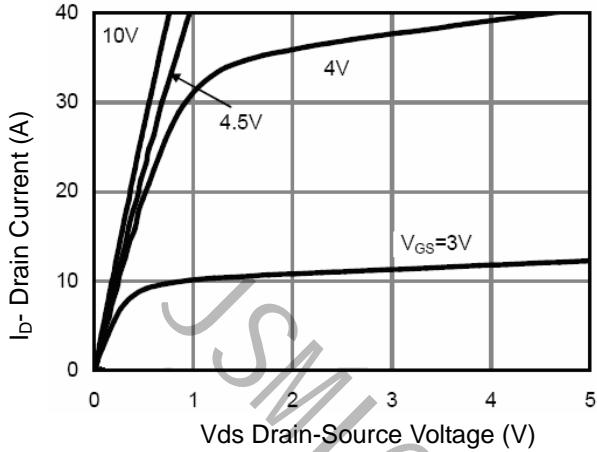
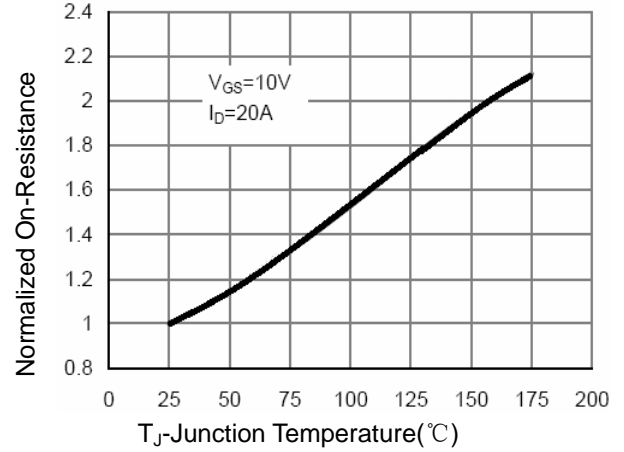
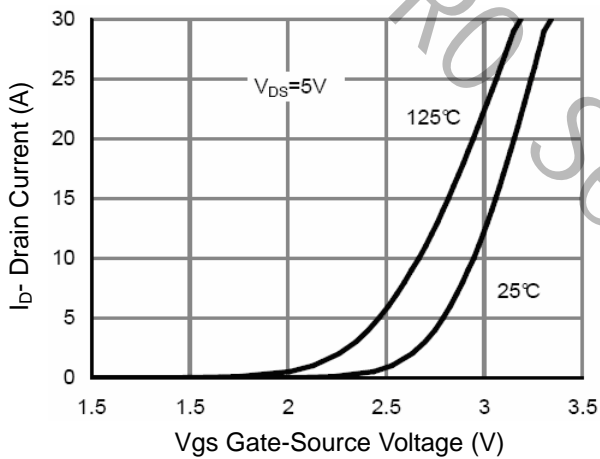
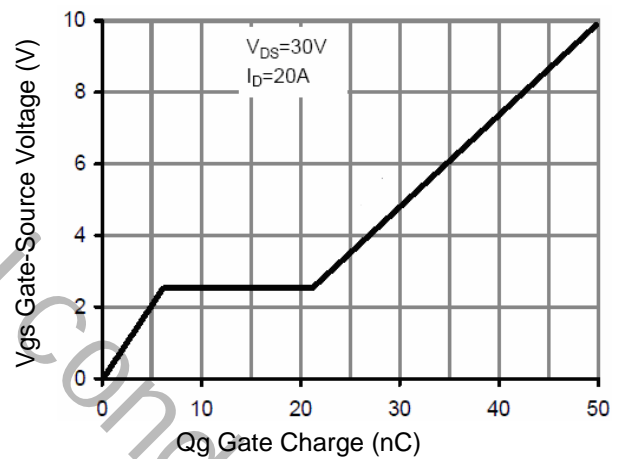
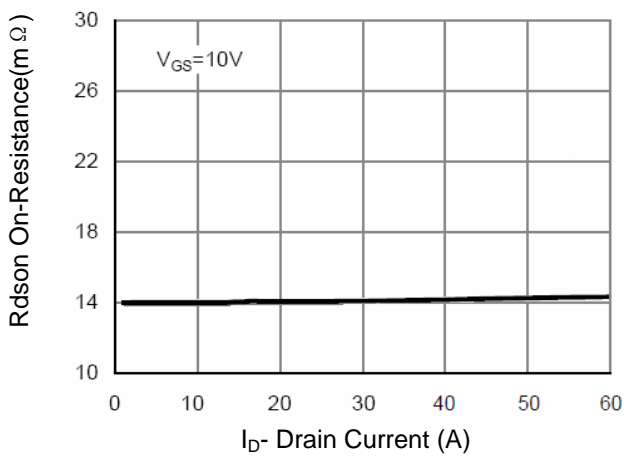
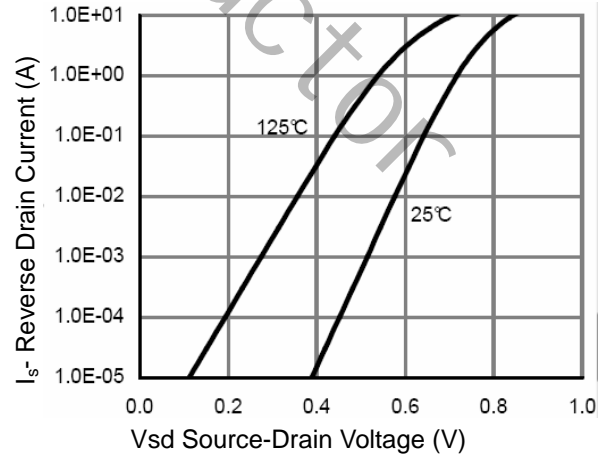
Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	-	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	12	15	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=20A$	18	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{ISS}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	2050	-	PF
Output Capacitance	C_{OSS}		-	158	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	120	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=6.7\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	7.4	-	nS
Turn-on Rise Time	t_r		-	5.1	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	28.2	-	nS
Turn-Off Fall Time	t_f		-	5.5	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=20A,$ $V_{GS}=10V$	-	50	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	nC
Gate-Drain Charge	Q_{gd}		-	15	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	53	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ (Note 3)	-	28	-	nS
Reverse Recovery Charge	Q_{rr}		-	40	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Characteristics


Figure 1 Output Characteristics

Figure 4 Rdson-Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rdson- Drain Current

Figure 6 Source- Drain Diode Forward

Typical Characteristics (Continued)

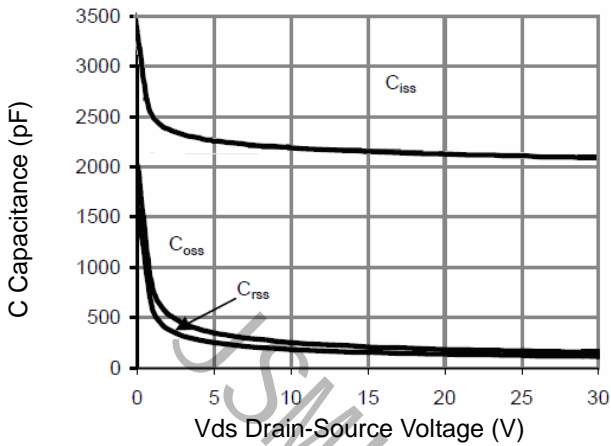


Figure 7 Capacitance vs Vds

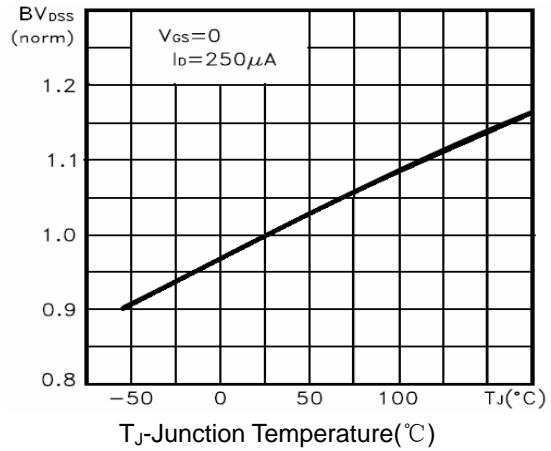


Figure 9 BV_{DSS} vs Junction Temperature

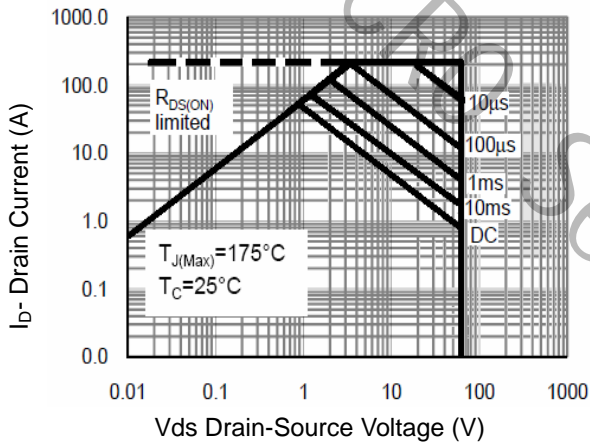


Figure 8 Safe Operation Area

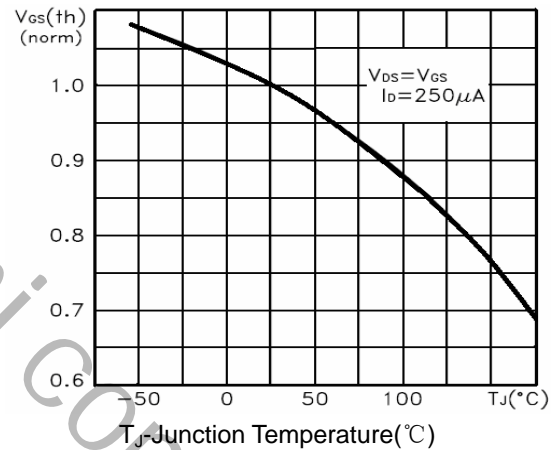


Figure 10 $V_{GS(th)}$ vs Junction Temperature

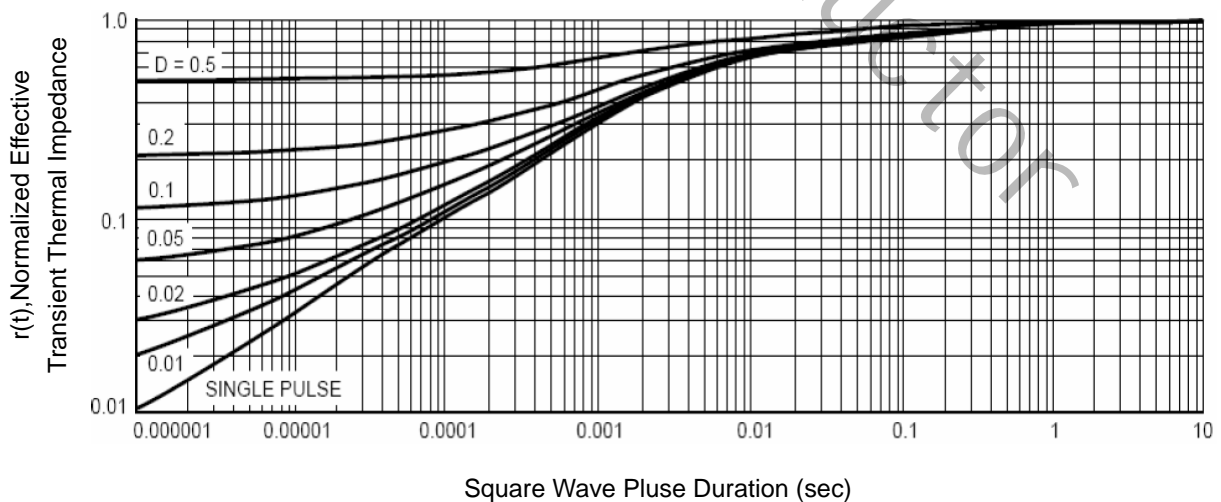
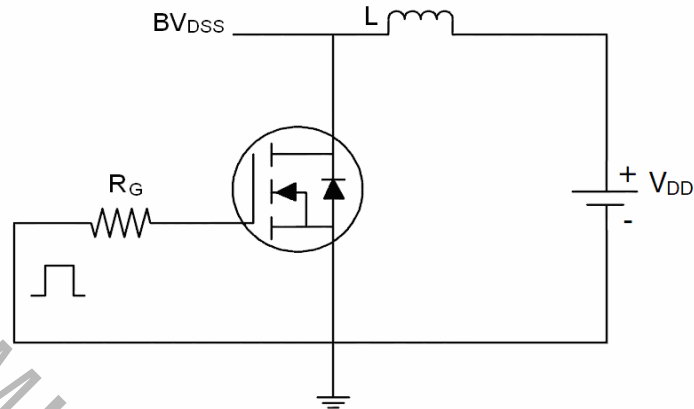


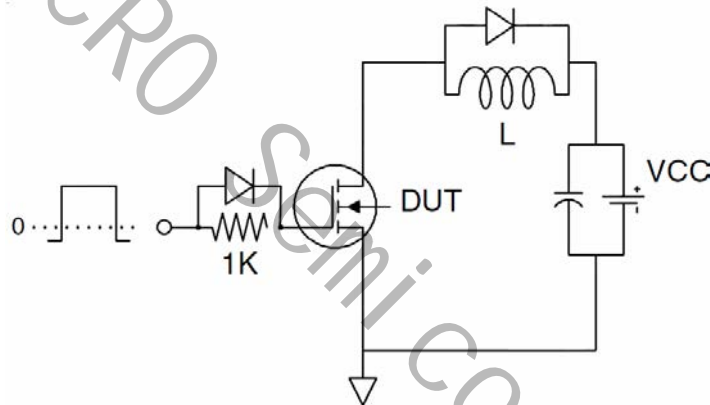
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

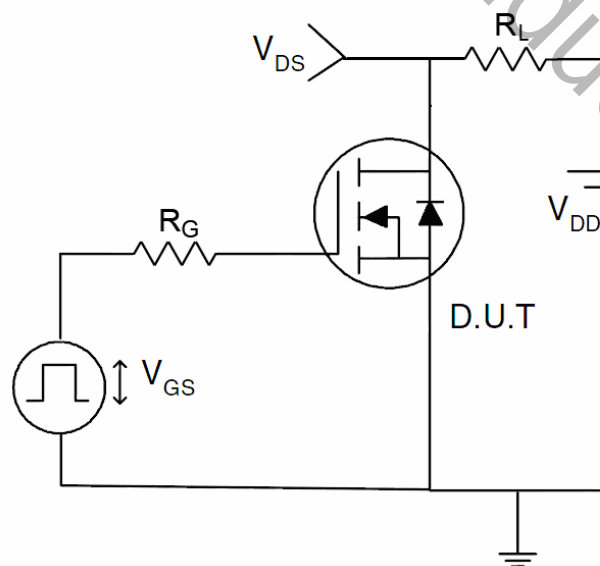
1) A_S test Circuit



2) Gate charge test Circuit



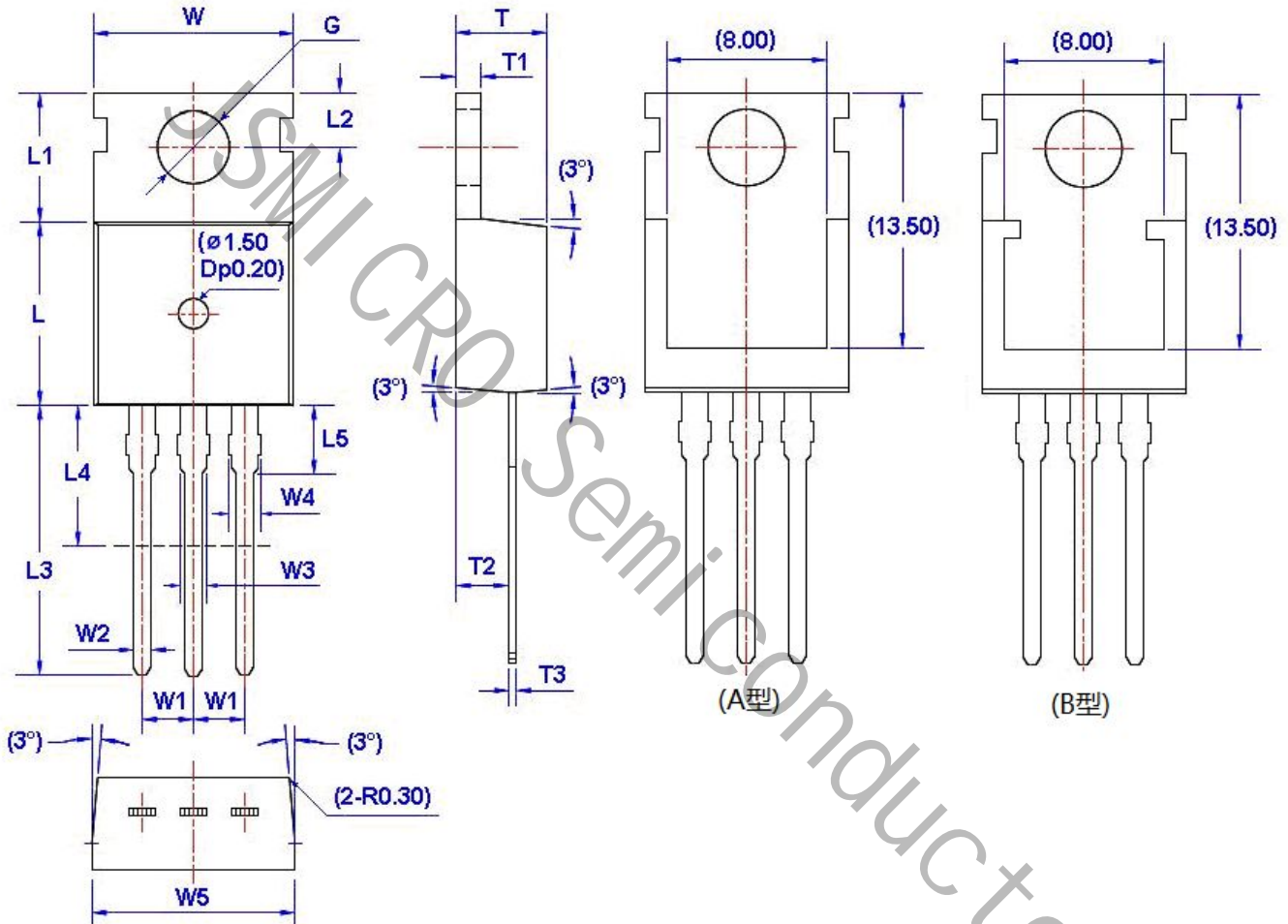
3) Switch Time Test Circuit



Package Dimension

TO-220

Unit:mm



Symbol	Size		Symbol	Size		Symbol	Size		Symbol	Size	
	Min	Max		Min	Max		Min	Max		Min	Max
W	9.66	10.28	W5	9.80	10.20	L4**	6.20	6.60	T3	0.45	0.60
W1	2.54 (TYP)		L	9.00	9.40	L5	2.79	3.30	G(Φ)	3.50	3.70
W2	0.70	0.95	L1	6.40	6.80	T	4.30	4.70			
W3	1.17	1.37	L2	2.70	2.90	T1	1.15	1.40			
W4*	1.32	1.72	L3	12.70	14.27	T2	2.20	2.60			