1. General Description

WD108xG is a high-performance quasi-resonant(QR) mode controller with low power consumption, high efficiency, etc. mainly used in offline fly-back converters.

Under normal load, the WD108xG works in QR mode. In order to reduce switching losses, the WD108xG's maximum switching frequency in QR mode is limited to 100 kHz. When the load is reduced, it works in PFM mode based on valley to conduction, and when it is light load or no load, the WD108xG works in burst mode to reduce switching losses, thereby reducing no-load power consumption and improving light load efficiency. In burst mode, the switching frequency is around 25 kHz, which effectively avoids the visible range of the human ear and eliminates audio noise.

The WD108xG has a very small VDD start-up current and operating current, which is a good peripheral design for system start time and no-load loss.

The WD108xG's built-in soft driver and optimized EMI technology make the WD108xG have good EMI performance. At the same time, the chip also provides more protection functions, including over-current protection (OCP), over-load protection (OLP), under-voltage lockout (UVLO), over-temperature protection (OTP), and over-voltage protection (OVP).

The WD108xG is available in a TO220F-6 package

2. Features

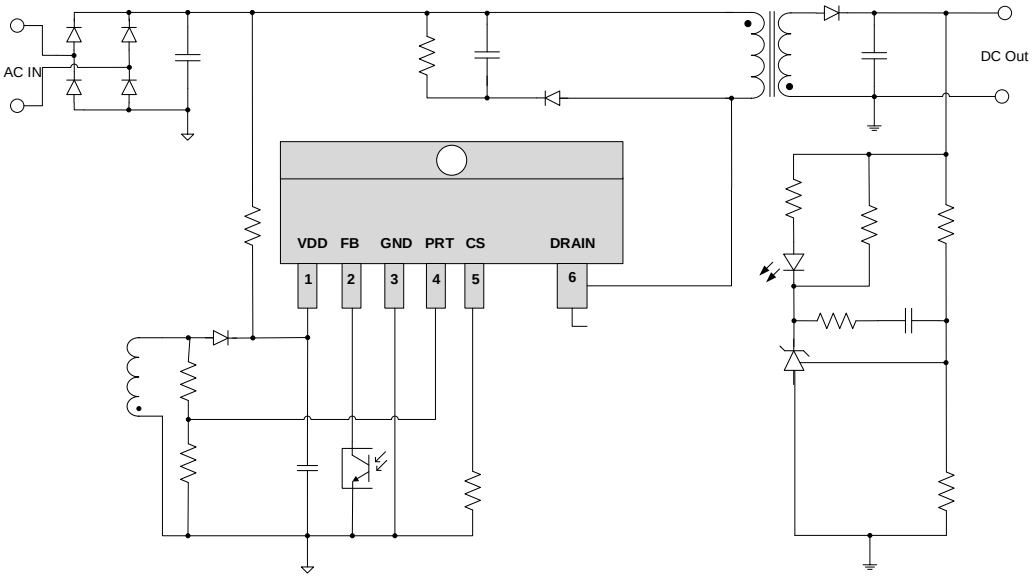
- Soft start at boot to reduce MOSFET overshoot
- Very low starting and operating currents
- Current mode PWM control
- Quasi-resonant mode of valley switching
- Burst mode control without audio noise reduces no-load power consumption and improves light-load efficiency
- The frequency can be increased in case of overload
- Frequency jitter contributes to good EMI performance
- Cycle-by-cycle current limiting provides stable limiting power over a common input voltage range
- Under-voltage Lockout (UVLO)
- Over-load Protection Function (OLP)
- Built-in and external optional over-temperature protection (OTP)
- Output Overvoltage Protection (OVP)
- Output diode short-circuit protection self-recovery
- Built-in 700V10A power tube

3. Applications

AC/DC off-line flyback switching power supply is used in:

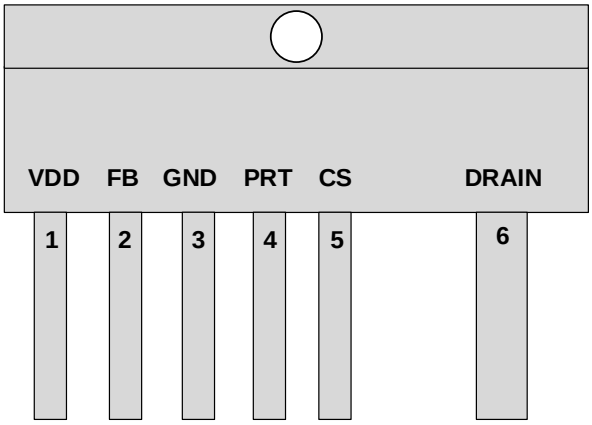
- Printers, Batteries
- Power Adapter

4. Typical Application



5. Pin Configuration

(Top View)



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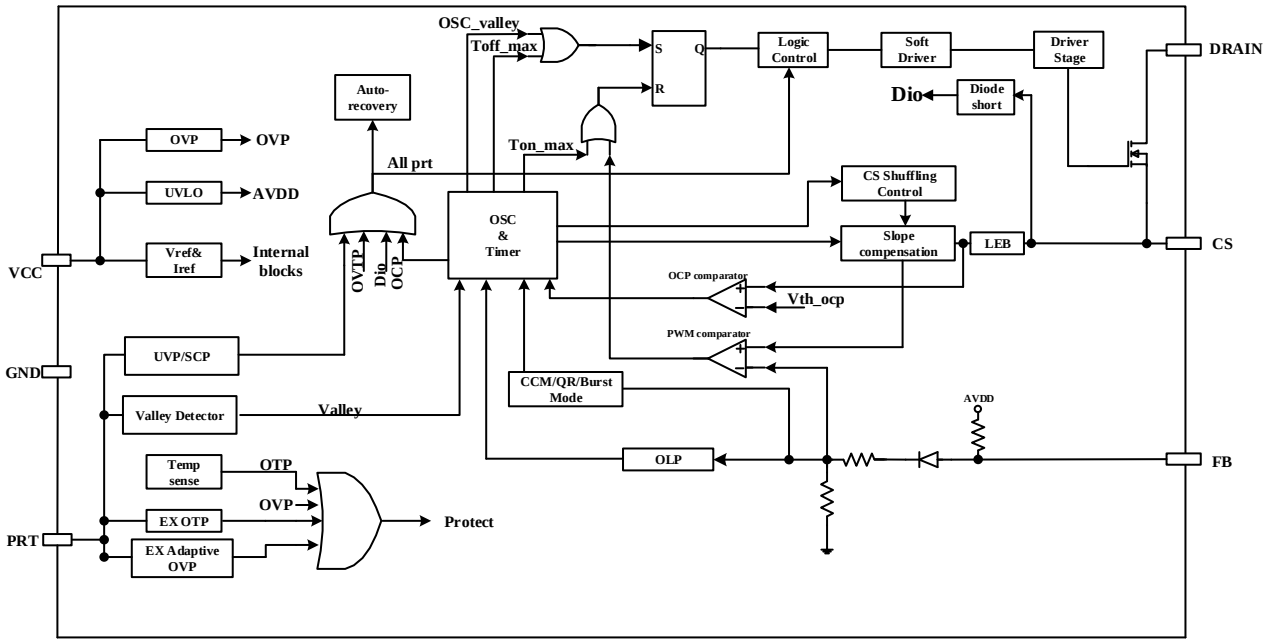
6. Pin Description

Pin Number	Pin Name	Function
1	VDD	Power Supply.
2	FB	Feedback signal input. The PWM duty cycle is determined by this pin level and the CS input signal.
3	GND	Ground.
4	PRT	Valley switching detection.
5	CS	Current sense
6	DRAIN	Drain of integrated MOSFET.

7. Functional Block Diagram



8. Absolute Maximum Ratings[1]

Parameter	Range
VDD supply voltage	V_{OVP}-1V
RT input voltage	-0.3 V to 7 V
CS input voltage	-0.3 V to 7 V
FB input voltage	-0.3 V to 7 V
Operating junction temperature T_J	-40 ℃ to 150 ℃
Operating ambient temperature T_A	-40 ℃ to 85 ℃
Storage Temperature T_{stg}	-55 ℃ to 150 ℃
Soldering temperature (solder, 10secs)	260 ℃

NOTE1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

9. Package Dissipation Rating

Package	$R_{\theta JA}$ (℃/W)
TO220F-6	2.6

10. Electrical Characteristics

(V_{DD}=20V, T_A=25℃, unless otherwise noted)

Symbol	Parameter	Text Conditions	Min	Typ	Max	Unit
Supply Voltage（VDD）						
I_{DD_ST}	VDD Startup Current	VDD=16V, measure the current into VDD		2	5	uA
I_{DD_OP}	VDD Operation Current	VDD=20V, FB=3V, CS=3.8V, measure the current into VDD		1.5	2.5	mA
I_{DD_Burst}	Burst Current	VDD=20V, FB=0.5V, CS=0V,measure the current into VDD		0.57	0.75	mA
$V_{UVLO(ON)}$	VDD Under-Voltage Lockout Enter	VDD falling		8.3		V
$V_{UVLO(OFF)}$	VDD Under Voltage Lockout Exit(Recovery)	VDD rising		18.1		V
V_{PULL_UP}	Pull-up PMOS active			10.2		V
Vdebounce _burst	Disable burst mode			9.4		V
OVP	VDD Over Voltage Protection voltage	FB=3V, CS=0V, Ramp up VDD until gate clock is off	27.7	29.2	30.7	V
Feedback Input（FB）						
A_{VCS}	PWM input gain	$\Delta V_{FB}/\Delta V_{CS}$		4.5		V/V
V_{FB_OPEN}	VFB open-loop voltage			5.0		V
I_{FB_SHORT}	FB pin short circuit current	Short circuit FB to GND and measure current		0.21		mA
$V_{TH\_Burst\_L}$	Enter the Burst mode threshold			1.30		V
$V_{TH\_Burst\_H}$	Exit Burst mode threshold			1.40		V
V_{TH_green}	Enter the Green mode threshold			2.3		V
V_{TH_PL}	The threshold voltage of FB when overload protection is triggered			4.39		V
t_{D_PL}	Power Limiting Debounce Time			15		ms

Symbol	Parameter	Text Conditions	Min	Typ	Max	Unit
Z_{FB_IN}	Input impedance			30		kΩ
Ton	Maximum on-time	VDD=20V, FB=3V, CS=0V		15		uS
Current Sense Input (CS)						
t_{LEB}	Leading edge blanking time			300		ns
$V_{TH\_OC\_min}$	Internal Current Limiting Threshold Voltage with zero duty cycle			0.5		V
$V_{TH\_OC\_max}$	Overcurrent protection threshold			0.70		V
t_{D_OC}	Detect and control delay	From Over Current Occurs till the gate driver output start to turn off		100		ns
t_{D_OCP}	OCP debounce time			60		ms
T_{SS_CS}	Soft-start time of CS threshold			4		ms
Oscillator						
f_{osc_QRmin}	QR frequency low limit	VDD=20V, FB=3V, CS=3.8V		50		kHz
Δf_{osc_QRmin}	FM range/fundamental frequency		-6.5		6.5	%
f_{osc_QRmax}	QR frequency high limit	VDD=20V, FB=3V, CS=3.8V, Delay5ms VDD=9V		82		kHz
f_{osc_max}	Peak frequency			100		kHz
$f_{JITTERING}$	Jitter frequency			250		Hz
SST_freq	Soft-start time of frequency			30		ms
Δf_T	Frequency temperature stability			1		%
Δf_{VDD}	Frequency voltage stability			1		%
f_{BURST}	Burst mode switch frequency			24		kHz

Symbol	Parameter		Text Conditions	Min	Typ	Max	Unit
Gate driver（GATE）							
V_{OL}	Output low					1	V
V_{OH}	Output high			7			V
V_{GATE_CLAMP}	Output clamp voltage				12		V
t_R	Output rising time				100		ns
t_F	Output falling time				30		ns
Composite functionality（PRT）							
V_{OTP}	OVP voltage thresholds				2.45		V
I_{IN_OVP}	OVP threshold				400		uA
Chip internal overtemperature protection（OTP）							
T_{Enter}	OTP level				135		℃
T_{EXIT}	OTP exit				123		℃
Power MOSFET inside the chip							
BV_{DSS}	Drain-source breakdown voltage			700			V
R_{DSON}	On-resistance	WD1082G	V_{GS}= 10V, I_{DS}=6A			0.87	Ω
R_{DSON}		WD1083G	V_{GS}= 10V, I_{DS}=6.5A			0.75	Ω
R_{DSON}		WD1084G	V_{GS}= 10V, I_{DS}=7A			0.65	Ω
R_{DSON}		WD1085G	V_{GS}= 10V, I_{DS}=9A			0.56	Ω

11. Function Description

The WD108xG is a high-performance AC/DC current-mode PWM controller for isolated fly-back applications. The WD108xG's burst mode control reduces power consumption and achieves high efficiency. At the same time, the WD108xG is highly integrated to reduce the number and size of external components, and its main internal functions are described as follows:

11.1 Protection controls

The reliability of a good power supply system is achieved by its rich protection functions. These include cycle-by-cycle current limit (OCP), over-voltage protection, over-temperature protection (OTP), FB open-circuit protection .etc.

The power supply is provided by the auxiliary windings of the transformer. The internal UVLO comparator detects the VDD pin voltage, and its turn-on and turn-off threshold voltages are fixed at 18.1V (UVLO-OFF) and 8.3V (UVLO-ON). During start-up, the VDD voltage must be charged to 18.1V through the start-up resistor and capacitor to turn on the chip, and the start-up capacitor will continue to supply current to the VDD until the transformer auxiliary windings are fully energized. The threshold voltage difference of UVLO is to prevent false triggering caused by VDD voltage drops during start-up. When the supply voltage is lower than 8.3V (UVLO-ON), the output of the WD108xG is automatically turned off, and the system is restarted after the power supply soft-start.

When the output is overloaded or short, the chip may be damaged. The WD108xG has an integrated OLP function, when an overload or short occurs, the feedback loop will pull up the FB terminal voltage, and when this voltage value exceeds 4.3V, the internal detection circuit will generate a delay signal of 15ms and eventually shut down the power MOSFET and pull down the VDD until the circuit restarts.

11.2 Starting Current and Operating Current

During start-up, the VDD value is lower than the UVLO threshold, so the WD108xG does not work, at this time, the current is charged to the capacitor through the start-up resistor to raise the VDD, when the VDD voltage rises to the point that the WD108xG exits UVLO mode, the WD108xG starts to work normally, outputs the gate signal, and the auxiliary winding of the transformer provides working current to the chip at this time. Lower start-up and operating currents mean larger start-up resistors and smaller start-up capacitors. The WD108xG has typical start-up and operating currents of 2uA and 1.5mA, respectively.

11.3 Soft start

Once the voltage of the VDD reaches UVLO(OFF), the internal soft-start circuit forces the peak voltage at the CS terminal to gradually rise from 0.05V to the maximum value over a period of 4ms to mitigate the voltage over-shoot experienced by the power MOS transistor during start-up. Each restart is accompanied by a soft-start process.

11.4 Current Detection and Overcurrent Limiting

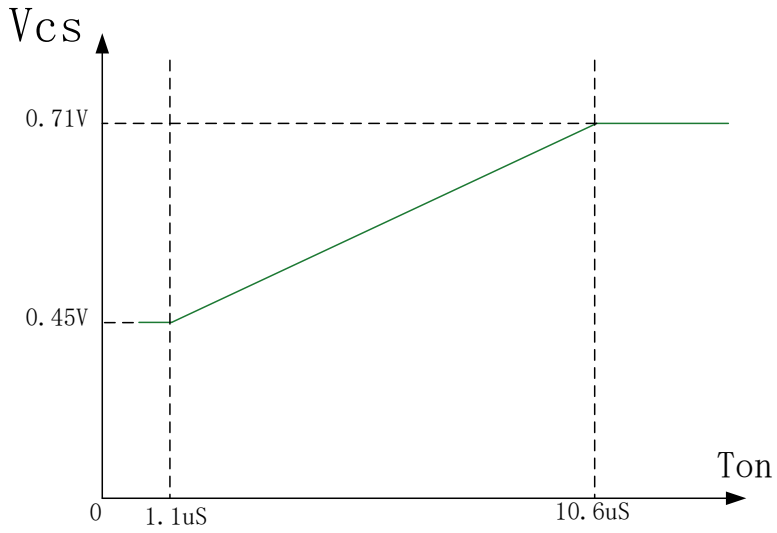
The WD108xG uses peak current control to regulate the output voltage and cycle-by-cycle current limiting. The switching peak current is detected by detecting the voltage on the resistor connected to the CS voltage, and the duty cycle depends on the current sensing signal and the feedback voltage V_{FB}. If the CS voltage is greater than the threshold voltage, the internal comparator triggers a signal and shuts down the power MOS transistor. Each time the power MOSFET is turned on, the overshoot of current will occur on the CS sampling

resistor due to the reverse recovery of the freewheeling diode. To avoid possible false triggering, an internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period.

11.5 Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

11.6 OCP Compensation



11.7 Gate drive

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

11.8 Burst working mode

A large part of the losses in switching power supplies come from the switching losses of the MOSFETs and the copper losses of the transformers. This part of the loss is closely related to the switching frequency. The lower the switching frequency, the lower the losses.

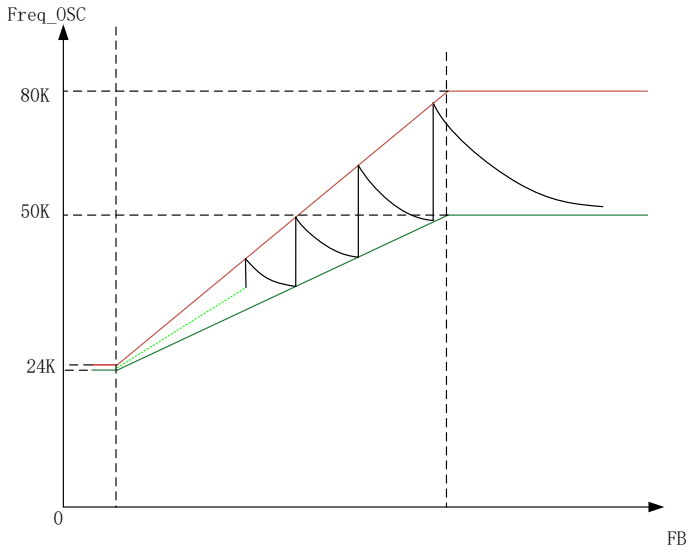
Under no-load or light-load conditions, the WD108xG's burst mode function continuously reduces the PWM frequency by adjusting the turn-off time of the switch. To avoid audio noise, the minimum PWM frequency is set to 25kHz. Depending on the load conditions, the conversion mode is automatically adjusted. To further reduce losses, the chip enters burst mode when the FB voltage is lower than the threshold voltage ($V_{REF\_BURST\_L}$) to enter burst mode. At this point, the PWM output signal is turned off, and the PWM output will not be turned on again until the FB voltage is higher than the threshold voltage ($V_{REF\_BURST\_H}$) to exit the burst mode. Burst mode further reduces the losses of the switching power supply, thereby improving the standby power consumption of the system.

11.9 Frequency jitter improves EMI

WD108XG has a frequency jitter function (adjusting the switching frequency), which optimizes the EMI performance and cost of the system.

11.10 Operation of the oscillator

The frequency adjustment of the WD108xG is shown in the following figure.



11.11 Input voltage OVP & Output voltage OVP composite function

The WD108xG's PRT pin provides reliable and accurate detection of the input voltage OVP and output voltage OVP, and the function of the composite pin is realized simultaneously by time-separated technology.
For the input voltage function and OVP function, I_{IN_OVP} is calculated as follows

$$I_{IN\_OVP} = \frac{V_{IN} \times \frac{Naux}{Np}}{R_{UP}}$$

Where: Naux is the number of auxiliary winding turns

Np is the number of secondary winding turns

For the output voltage function, V_{OUT_OVP} has the following formula:

$$V_{OUT\_OVP} = V_{OUT} \times \frac{Naux}{N_S} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}$$

Where: R_{UP} is the resistance between the PRT pin and the auxiliary winding

R_{DOWN} is the resistance between the PRT pin and the ground

12. Package Information

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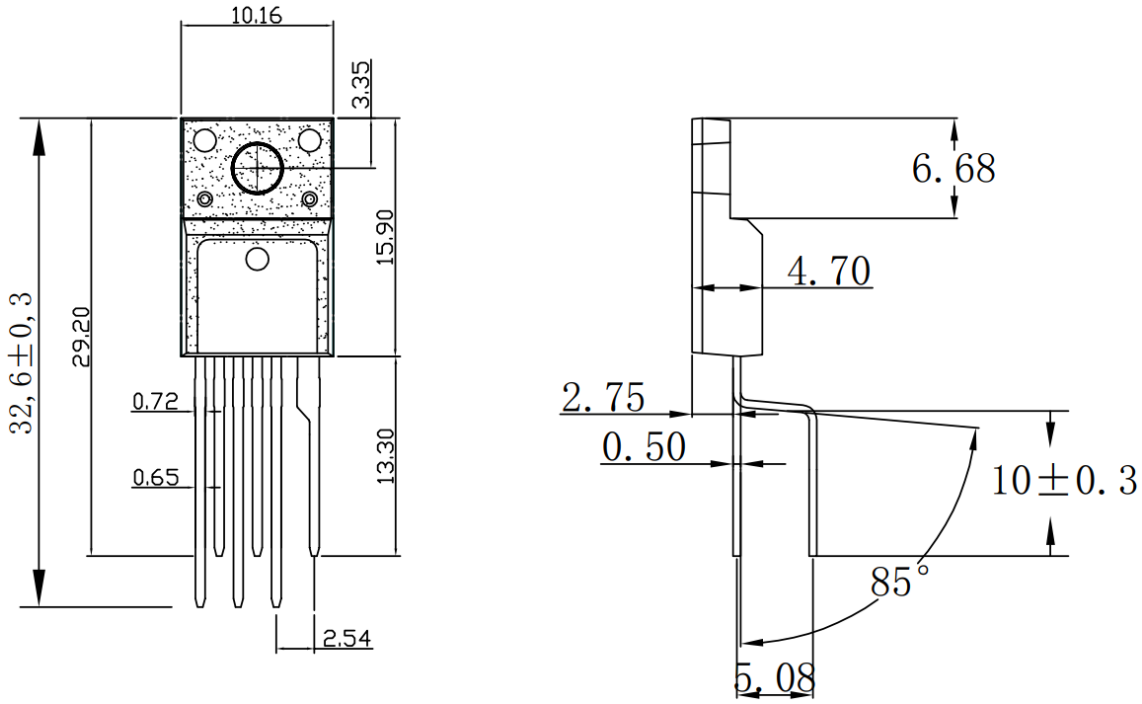

13. Ordering Information

Product Name	Package	Package Quantity
WD1082GDET	TO220F-6	50/Tube
WD1083GDET	TO220F-6	50/Tube
WD1084GDET	TO220F-6	50/Tube
WD1085GDET	TO220F-6	50/Tube

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For additional information, please contact your local Sales Representative.

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The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.
Users should verify actual device performance in their specific applications.

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