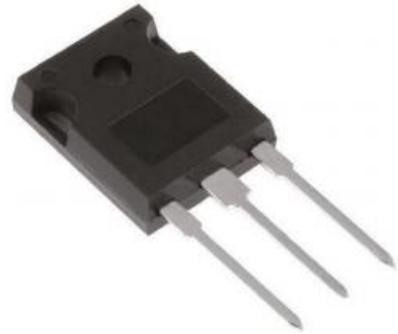


N-Channel MOSFET

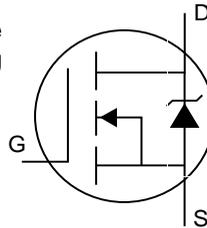
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

TO-247AC



Description

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



$$V_{DSS} = 55V$$

$$R_{DS(on)} = 0.008\Omega$$

$$I_D = 110A\text{⑥}$$

Absolute Maximum Ratings

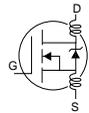
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	110⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	80⑥	
I_{DM}	Pulsed Drain Current ①⑤	390	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	480	mJ
I_{AR}	Avalanche Current①	59	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

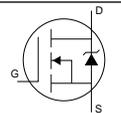
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.008	Ω	V _{GS} = 10V, I _D = 59A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	42	—	—	S	V _{DS} = 25V, I _D = 59A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 44V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	170	nC	I _D = 59A
Q _{gs}	Gate-to-Source Charge	—	—	32		V _{DS} = 44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	74		V _{GS} = 10V, See Fig. 6 and 13 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	—	14	—	ns	V _{DD} = 28V
t _r	Rise Time	—	100	—		I _D = 59A
t _{d(off)}	Turn-Off Delay Time	—	43	—		R _G = 2.5Ω
t _f	Fall Time	—	70	—		R _D = 0.39Ω, See Fig. 10 ^{④⑤}
L _D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	13	—		
C _{iss}	Input Capacitance	—	4000	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1300	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	480	—		f = 1.0MHz, See Fig. 5 ^⑤



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	110 ^⑥		MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	390		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 59A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	110	170	ns	T _J = 25°C, I _F = 59A
Q _{rr}	Reverse Recovery Charge	—	450	680	nC	di/dt = 100A/μs ^{④⑤}



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 25V, starting T_J = 25°C, L = 190μH
R_G = 25Ω, I_{AS} = 59A. (See Figure 12)
- ③ I_{SD} ≤ 59A, di/dt ≤ 290A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRF3205 data and test conditions
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

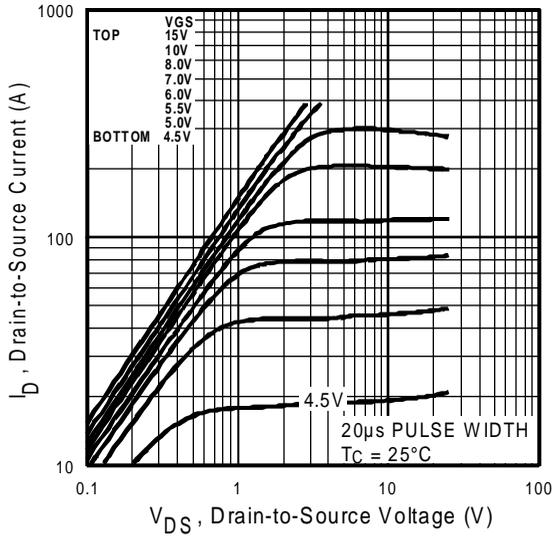


Fig 1. Typical Output Characteristics

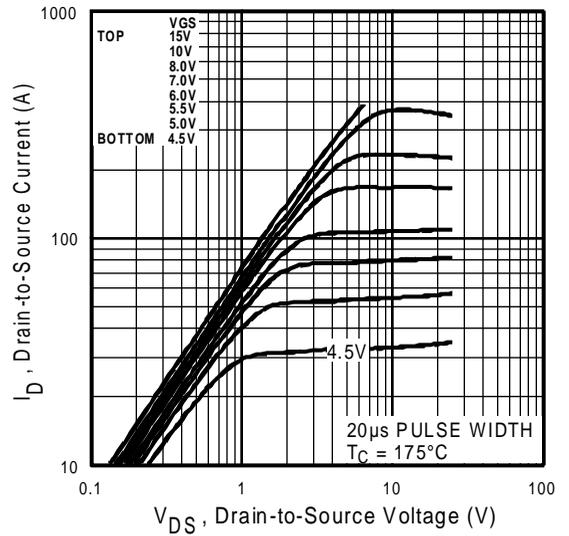


Fig 2. Typical Output Characteristics

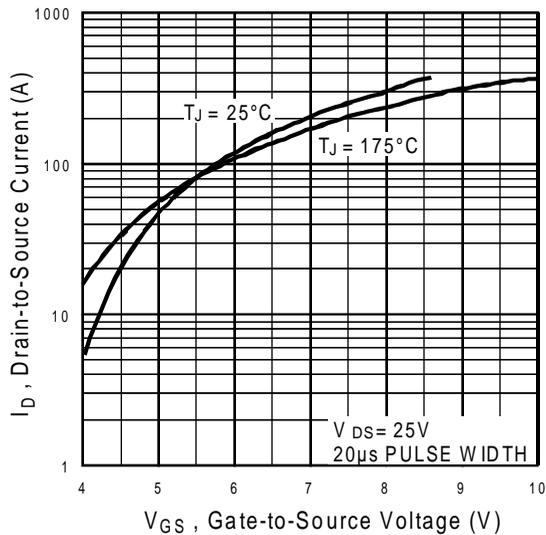


Fig 3. Typical Transfer Characteristics

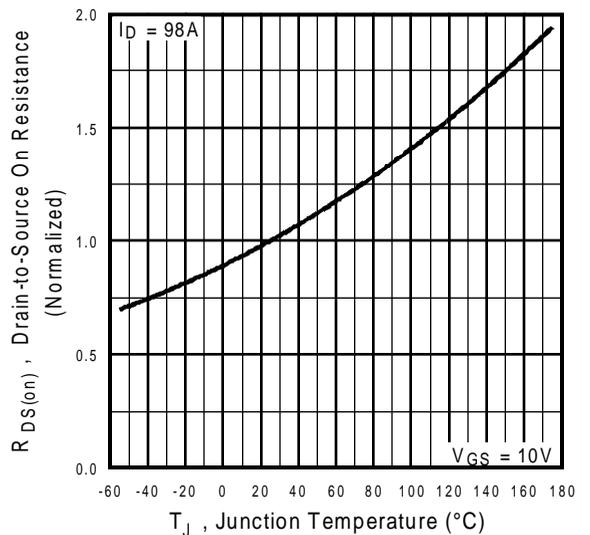


Fig 4. Normalized On-Resistance Vs. Temperature

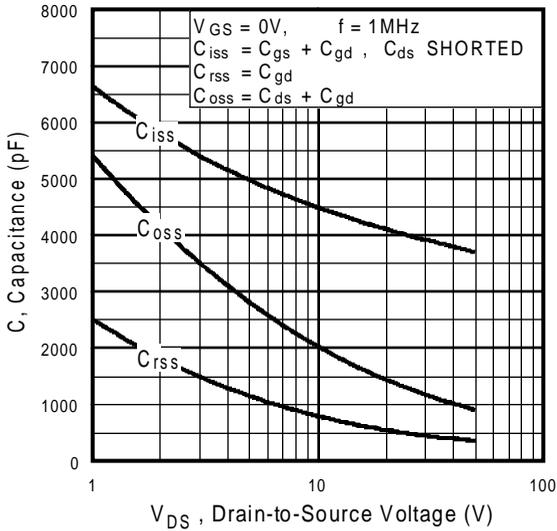


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

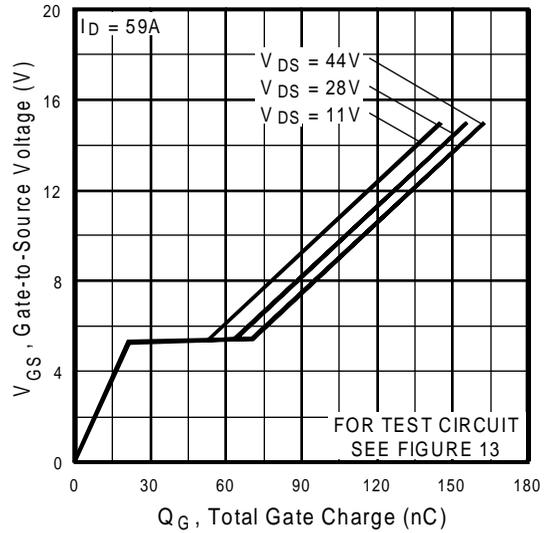


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

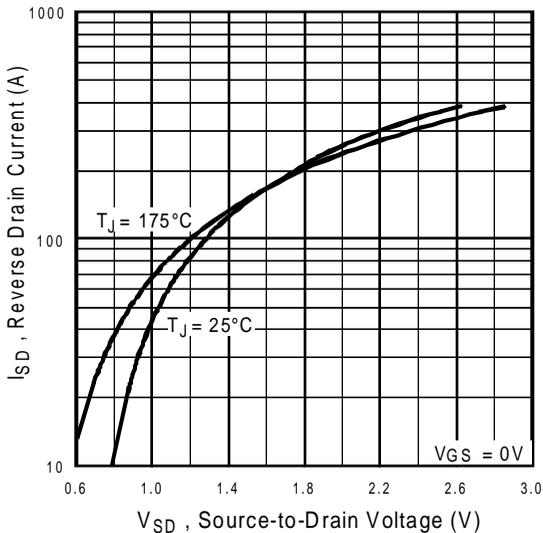


Fig 7. Typical Source-Drain Diode Forward Voltage

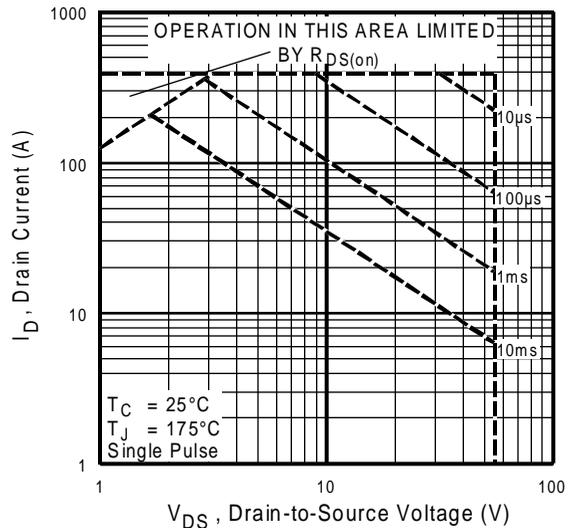


Fig 8. Maximum Safe Operating Area

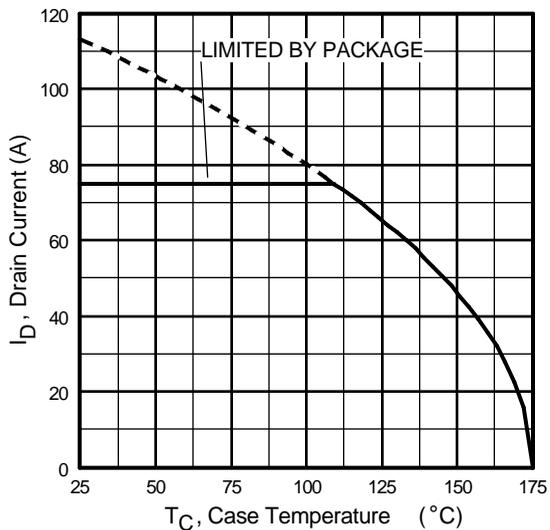


Fig 9. Maximum Drain Current Vs. Case Temperature

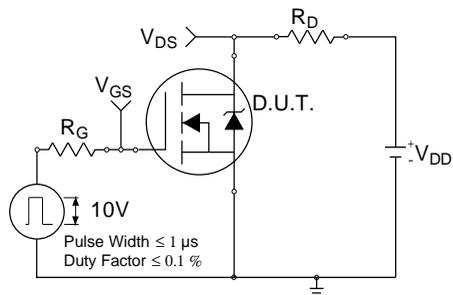


Fig 10a. Switching Time Test Circuit

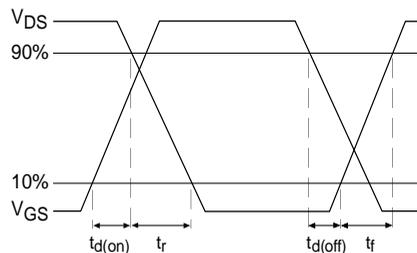


Fig 10b. Switching Time Waveforms

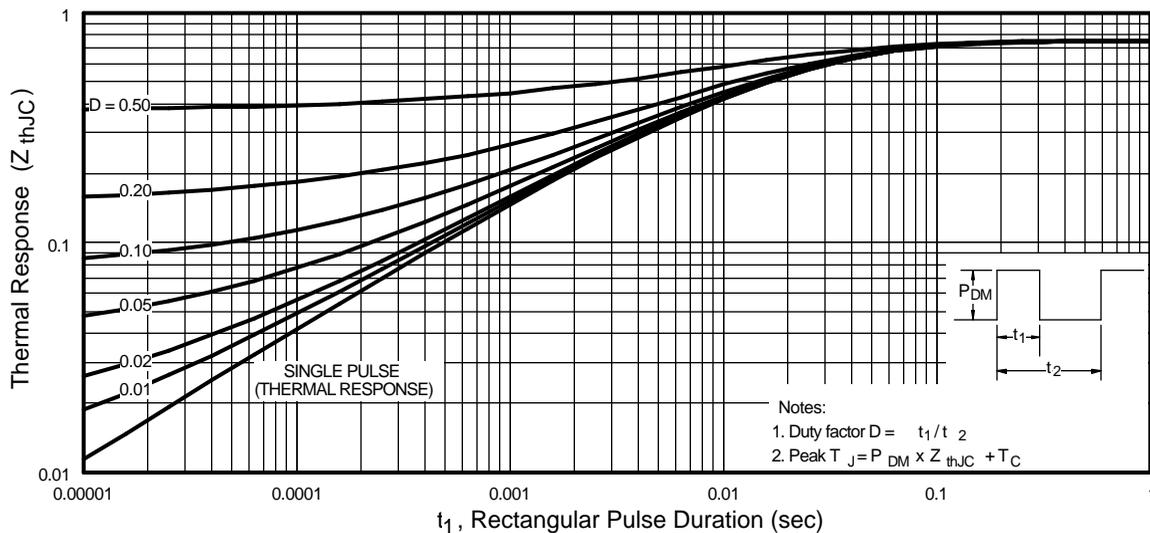


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

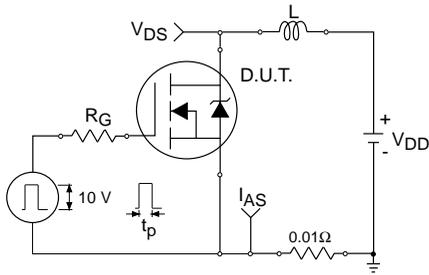


Fig 12a. Unclamped Inductive Test Circuit

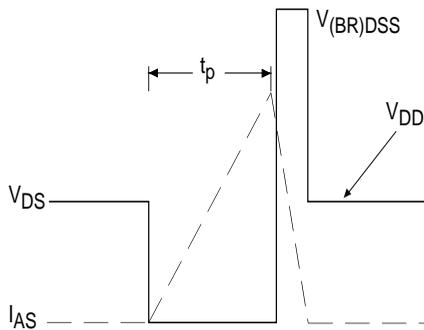


Fig 12b. Unclamped Inductive Waveforms

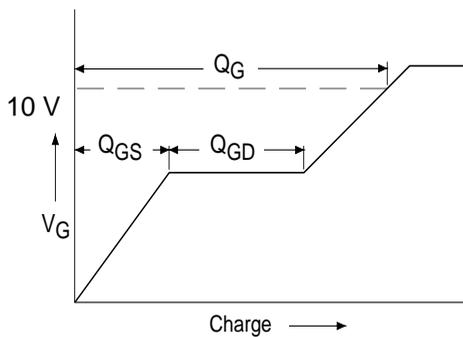


Fig 13a. Basic Gate Charge Waveform

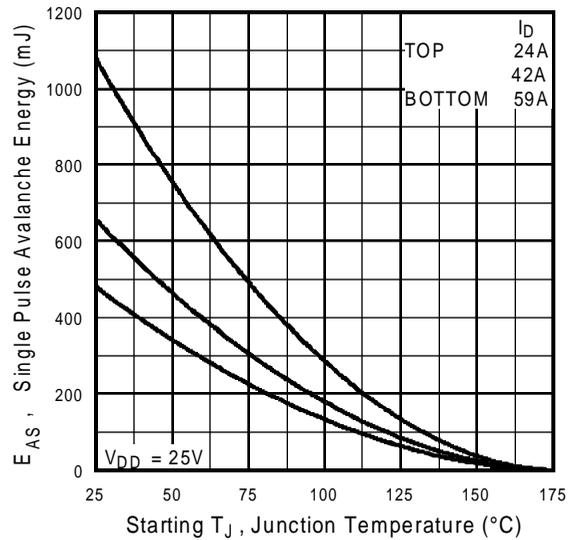


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

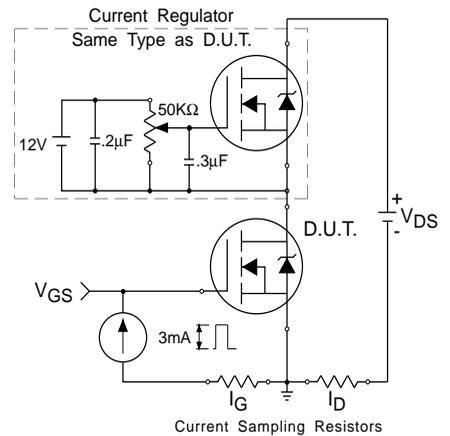
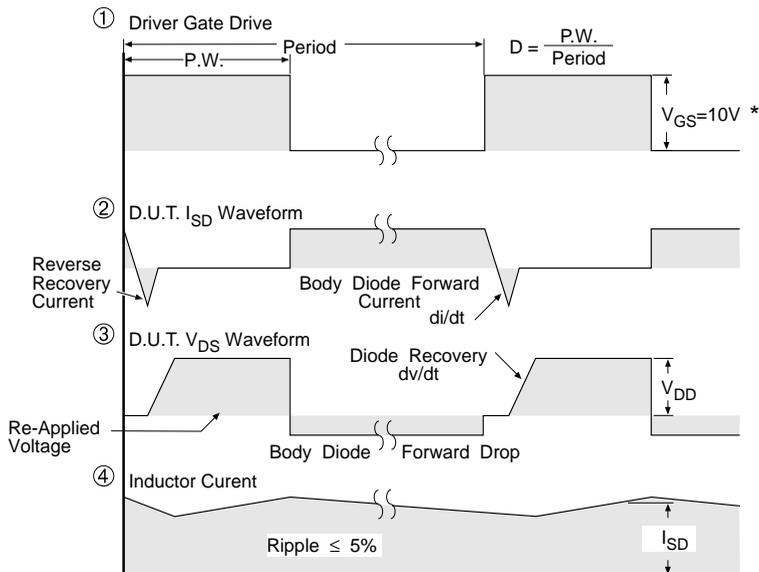
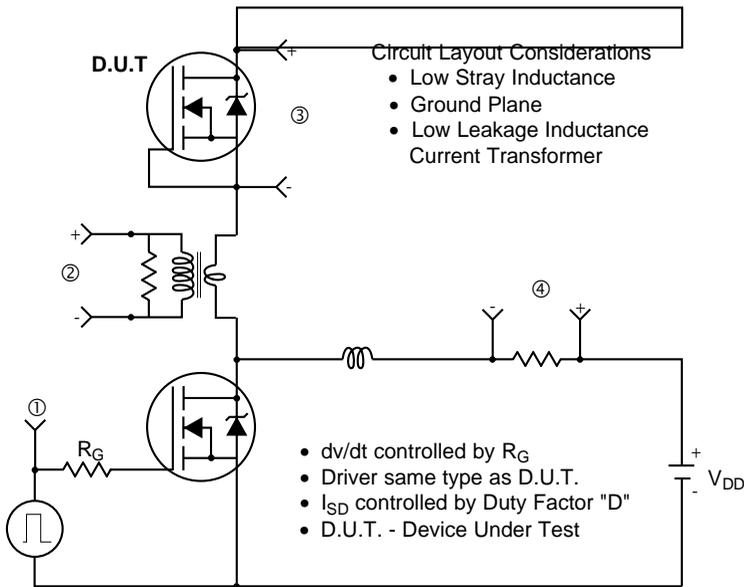


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

