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March 2009

# FDS6679AZ

# P-Channel PowerTrench® MOSFET

-30V, -13A,  $9m\Omega$ 

#### **General Description**

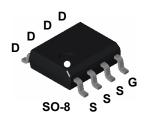
This P-Channel MOSFET is producted using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance.

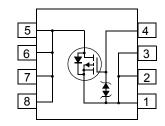
This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

#### **Features**

- Max  $r_{DS(on)}$  = 9.3m $\Omega$  at  $V_{GS}$  = -10V,  $I_D$  = -13A
- Max  $r_{DS(on)}$  = 14.8m $\Omega$  at  $V_{GS}$  = -4.5V,  $I_D$  = -11A
- Extended V<sub>GS</sub> range (-25V) for battery applications
- HBM ESD protection level of 6kV typical (note 3)
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handing capability
- RoHS Compliant







### MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DS</sub>	Drain to Source Voltage		-30	V
V <sub>GS</sub>	Gate to Source Voltage		±25	V
1	Drain Current -Continuous	(Note 1a)	-13	А
ID	-Pulsed		-65	A
	Power Dissipation for Single Operation	(Note 1a)	2.5	
$P_{D}$		(Note 1b)	1.2	W
		(Note 1c)	1.0	
T <sub>.I</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W

#### **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS6679AZ	FDS6679AZ	13"	12mm	2500 units

### Electrical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

**Parameter** 

Off Char	Off Characteristics						
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V	
$\frac{\Delta B_{VDSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25°C		-20		mV/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24V, V <sub>GS</sub> =0V			-1	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$			±10	μΑ	

**Test Conditions** 

Min

Тур

Max

Units

#### On Characteristics (Note 2)

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25°C		6.5		mV/°C
		$V_{GS} = -10V, I_D = -13A$		7.7	9.3	
rnov	Drain to Source On Resistance	$V_{GS} = -4.5V, I_D = -11A$		11.8	14.8	mΩ
r <sub>DS(on)</sub>	Diam to oddree on registance	$V_{GS} = -10V, I_D = -13A,$ $T_J = 125^{\circ}C$		10.7	13.4	11122
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5V, I_{D} = -13A$		55		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ - 45\\ \\ - 0\\	2890	3845	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz	500	665	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 1101112	495	745	pF

#### **Switching Characteristics (Note 2)**

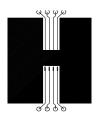
t <sub>d(on)</sub>	Turn-On Delay Time	., .=., .	13	24	ns
t <sub>r</sub>	Rise Time	$V_{DD} = -15V, I_{D} = -1A$ $V_{GS} = -10V, R_{GS} = 6\Omega$	15	27	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = -10V, K <sub>GS</sub> = 6£2	210	336	ns
t <sub>f</sub>	Fall Time		92	148	ns
Qg	Total Gate Charge	$V_{DS} = -15V, V_{GS} = -10V,$ $I_{D} = -13A$	68	96	nC
$Q_g$	Total Gate Charge	\\ 45\\\\ 5\\	38	54	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = -15V, V_{GS} = -5V,$ $I_{D} = -13A$	10		nC
$Q_{gd}$	Gate to Drain Charge	ID = 10A	17		nC

#### **Drain-Source Diode Characteristic**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_{S} = -2.1A$	-0.7	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	$I_F = -13A$ , $di/dt = 100A/\mu s$		40	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$I_F = -13A$ , di/dt = 100A/ $\mu$ s		-31	nC

#### Notes

13 R<sub>8,IA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>8,IC</sub> is guaranteed by design while R<sub>8CA</sub> is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)105°C/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

Scale 1:1 on letter size paper

- 2: Pulse Test:Pulse Width <300µs, Duty Cycle <2.0%
- 3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

#### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

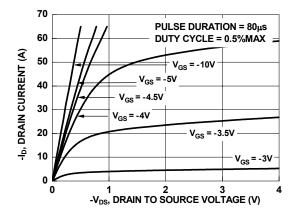


Figure 1. On Region Characteristics

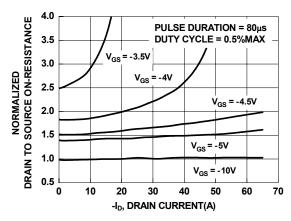


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

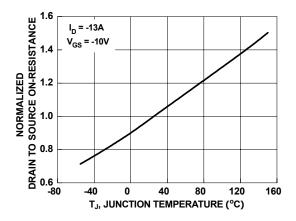


Figure 3. Normalized On Resistance vs Junction Temperature

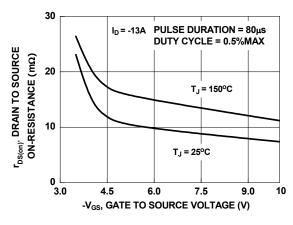


Figure 4. On-Resistance vs Gate to Source Voltage

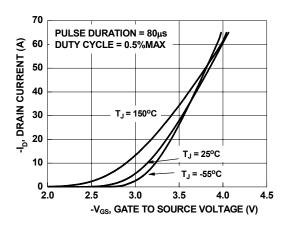


Figure 5. Transfer Characteristics

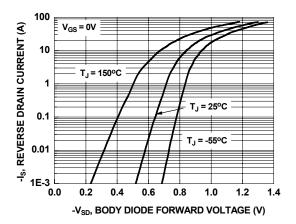


Figure 6. Source to Drain Diode Forward Voltage vs Source Current



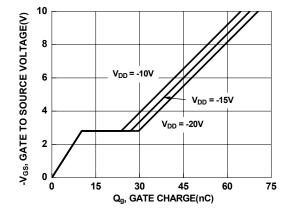


Figure 7. Gate Charge Characteristics

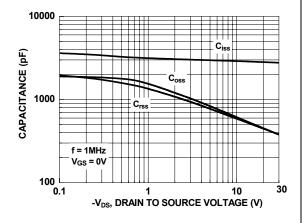


Figure 8. Capacitance vs Drain to Source Voltage

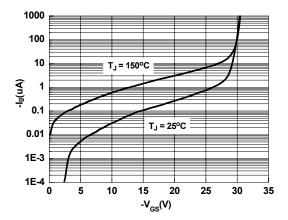


Figure 9.  $I_g vs V_{GS}$ 

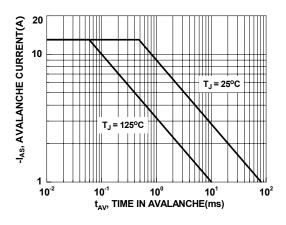


Figure 10. Unclamped Inductive Switching Capability

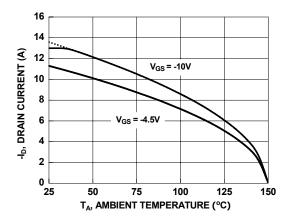


Figure 11. Maximum Continuous Drain Current vs
Ambient Temperature

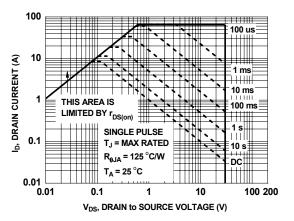


Figure 12. Forward Bias Safe Operating Area



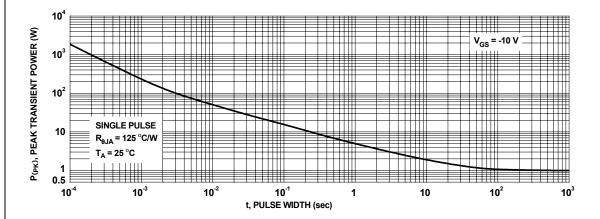


Figure 13. Single Pulse Maximum Power Dissipation

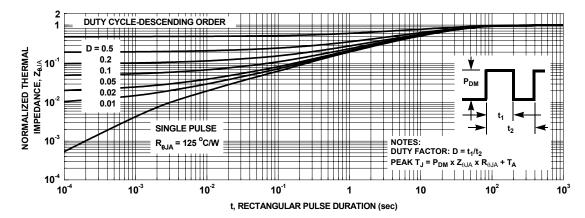


Figure 14. Junction-to-Ambient Transient Thermal Response Curve





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