



# STN3NF06L

N-channel 60 V, 0.07  $\Omega$ , 4 A, SOT-223  
STripFET™ II Power MOSFET

## Features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max	I <sub>D</sub>
STN3NF06L	60 V	< 0.1 $\Omega$	4 A

- Exceptional dv/dt capability
- Avalanche rugged technology
- 100% avalanche tested
- Low threshold drive

## Application

- Switching applications

## Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

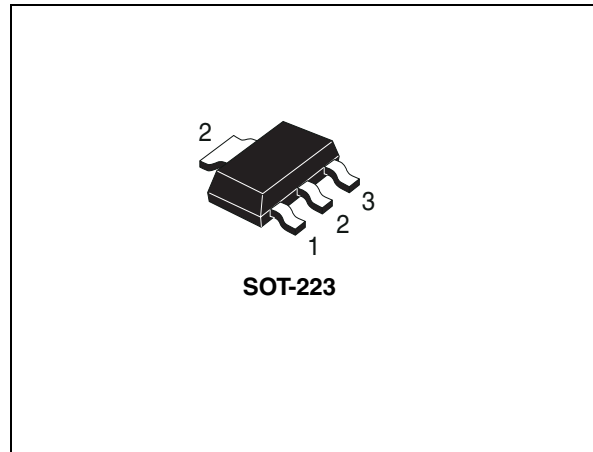


Figure 1. Internal schematic diagram

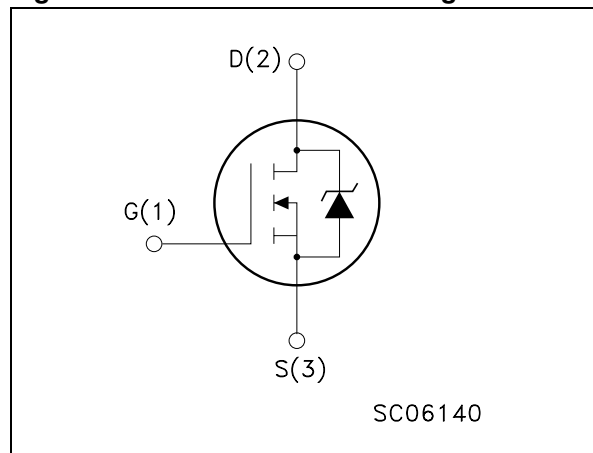


Table 1. Device summary

Order code	Marking	Package	Packaging
STN3NF06L	3NF06L	SOT-223	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60	V
$V_{GS}$	Gate-source voltage	$\pm 16$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.9	A
$I_{DM}^{(2)}$	Drain current (pulsed)	16	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	3.3	W
	Derating factor	0.026	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	200	mJ
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Current limited by the package
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 3\text{ A}$ ,  $di/dt \leq 150\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$
4. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 4\text{ A}$ ,  $V_{DD} = 30\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-PCB <sup>(1)</sup> max	38	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-PCB <sup>(2)</sup> max	100	$^\circ\text{C}/\text{W}$
$T_l^{(3)}$	Maximum lead temperature for soldering purpose typ	260	$^\circ\text{C}$

1. When Mounted on FR-4 board with 1 inch<sup>2</sup> pad, 2 oz. of Cu. and  $t < 10\text{ sec.}$
2. When mounted on minimum recommended footprint
3. for 10 sec. 1.6 mm from case

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating @ } 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1		2.8	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.5\text{ A}$ $V_{GS} = 5\text{ V}$ , $I_D = 1.5\text{ A}$		0.07 0.085	0.10 0.12	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 1.5\text{ A}$		3		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		340 63 30		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 48\text{ V}$ , $I_D = 3\text{ A}$ $V_{GS} = 5\text{ V}$ (see Figure 15)		7 1.5 2.8	9	nC nC nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time rise time	$V_{DD} = 30\text{ V}$ , $I_D = 1.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 5\text{ V}$ (see Figure 14)		9 25		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time fall time	$V_{DD} = 30\text{ V}$ , $I_D = 1.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 5\text{ V}$ (see Figure 14)		20 10		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current				4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=4\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=25\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 16)</i>		50		ns
$Q_{rr}$	Reverse recovery charge			88		nC
$I_{RRM}$	Reverse recovery current			3.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

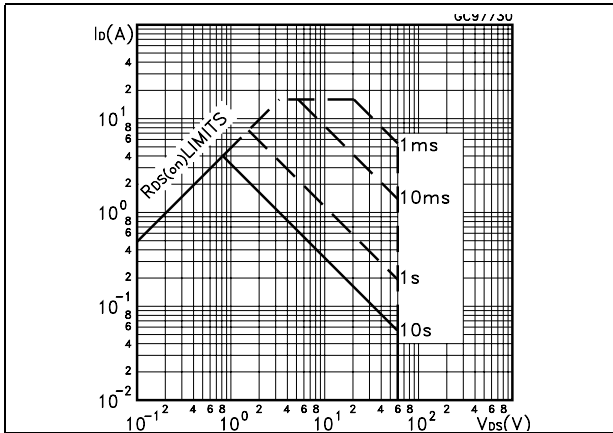


Figure 3. Thermal impedance

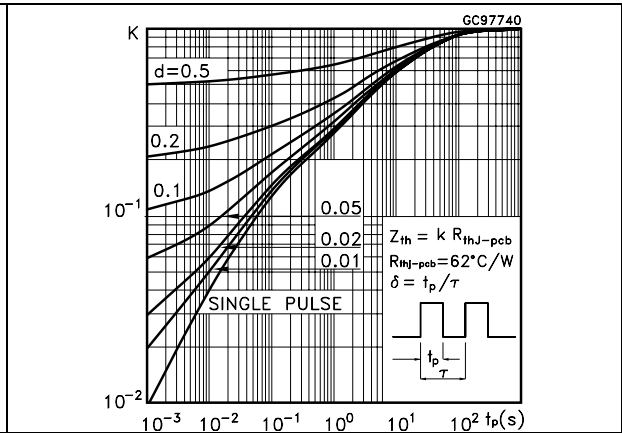


Figure 4. Output characteristics

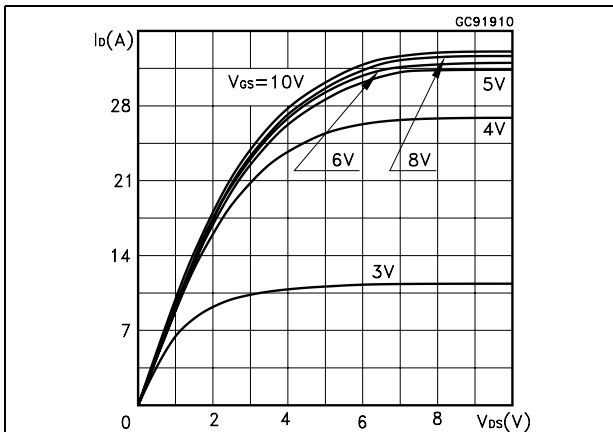


Figure 5. Transfer characteristics

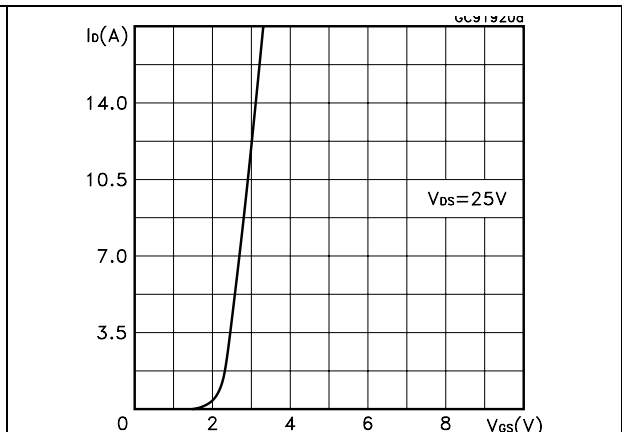


Figure 6. Transconductance

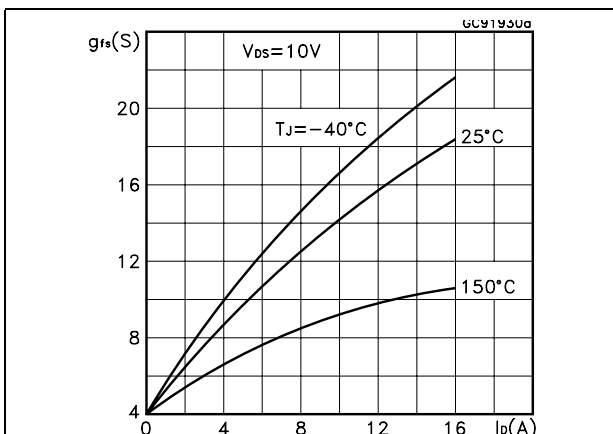


Figure 7. Static drain-source on resistance

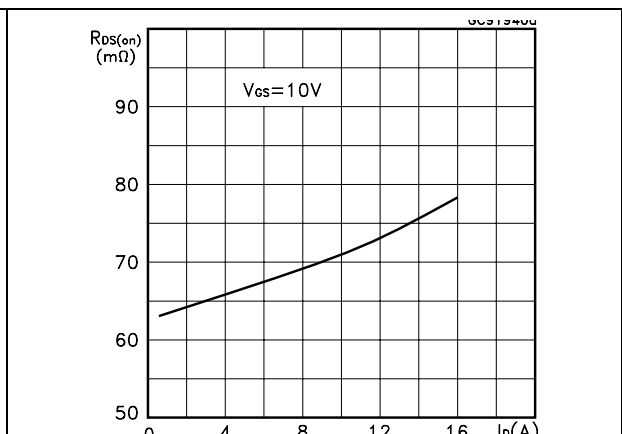


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

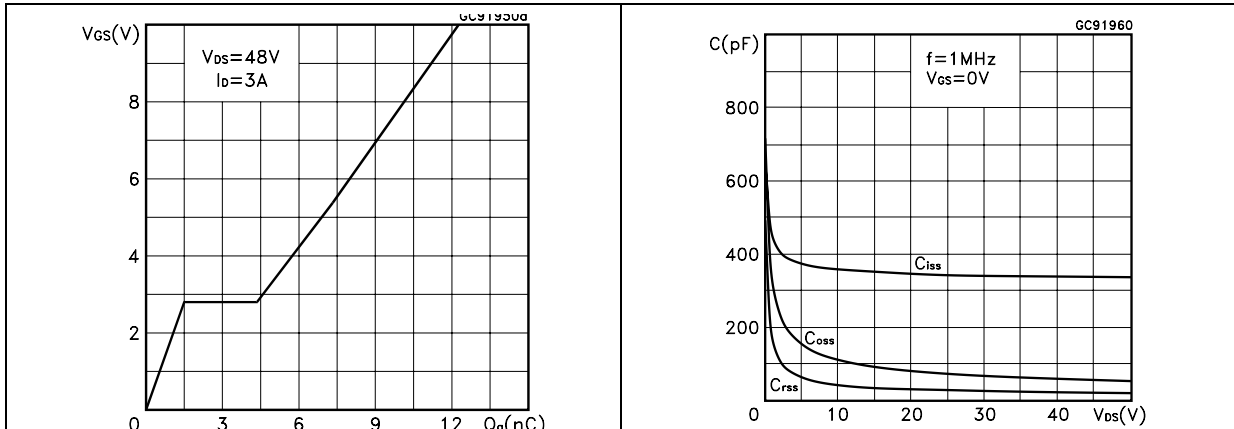


Figure 10. Normalized gate threshold voltage vs. temperature

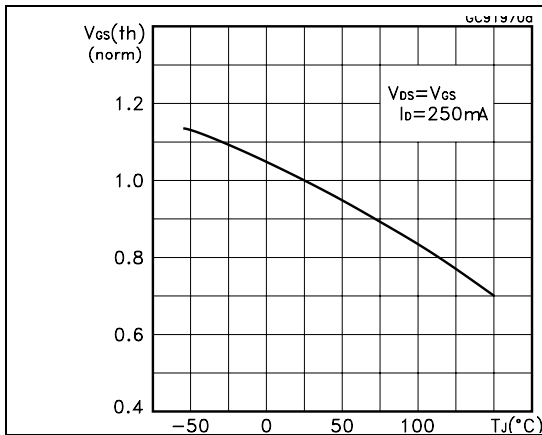


Figure 11. Normalized on resistance vs. temperature

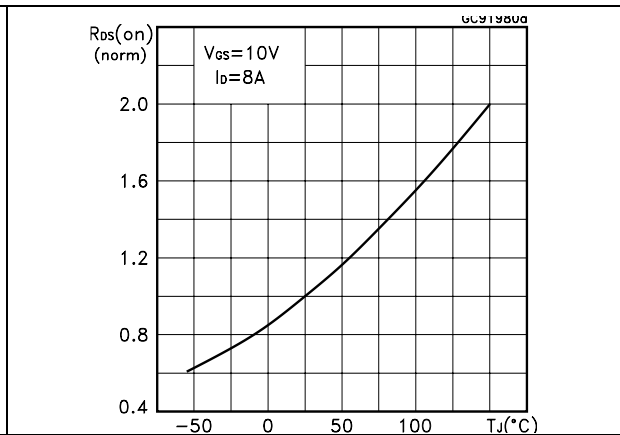


Figure 12. Source-drain diode forward characteristics

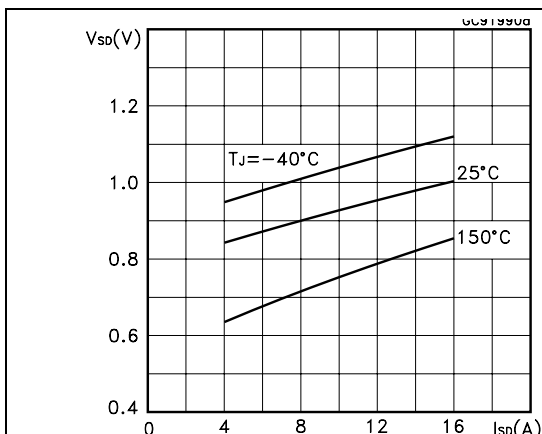
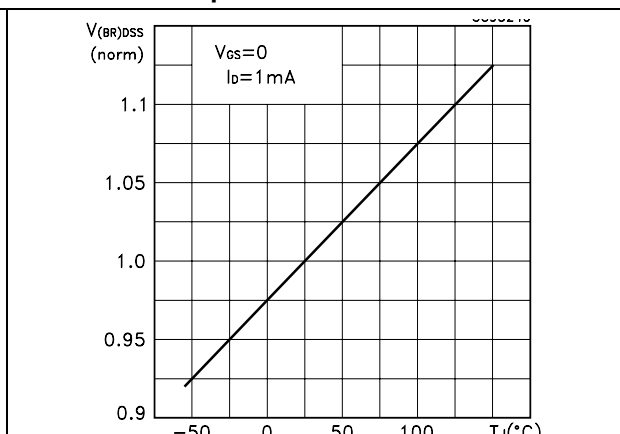


Figure 13. Normalized breakdown voltage vs. temperature



### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

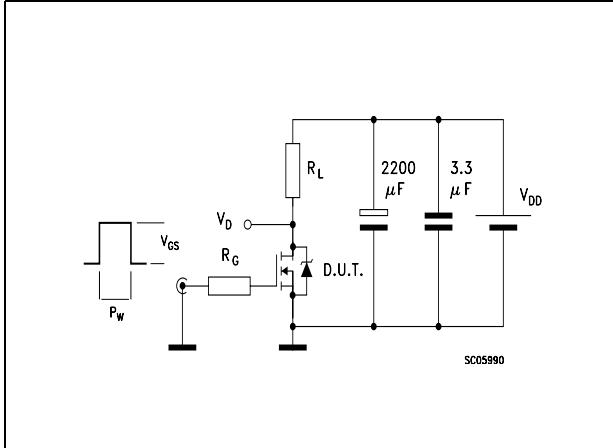


Figure 15. Gate charge test circuit

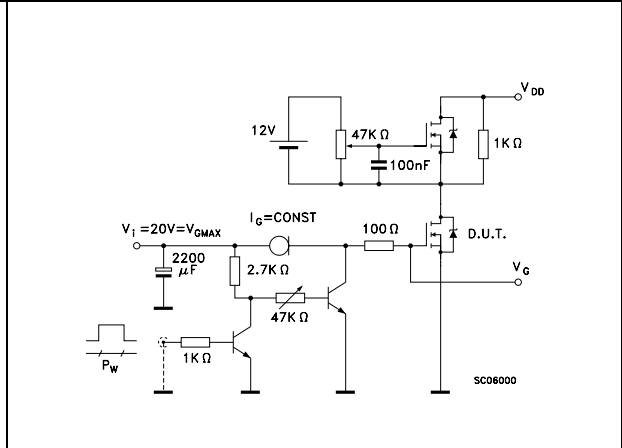


Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped Inductive load test circuit

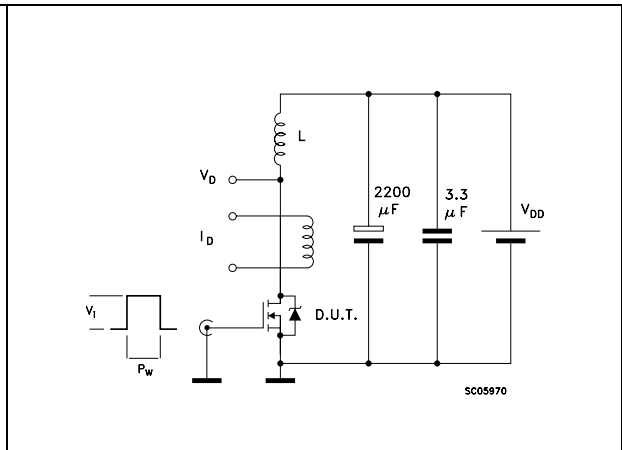


Figure 18. Unclamped inductive waveform

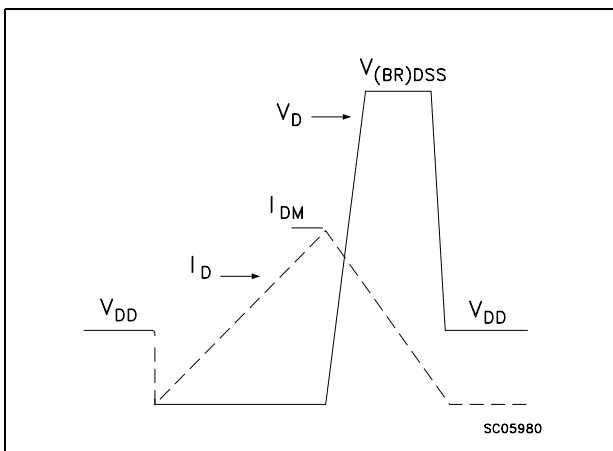
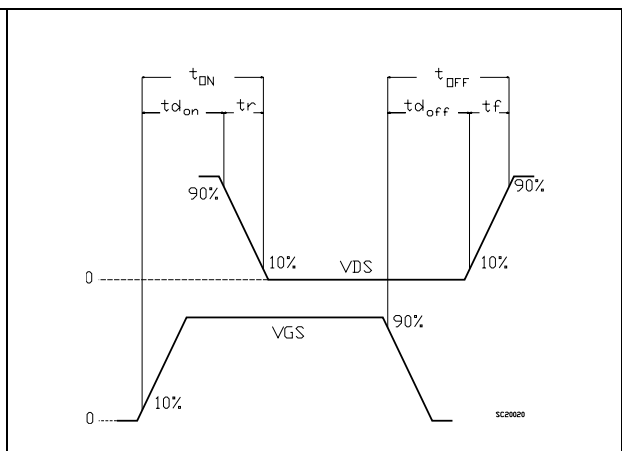


Figure 19. Switching time waveform



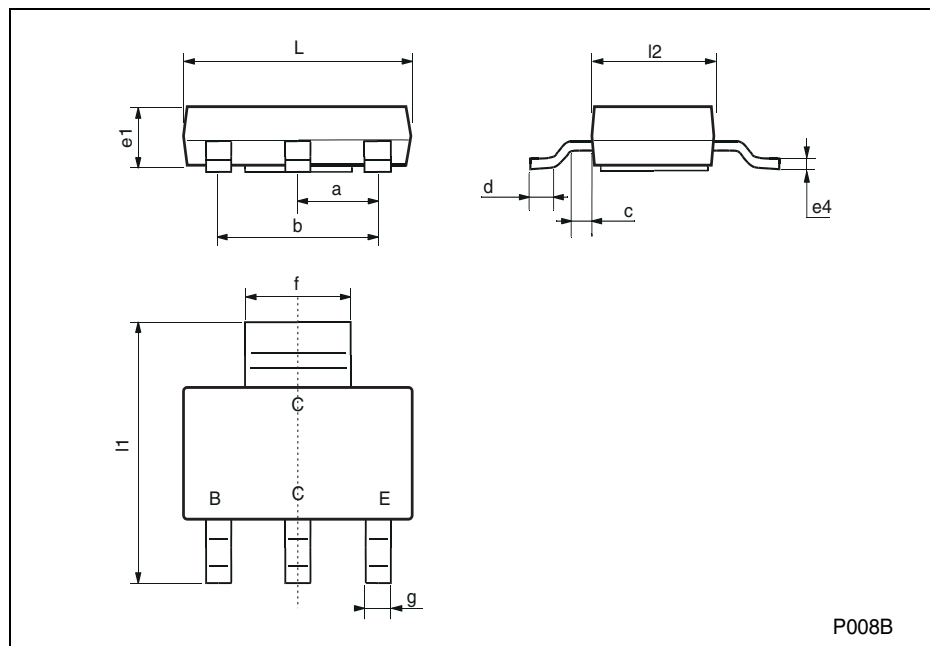


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**SOT-223 MECHANICAL DATA**

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a	2.27	2.3	2.33	89.4	90.6	91.7
b	4.57	4.6	4.63	179.9	181.1	182.3
c	0.2	0.4	0.6	7.9	15.7	23.6
d	0.63	0.65	0.67	24.8	25.6	26.4
e1	1.5	1.6	1.7	59.1	63	66.9
e4			0.32			12.6
f	2.9	3	3.1	114.2	118.1	122.1
g	0.67	0.7	0.73	26.4	27.6	28.7
l1	6.7	7	7.3	263.8	275.6	287.4
l2	3.5	3.5	3.7	137.8	137.8	145.7
L	6.3	6.5	6.7	248	255.9	263.8



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
21-Jun-2004	5	Complete version.
04-Oct-2006	6	New template, no content change.
01-Feb-2007	7	Typo mistake on <a href="#">Table 2</a> .
12-Jun-2008	8	Corrected marking on <a href="#">Table 1</a>

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