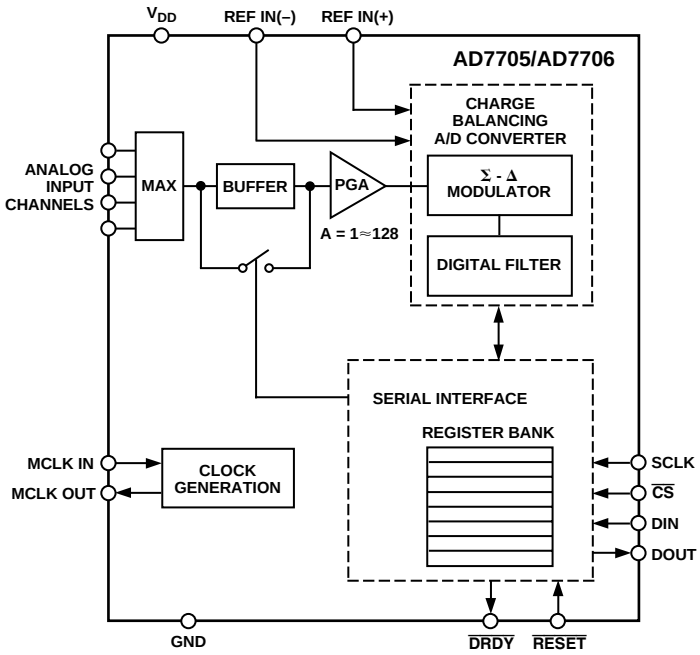
3 V/5 V, 1 mW 2-/3-Channel 16-Bit, Sigma-Delta ADCs

AD7705/AD7706*

FEATURES

AD7705: Two Fully Differential Input Channel ADCs
AD7706: Three Pseudo Differential Input Channel ADCs
16 Bits No Missing Codes
0.003% Nonlinearity
Programmable Gain Front End
Gains from 1 to 128
Three-Wire Serial Interface
SPI™, QSPI™, MICROWIRE™ and DSP Compatible
Schmitt Trigger Input on SCLK
Ability to Buffer the Analog Input
2.7 V to 3.3 V or 4.75 V to 5.25 V Operation
Power Dissipation 1 mW max @ 3 V
Standby Current 8 μA max
16-Lead DIP, 16-Lead SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7705/AD7706 are complete analog front ends for low frequency measurement applications. These two-/three-channel devices can accept low level input signals directly from a transducer and produce a serial digital output. They employ a sigma-delta conversion technique to realize up to 16 bits of no missing codes performance. The selected input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via an on-chip control register allowing adjustment of the filter cutoff and output update rate.

The AD7705/AD7706 operate from a single 2.7 V to 3.3 V or 4.75 V to 5.25 V supply. The AD7705 features two fully differential analog input channels while the AD7706 features three pseudo differential input channels. Both devices feature a differential reference input. Input signal ranges of 0 mV to +20 mV through 0 V to +2.5 V can be incorporated on both devices when operating with a V_{DD} of 5 V and a reference of 2.5 V. They can also handle bipolar input signal ranges of ±20 mV through ±2.5 V, which are referenced to the AIN(–) inputs on the AD7705 and to the COMMON input on the AD7706. The AD7705/AD7706, with 3 V supply and a 1.225 V reference, can handle unipolar input signal ranges of 0 mV to +10 mV through 0 V to +1.225 V. Its bipolar input signal ranges are ±10 mV through ±1.225 V. The AD7705/AD7706 thus perform all signal conditioning and conversion for a two- or three-channel system.

The AD7705/AD7706 are ideal for use in smart, microcontroller or DSP-based systems. They feature a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and update rate selection can be configured in software using the input serial port. The part contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 20 μW typ. These parts are available in a 16-lead, 0.3 inch-wide, plastic dual-in-line package (DIP), a 16-lead wide body (0.3 inch) small outline (SOIC) package and also a low profile 16-lead TSSOP.

PRODUCT HIGHLIGHTS

1. The AD7705/AD7706 consumes less than 1 mW at 3 V supplies and 1 MHz master clock, making it ideal for use in low power systems. Standby current is less than 8 μA.
2. The programmable gain input allows the AD7705/AD7706 to accept input signals directly from a strain gage or transducer, removing a considerable amount of signal conditioning.
3. The AD7705/AD7706 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems.
4. The part features excellent static performance specifications with 16 bits, no missing codes, ±0.003% accuracy and low rms noise (<600 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.

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AD7705/AD7706–SPECIFICATIONS (V_{DD} = +3 V or 5 V, REF IN(+) = +1.225 V with V_{DD} = 3 V and +2.5 V with V_{DD} = 5 V; REF IN(–) = GND; MCLK IN = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
No Missing Codes	16	Bits min	Guaranteed by Design. Filter Notch < 60 Hz
Output Noise	See Tables I and III		Depends on Filter Cutoffs and Selected Gain
Integral Nonlinearity[2]	±0.003	% of FSR max	Filter Notch < 60 Hz. Typically ±0.0003%
Unipolar Offset Error	See Note 3		
Unipolar Offset Drift[4]	0.5	µV/°C typ	
Bipolar Zero Error	See Note 3		
Bipolar Zero Drift[4]	0.5	µV/°C typ	For Gains 1, 2 and 4
	0.1	µV/°C typ	For Gains 8, 16, 32, 64 and 128
Positive Full-Scale Error[5]	See Note 3		
Full-Scale Drift[4, 6]	0.5	µV/°C typ	
Gain Error[7]	See Note 3		
Gain Drift[4, 8]	0.5	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.003	% of FSR typ	Typically ±0.001%
Bipolar Negative Full-Scale Drift[4]	1	µV/°C typ	For Gains of 1 to 4
	0.6	µV/°C typ	For Gains of 8 to 128
ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN Unless Noted
Input Common-Mode Rejection (CMR)[2]			
V_{DD} = 5 V			
Gain = 1	96	dB typ	
Gain = 2	105	dB typ	
Gain = 4	110	dB typ	
Gain = 8→128	130	dB typ	
V_{DD} = 3 V			
Gain = 1	105	dB typ	
Gain = 2	110	dB typ	
Gain = 4	120	dB typ	
Gain = 8→128	130	dB typ	
Normal-Mode 50 Hz Rejection[2]	98	dB typ	For Filter Notches of 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Normal-Mode 60 Hz Rejection[2]	98	dB typ	For Filter Notches of 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 50 Hz Rejection[2]	150	dB typ	For Filter Notches of 25 Hz, 50 Hz, $\pm 0.02 \times f_{NOTCH}$
Common-Mode 60 Hz Rejection[2]	150	dB typ	For Filter Notches of 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Absolute/Common-Mode REF IN Voltage[2]	GND to V_{DD}	V min to V max	
Absolute/Common-Mode AIN Voltage[2, 9]	GND – 30 mV	V min	BUF Bit of Setup Register = 0
	V_{DD} + 30 mV	V max	
Absolute/Common-Mode AIN Voltage[2, 9]	GND + 50 mV	V min	BUF Bit of Setup Register = 1
	V_{DD} – 1.5 V	V max	
AIN DC Input Current[2]	1	nA max	
AIN Sampling Capacitance[2]	10	pF max	
AIN Differential Voltage Range[10]	0 to $+V_{REF}/GAIN$[11]	nom	Unipolar Input Range (B/U Bit of Setup Register = 1)
	$\pm V_{REF}/GAIN$	nom	Bipolar Input Range (B/U Bit of Setup Register = 0)
AIN Input Sampling Rate, f_S	$GAIN \times f_{CLKIN}/64$		For Gains of 1 to 4
	$f_{CLKIN}/8$		For Gains of 8 to 128
Reference Input Range			
REF IN(+) – REF IN(–) Voltage	1/1.75	V min/max	V_{DD} = 2.7 V to 3.3 V. V_{REF} = 1.225 ± 1% for Specified Performance
REF IN(+) – REF IN(–) Voltage	1/3.5	V min/max	V_{DD} = 4.75 V to 5.25 V. V_{REF} = 2.5 ± 1% for Specified Performance
REF IN Input Sampling Rate, f_S	$f_{CLKIN}/64$		
LOGIC INPUTS			
Input Current			
All Inputs Except MCLK IN	±1	µA max	Typically ±20 nA
MCLK	±10	µA max	Typically ±2 µA
All Inputs Except SCLK and MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	V_{DD} = 3 V and 5 V
SCLK Only (Schmitt Triggered Input)			V_{DD} = 5 V NOMINAL
V_{T+}	1.4/3	V min/V max	
V_{T-}	0.8/1.4	V min/V max	
$V_{T+} - V_{T-}$	0.4/0.8	V min/V max	
SCLK Only (Schmitt Triggered Input)			V_{DD} = 3 V NOMINAL
V_{T+}	1/2.5	V min/V max	
V_{T-}	0.4/1.1	V min/V max	
$V_{T+} - V_{T-}$	0.375/0.8	V min/V max	
MCLK IN Only			V_{DD} = 5 V NOMINAL
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
MCLK IN Only			V_{DD} = 3 V NOMINAL
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	

Parameter	B Version[1]	Units	Conditions/Comments
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA Except for MCLK OUT.[12] V_{DD} = 5 V.
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 100 μA Except for MCLK OUT.[12] V_{DD} = 3 V.
V_{OH}, Output High Voltage	4	V min	I_{SOURCE} = 200 μA Except for MCLK OUT.[12] V_{DD} = 5 V.
V_{OH}, Output High Voltage	V_{DD}–0.6	V min	I_{SOURCE} = 100 μA Except for MCLK OUT.[12] V_{DD} = 3 V.
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[13]	9	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
SYSTEM CALIBRATION			
Positive Full-Scale Calibration Limit[14]	$(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (1 to 128)
Negative Full-Scale Calibration Limit[14]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (1 to 128)
Offset Calibration Limit[14]	$-(1.05 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (1 to 128)
Input Span[15]	$(0.8 \times V_{REF})/GAIN$	V min	GAIN Is the Selected PGA Gain (1 to 128)
	$(2.1 \times V_{REF})/GAIN$	V max	GAIN Is the Selected PGA Gain (1 to 128)
POWER REQUIREMENTS			
V_{DD} Voltage	+2.7 to +3.3	V min to V max	For Specified Performance
Power Supply Currents[16]			Digital I/Ps = 0 V or V_{DD}. External MCLK IN and CLK DIS = 1
	0.32	mA max	BUF Bit = 0. f_{CLKIN} = 1 MHz. Gains of 1 to 128
	0.6	mA max	BUF Bit = 1. f_{CLKIN} = 1 MHz. Gains of 1 to 128
	0.4	mA max	BUF Bit = 0. f_{CLKIN} = 2.4576 MHz. Gains of 1 to 4
	0.6	mA max	BUF Bit = 0. f_{CLKIN} = 2.4576 MHz. Gains of 8 to 128
	0.7	mA max	BUF Bit = 1. f_{CLKIN} = 2.4576 MHz. Gains of 1 to 4
	1.1	mA max	BUF Bit = 1. f_{CLKIN} = 2.4576 MHz. Gains of 8 to 128
V_{DD} Voltage	+4.75 to +5.25	V min to V max	For Specified Performance
Power Supply Currents[16]			Digital I/Ps = 0 V or V_{DD}. External MCLK IN and CLK DIS = 1.
	0.45	mA max	BUF Bit = 0. f_{CLKIN} = 1 MHz. Gains of 1 to 128
	0.7	mA max	BUF Bit = 1. f_{CLKIN} = 1 MHz. Gains of 1 to 128
	0.6	mA max	BUF Bit = 0. f_{CLKIN} = 2.4576 MHz. Gains of 1 to 4
	0.85	mA max	BUF Bit = 0. f_{CLKIN} = 2.4576 MHz. Gains of 8 to 128
	0.9	mA max	BUF Bit = 1. f_{CLKIN} = 2.4576 MHz. Gains of 1 to 4
	1.3	mA max	BUF Bit = 1. f_{CLKIN} = 2.4576 MHz. Gains of 8 to 128
Standby (Power-Down) Current[17]	16	μA max	External MCLK IN = 0 V or V_{DD}. V_{DD} = 5 V. See Figure 9
	8	μA max	External MCLK IN = 0 V or V_{DD}. V_{DD} = 3 V
Power Supply Rejection[18]	See Note 19	dB typ	

NOTES

[1]Temperature range as follows: B Version, –40°C to +85°C.

[2]These numbers are established from characterization or design at initial product release.

[3]A calibration is effectively a conversion so these errors will be of the order of the conversion noise shown in Tables I and III. This applies after calibration at the temperature of interest.

[4]Recalibration at any temperature will remove these drift errors.

[5]Positive Full-Scale Error includes Zero-Scale Errors (Unipolar Offset Error or Bipolar Zero Error) and applies to both unipolar and bipolar input ranges.

[6]Full-Scale Drift includes Zero-Scale Drift (Unipolar Offset Drift or Bipolar Zero Drift) and applies to both unipolar and bipolar input ranges.

[7]Gain Error does not include Zero-Scale Errors. It is calculated as Full-Scale Error–Unipolar Offset Error for unipolar ranges and Full-Scale Error–Bipolar Zero Error for bipolar ranges.

[8]Gain Error Drift does not include Unipolar Offset Drift/Bipolar Zero Drift. It is effectively the drift of the part if zero scale calibrations only were performed.

[9]This common-mode voltage range is allowed provided that the input voltage on analog inputs does not go more positive than V_{DD} + 30 mV or go more negative than GND – 30 mV. Parts are functional with voltages down to GND – 200 mV, but with increased leakage at high temperature.

[10]The analog input voltage range on AIN(+) is given here with respect to the voltage on AIN(–) on the AD7705 and is given with respect to the COMMON input on the AD7706. The absolute voltage on the analog inputs should not go more positive than V_{DD} + 30 mV, or go more negative than GND – 30 mV for specified performance, input voltages of GND – 200 mV can be accommodated, but with increased leakage at high temperature.

[11]V_{REF} = REF IN(+) – REF IN(–).

[12]These logic output levels apply to the MCLK OUT only when it is loaded with one CMOS load.

[13]Sample tested at +25°C to ensure compliance.

[14]After calibration, if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, the device will output all 0s.

[15]These calibration and span limits apply provided the absolute voltage on the analog inputs does not exceed V_{DD} + 30 mV or go more negative than GND – 30 mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.

[16]When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the V_{DD} current and power dissipation will vary depending on the crystal or resonator type (see Clocking and Oscillator Circuit section).

[17]If the external master clock continues to run in standby mode, the standby current increases to 150 μA typical at 5 V and 75 μA at 3 V. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode and the power dissipation depends on the crystal or resonator type (see Standby Mode section).

[18]Measured at dc and applies in the selected passband. PSRR at 50 Hz will exceed 120 dB with filter notches of 25 Hz or 50 Hz. PSRR at 60 Hz will exceed 120 dB with filter notches of 20 Hz or 60 Hz.

[19]PSRR depends on both gain and V_{DD}.

Gain	1	2	4	8–128
V_{DD} = 3 V	86	78	85	93
V_{DD} = 5 V	90	78	84	91

Specifications subject to change without notice.

AD7705/AD7706

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +2.7 V to +5.25 V; GND = 0 V; f_{CLKIN} = 2.4576 MHz; Input Logic 0 = 0 V, Logic 1 = V_{DD} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master Clock Frequency: Crystal Oscillator or Externally Supplied
	2.5	MHz max	for Specified Performance
$t_{CLKIN\ LO}$	0.4 × t_{CLKIN}	ns min	Master Clock Input Low Time. t_{CLKIN} = 1/f_{CLKIN}
$t_{CLKIN\ HI}$	0.4 × t_{CLKIN}	ns min	Master Clock Input High Time
t_1	500 × t_{CLKIN}	ns nom	$\overline{DRDY}$ High Time
t_2	100	ns min	$\overline{RESET}$ Pulsewidth
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ Setup Time
t_4	120	ns min	$\overline{CS}$ Falling Edge to SCLK Rising Edge Setup Time
t_5[5]	0	ns min	SCLK Falling Edge to Data Valid Delay
	80	ns max	V_{DD} = +5 V
	100	ns max	V_{DD} = +3.0 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Rising Edge
	60	ns max	V_{DD} = +5 V
	100	ns max	V_{DD} = +3.0 V
t_{10}	100	ns max	SCLK Falling Edge to $\overline{DRDY}$ High[7]
Write Operation			
t_{11}	120	ns min	$\overline{CS}$ Falling Edge to SCLK Rising Edge Setup Time
t_{12}	30	ns min	Data Valid to SCLK Rising Edge Setup Time
t_{13}	20	ns min	Data Valid to SCLK Rising Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 16 and 17.

[3]f_{CLKIN} Duty Cycle range is 45% to 55%. f_{CLKIN} must be supplied whenever the AD7705/AD7706 is not in Standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.

[4]The AD7705/AD7706 is production tested with f_{CLKIN} at 2.4576 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.

[5]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[7]$\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

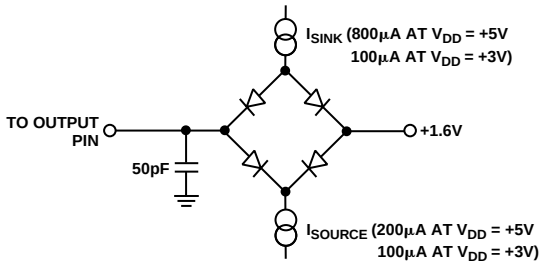


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Analog Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 105°C/W
  Lead Temperature, (Soldering, 10 sec) . . . . . +260°C
SOIC Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
SSOP Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 139°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . >4000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	V_{DD} Supply	Temperature Range	Package Description	Package Options
AD7705BN	2.7 V to 5.25 V	–40°C to +85°C	Plastic DIP	N-16
AD7705BR	2.7 V to 5.25 V	–40°C to +85°C	SOIC	R-16
AD7705BRU	2.7 V to 5.25 V	–40°C to +85°C	TSSOP	RU-16
EVAL-AD7705EB		Evaluation Board		
AD7706BN	2.7 V to 5.25 V	–40°C to +85°C	Plastic DIP	N-16
AD7706BR	2.7 V to 5.25 V	–40°C to +85°C	SOIC	R-16
AD7706BRU	2.7 V to 5.25 V	–40°C to +85°C	TSSOP	RU-16
EVAL-AD7706EB		Evaluation Board		

PIN CONFIGURATIONS

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock. Schmitt-Triggered Logic Input. An external serial clock is applied to this input to access serial data from the AD7705/AD7706. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7705/AD7706 in smaller batches of data.
2	MCLK IN	Master Clock signal for the device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The part can be operated with clock frequencies in the range 500 kHz to 5 MHz.
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuitry and is capable of driving one CMOS load. If the user does not require it, this MCLK OUT can be turned off via the CLK DIS bit of the Clock Register. This ensures that the part is not burning unnecessary power driving capacitive loads on MCLK OUT.
4	$\overline{CS}$	Chip Select. Active low Logic Input used to select the AD7705/AD7706. With this input hard-wired low, the AD7705/AD7706 can operate in its three-wire interface mode with SCLK, DIN and DOUT used to interface to the device. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7705/AD7706.
5	$\overline{RESET}$	Logic Input. Active low input that resets the control logic, interface logic, calibration coefficients, digital filter and analog modulator of the part to power-on status.
6	AIN2(+)[AIN1]	AD7705: Positive input of the differential Analog Input Channel 2. AD7706: Analog Input Channel 1.
7	AIN1(+)[AIN2]	AD7705: Positive input of the differential Analog Input Channel 1. AD7706: Analog Input Channel 2.
8	AIN1(–)[COMMON]	AD7705: Negative input of the differential Analog Input Channel 1. AD7706: COMMON Input. Analog inputs for Channels 1, 2 and 3 are referenced to this input.
9	REF IN(+)	Reference Input. Positive input of the differential Reference Input to the AD7705/AD7706. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between V_{DD} and GND.

Pin No.	Mnemonic	Function
10	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7705/AD7706. The REF IN(–) can lie anywhere between V_{DD} and GND provided REF IN(+) is greater than REF IN(–).
11	AIN2(–)[AIN3]	AD7705: Negative input of the differential analog Input Channel 2. AD7706: Analog Input Channel 3.
12	$\overline{\text{DRDY}}$	Logic Output. A logic low on this output indicates that a new output word is available from the AD7705/AD7706 data register. The $\overline{\text{DRDY}}$ pin will return high upon completion of a read operation of a full output word. If no data read has taken place between output updates, the $\overline{\text{DRDY}}$ line will return high for 500 × $t_{CLK\ IN}$ cycles prior to the next output update. While $\overline{\text{DRDY}}$ is high, a read operation should neither be attempted nor in progress to avoid reading from the data register as it is being updated. The $\overline{\text{DRDY}}$ line will return low again when the update has taken place. $\overline{\text{DRDY}}$ is also used to indicate when the AD7705/AD7706 has completed its on-chip calibration sequence.
13	DOUT	Serial Data Output with serial data being read from the output shift register on the part. This output shift register can contain information from the setup register, communications register, clock register or data register, depending on the register selection bits of the Communications Register.
14	DIN	Serial Data Input with serial data being written to the input shift register on the part. Data from this input shift register is transferred to the setup register, clock register or communications register, depending, on the register selection bits of the Communications Register.
15	V_{DD}	Supply Voltage, +2.7 V to +5.25 V operation.
16	GND	Ground reference point for the AD7705/AD7706's internal circuitry.

OUTPUT NOISE (5 V OPERATION)

Table I shows the AD7705/AD7706 output rms noise for the selectable notch and –3 dB frequencies for the part, as selected by FS0 and FS1 of the Clock Register. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5 V and V_{DD} = 5 V. These numbers are typical and are generated at an analog input voltage of 0 V with the part used in either buffered or unbuffered mode. Table II meanwhile shows the output *peak-to-peak* noise for the selectable notch and –3 dB frequencies for the part. *It is important to note that these numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.* The numbers given are for bipolar input ranges with a V_{REF} of +2.5 V and for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLK DIV bit of the Clock Register set to 0.

Table I. Output RMS Noise vs. Gain and Output Update Rate @ 5 V

Filter First Notch and O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
60 Hz	15.72 Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
250 Hz	65.5 Hz	110	49	31	17	8	3.6	2.3	1.7
500 Hz	131 Hz	550	285	145	70	41	22	9.1	4.7
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
25 Hz	6.55 Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
100 Hz	26.2 Hz	110	49	31	17	8	3.6	2.3	1.7
200 Hz	52.4 Hz	550	285	145	70	41	22	9.1	4.7

Table II. Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V

Filter First Notch and O/P Data Rate	–3 dB Frequency	Typical Peak-to-Peak Resolution Bits Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	16	16	16	16	16	16	15	14
60 Hz	15.72 Hz	16	16	16	16	15	14	14	13
250 Hz	65.5 Hz	13	13	13	13	13	13	12	12
500 Hz	131 Hz	10	10	10	10	10	10	10	10
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	16	16	16	16	16	16	15	14
25 Hz	6.55 Hz	16	16	16	16	15	14	14	13
100 Hz	26.2 Hz	13	13	13	13	13	13	12	12
200 Hz	52.4 Hz	10	10	10	10	10	10	10	10

OUTPUT NOISE (3 V OPERATION)

Table III shows the AD7705/AD7706 output rms noise for the selectable notch and –3 dB frequencies for the part, as selected by FS0 and FS1 of the Clock Register. The numbers given are for the bipolar input ranges with a V_{REF} of +1.225 V and a V_{DD} = 3 V. These numbers are typical and are generated at an analog input voltage of 0 V with the part used in either buffered or unbuffered mode. Table II meanwhile shows the output *peak-to-peak* noise for the selectable notch and –3 dB frequencies for the part. *It is important to note that these numbers represent the resolution for which there will be no code flicker. They are not calculated based on rms noise but on peak-to-peak noise.* The numbers given are for bipolar input ranges with a V_{REF} of +1.225 V and for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLK DIV bit of the Clock Register set to 0.

Table III. Output RMS Noise vs. Gain and Output Update Rate @ 3 V

Filter First Notch and O/P Data Rate	–3 dB Frequency	Typical Output RMS Noise in μV Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
60 Hz	15.72 Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
250 Hz	65.5 Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
500 Hz	131 Hz	270	135	65	41	22	9.7	5.1	3.3
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
25 Hz	6.55 Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
100 Hz	26.2 Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
200 Hz	52.4 Hz	270	135	65	41	22	9.7	5.1	3.3

Table IV. Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 3 V

Filter First Notch and O/P Data Rate	–3 dB Frequency	Typical Peak-to-Peak Resolution in Bits Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
50 Hz	13.1 Hz	16	16	15	15	14	13	13	12
60 Hz	15.72 Hz	16	16	15	14	14	13	13	12
250 Hz	65.5 Hz	13	13	13	13	12	12	11	11
500 Hz	131 Hz	10	10	10	10	10	10	10	10
MCLK IN = 1 MHz									
20 Hz	5.24 Hz	16	16	15	15	14	13	13	12
25 Hz	6.55 Hz	16	16	15	14	14	13	13	12
100 Hz	26.2 Hz	13	13	13	13	12	12	11	11
200 Hz	52.4 Hz	10	10	10	10	10	10	10	10

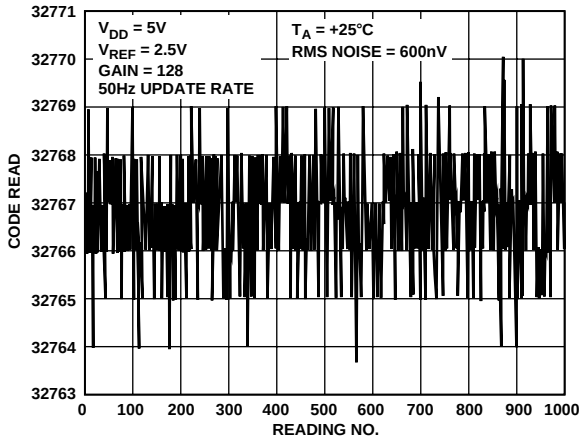


Figure 2. Typical Noise Plot @ Gain = 128 with 50 Hz Update Rate

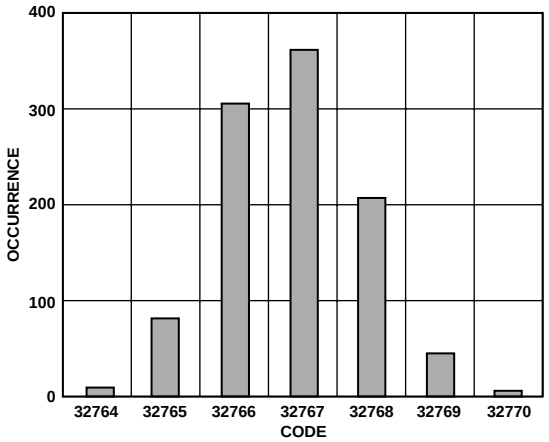


Figure 5. Histogram of Data in Figure 2

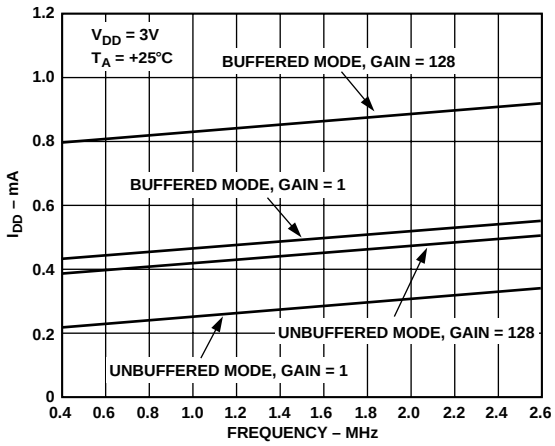


Figure 3. Typical I_{DD} vs. MCLKIN Frequency @ 3 V

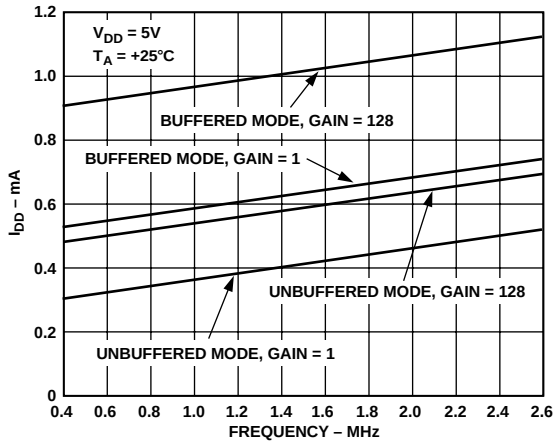


Figure 6. Typical I_{DD} vs. MCLKIN Frequency @ 5 V

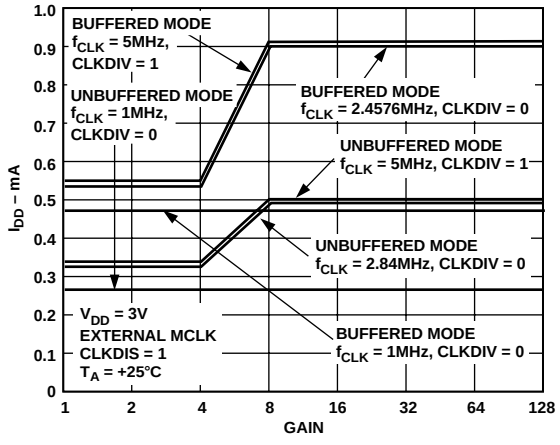


Figure 4. Typical I_{DD} vs. Gain and Clock Frequency @ 3 V

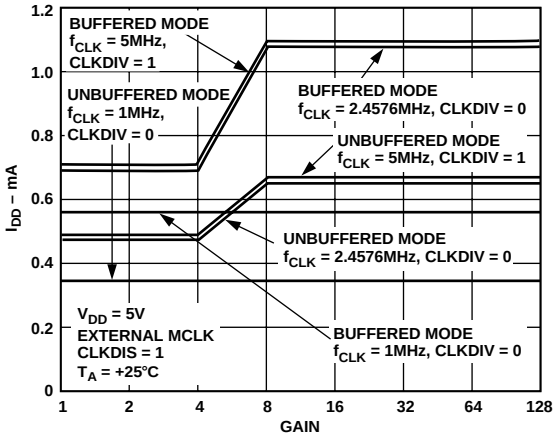


Figure 7. Typical I_{DD} vs. Gain and Clock Frequency @ 5 V

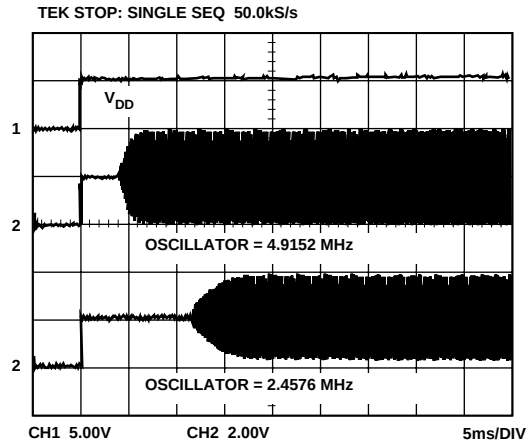


Figure 8. Typical Crystal Oscillator Power-Up Time

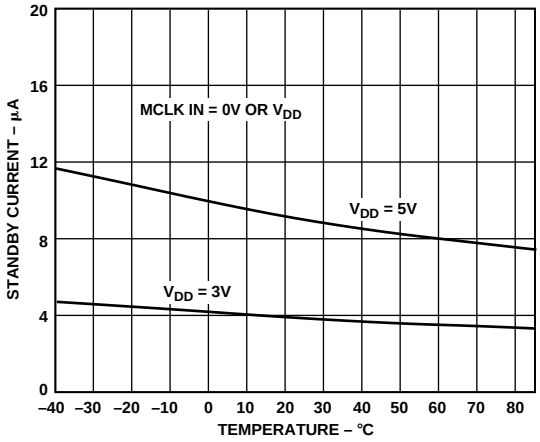


Figure 9. Standby Current vs. Temperature

ON-CHIP REGISTERS

The AD7705/AD7706 contains eight on-chip registers which can be accessed via the serial port of the part. The first of these is a Communications Register that controls the channel selection, decides whether the next operation is a read or write operation and also decides which register the next read or write operation accesses. All communications to the part must start with a write operation to the Communications Register. After power-on or $\overline{\text{RESET}}$, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any other register on the part (including the Communications Register itself and the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register. The Communications Register also controls the standby mode and channel selection and the $\overline{\text{DRDY}}$ status is also available by reading from the Communications Register. The second register is a Setup Register that determines calibration mode, gain setting, bipolar/unipolar operation and buffered mode. The third register is labelled the Clock Register and contains the filter selection bits and clock control bits. The fourth register is the Data Register from which the output data from the part is accessed. The final registers are the calibration registers which store channel calibration data. The registers are discussed in more detail in the following sections.

Communications Register (RS2, RS1, RS0 = 0, 0, 0)

The Communications Register is an 8-bit register from which data can either be read or to which data can be written. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation and to which register this operation takes place. Once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a $\overline{\text{RESET}}$, the AD7705/AD7706 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, if a write operation of sufficient duration (containing at least 32 serial clock cycles) takes place with DIN high, the AD7705 returns to this default state. Table V outlines the bit designations for the Communications Register.

Table V. Communications Register

0/$\overline{\text{DRDY}}$ (0)	RS2 (0)	RS1 (0)	RS0 (0)	R/$\overline{\text{W}}$ (0)	STBY (0)	CH1 (0)	CH0 (0)

0/$\overline{\text{DRDY}}$ — For a write operation, a "0" must be written to this bit so that the write operation to the Communications Register actually takes place. If a "1" is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a "0" is written to this bit. Once a "0" is written to this bit, the next seven bits will be loaded to the Communications Register. For a read operation, this bit provides the status of the $\overline{\text{DRDY}}$ flag from the part. The status of this bit is the same as the $\overline{\text{DRDY}}$ output pin.

RS2–RS0 — Register Selection Bits. These three bits select to which one of eight on-chip registers the next read or write operation takes place, as shown in Table VI, along with the register size. When the read or write operation to the selected register is complete, the part returns to where it is waiting for a write operation to the Communications Register. It does not remain in a state where it will continue to access the register.

Table VI. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register	8 Bits
0	0	1	Setup Register	8 Bits
0	1	0	Clock Register	8 Bits
0	1	1	Data Register	16 Bits
1	0	0	Test Register	8 Bits
1	0	1	No Operation	
1	1	0	Offset Register	24 Bits
1	1	1	Gain Register	24 Bits

R/$\overline{W}$ Read/$\overline{Write}$ Select. This bit selects whether the next operation is a read or write operation to the selected register. A "0" indicates a write cycle for the next operation to the appropriate register, while a "1" indicates a read operation from the appropriate register.

STBY Standby. Writing a "1" to this bit puts the part into its standby or power-down mode. In this mode, the part consumes only 10 μA of power supply current. The part retains its calibration coefficients and control word information when in STANDBY. Writing a "0" to this bit places the part in its normal operating mode.

CH1–CH0 Channel Select. These two bits select a channel for conversion or for access to the calibration coefficients as outlined in Table VII. Three pairs of calibration registers on the part are used to store the calibration coefficients following a calibration on a channel. They are shown in Tables VII for the AD7705 and Table VIII for the AD7706 to indicate which channel combinations have independent calibration coefficients. With CH1 at Logic 1 and CH0 at a Logic 0, the part looks at the AIN1(–) input internally shorted to itself on the AD7705 or at COMMON internally shorted to itself on the AD7706. This can be used as a test method to evaluate the noise performance of the part with no external noise sources. In this mode, the AIN1(–)/COMMON input should be connected to an external voltage within the allowable common-mode range for the part.

Table VII. Channel Selection for AD7705

CH1	CH0	AIN(+)	AIN(–)	Calibration Register Pair
0	0	AIN1(+)	AIN1(–)	Register Pair 0
0	1	AIN2(+)	AIN2(–)	Register Pair 1
1	0	AIN1(–)	AIN1(–)	Register Pair 0
1	1	AIN1(–)	AIN2(–)	Register Pair 2

Table VIII. Channel Selection for AD7706

CH1	CH0	AIN	Reference	Calibration Register Pair
0	0	AIN1	COMMON	Register Pair 0
0	1	AIN2	COMMON	Register Pair 1
1	0	COMMON	COMMON	Register Pair 0
1	1	AIN3	COMMON	Register Pair 2

Setup Register (RS2, RS1, RS0 = 0, 0, 1); Power-On/Reset Status: 01 Hex

The Setup Register is an eight bit register from which data can either be read or to which data can be written. Table IX outlines the bit designations for the Setup Register.

Table IX. Setup Register

MD1 (0)	MD0 (0)	G2 (0)	G1 (0)	G0 (0)	$\overline{B}$/U (0)	BUF (0)	FSYNC (1)

MD1	MD0	Operating Mode
0	0	Normal Mode: this is the normal mode of operation of the device whereby the device is performing normal conversions.
0	1	Self-Calibration: this activates self-calibration on the channel selected by CH1 and CH0 of the Communications Register. This is a one-step calibration sequence and when complete the part returns to Normal Mode with MD1 and MD0 returning to 0, 0. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this self-calibration is complete and a new valid word is available in the data register. The zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs and the full-scale calibration is performed at the selected gain on an internally-generated V_{REF}/Selected Gain.
1	0	Zero-Scale System Calibration: this activates zero scale system calibration on the channel selected by CH1 and CH0 of the Communications Register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this zero-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to Normal Mode with MD1 and MD0 returning to 0, 0.
1	1	Full-Scale System Calibration: this activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. Once again, the $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this full-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to Normal Mode with MD1 and MD0 returning to 0, 0.

G2–G0 Gain Selection Bits. These bits select the gain setting for the on-chip PGA as outlined in Table X.

Table X. Gain Selection

G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

$\overline{B}$/U Bipolar/Unipolar Operation. A “0” in this bit selects Bipolar Operation. A “1” in this bit selects Unipolar Operation.

BUF Buffer Control. With this bit at “0,” the on-chip buffer on the analog input is shorted out. With the buffer shorted out, the current flowing in the V_{DD} line is reduced. When this bit is high, the on-chip buffer is in series with the analog input allowing the input to handle higher source impedances.

FSYNC Filter Synchronization. When this bit is high, the nodes of the digital filter, the filter control logic and the calibration control logic are held in a reset state and the analog modulator is also held in its reset state. When this bit goes low, the modulator and filter start to process data and a valid word is available in 3×1/(output update rate), i.e., the settling time of the filter. This FSYNC bit does not affect the digital interface and does not reset the $\overline{DRDY}$ output if it is low.

Clock Register (RS2, RS1, RS0 = 0, 1, 0); Power-On/Reset Status: 05 Hex

The Clock Register is an 8-bit register from which data can either be read or to which data can be written. Table XI outlines the bit designations for the Clock Register.

Table XI. Clock Register

ZERO (0)	**ZERO (0)**	**ZERO (0)**	**CLKDIS (0)**	**CLKDIV (0)**	**CLK (1)**	**FS1 (0)**	**FS0 (1)**

ZERO — Zero. A zero MUST be written to these bits to ensure correct operation of the AD7705/AD7706. Failure to do so may result in unspecified operation of the device.

CLKDIS — Master Clock Disable Bit. A Logic 1 in this bit disables the master clock from appearing at the MCLK OUT pin. When disabled, the MCLK OUT pin is forced low. This feature allows the user the flexibility of using the MCLK OUT as a clock source for other devices in the system or of turning off the MCLK OUT as a power saving feature. When using an external master clock on the MCLK IN pin, the AD7705/AD7706 continues to have internal clocks and will convert normally with the CLKDIS bit active. When using a crystal oscillator or ceramic resonator across the MCLK IN and MCLK OUT pins, the AD7705/AD7706 clock is stopped and no conversions take place when the CLKDIS bit is active.

CLKDIV — Clock Divider Bit. With this bit at a Logic 1, the clock frequency appearing at the MCLK IN pin is divided by two before being used internally by the AD7705/AD7706. For example, when this bit is set to 1, the user can operate with a 4.9152 MHz crystal between MCLK IN and MCLK OUT and internally the part will operate with the specified 2.4576 MHz. With this bit at a Logic 0, the clock frequency appearing at the MCLK IN pin is the frequency used internally by the part.

CLK — Clock Bit. This bit should be set in accordance with the operating frequency of the AD7705/AD7706. If the device has a master clock frequency of 2.4576 MHz (CLKDIV = 0) or 4.9152 MHz (CLKDIV = 1), then this bit should be set to a "1." If the device has a master clock frequency of 1 MHz (CLKDIV = 0) or 2 MHz (CLKDIV = 1), this bit should be set to a "0." This bit sets up the appropriate scaling currents for a given operating frequency and also chooses (along with FS1 and FS0) the output update rate for the device. If this bit is not set correctly for the master clock frequency of the device, then the AD7705/AD7706 may not operate to specification.

FS1, FS0 — Filter Selection Bits. Along with the CLK bit, FS1 and FS0 determine the output update rate, filter first notch and –3 dB frequency as outlined in Table XII. The on-chip digital filter provides a $sinc^3$ (or $Sinx/x^3$) filter response. In association with the gain selection, it also determines the output noise of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I to IV show the effect of filter notch frequency and gain on the output noise and effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, a new word is available at a 50 Hz output rate or every 20 ms. If the first notch is at 500 Hz, a new word is available every 2 ms. A calibration should be initiated when any of these bits are changed.

The settling time of the filter to a full-scale step input is worst case 4 × 1/(output data rate). For example, with the filter first notch at 50 Hz, the settling time of the filter to a full-scale step input is 80 ms max. If the first notch is at 500 Hz, the settling time is 8 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the FSYNC bit high, the settling-time will be 3 × 1/(output data rate) from when the FSYNC bit returns low.

The –3 dB frequency is determined by the programmed first notch frequency according to the relationship:

$$filter\ –3\ dB\ frequency = 0.262 \times filter\ first\ notch\ frequency$$

Table XII. Output Update Rates

CLK*	FS1	FS0	Output Update Rate	–3 dB Filter Cutoff
0	0	0	20 Hz	5.24 Hz
0	0	1	25 Hz	6.55 Hz
0	1	0	100 Hz	26.2 Hz
0	1	1	200 Hz	52.4 Hz
1	0	0	50 Hz	13.1 Hz
1	0	1	60 Hz	15.7 Hz
1	1	0	250 Hz	65.5 Hz
1	1	1	500 Hz	131 Hz

*Assumes correct clock frequency on MCLK IN pin with CLKDIV bit set appropriately.

Data Register (RS2, RS1, RS0 = 0, 1, 1)
The Data Register on the part is a 16-bit read-only register that contains the most up-to-date conversion result from the AD7705/AD7706. If the Communications Register sets up the part for a write operation to this register, a write operation must actually take place to return the part to where it is expecting a write operation to the Communications Register. However, the 16 bits of data written to the part will be ignored by the AD7705/AD7706.

Test Register (RS2, RS1, RS0 = 1, 0, 0); Power-On/Reset Status: 00 Hex
The part contains a Test Register that is used when testing the device. The user is advised not to change the status of any of the bits in this register from the default (Power-on or RESET) status of all 0s as the part will be placed in one of its test modes and will not operate correctly.

Zero-Scale Calibration Register (RS2, RS1, RS0 = 1, 1, 0); Power-On/Reset Status: 1F4000 Hex
The AD7705/AD7706 contains independent sets of zero-scale registers, one for each of the input channels. Each of these registers is a 24-bit read/write register; 24 bits of data must be written otherwise no data will be transferred to the register. This register is used in conjunction with its associated full-scale register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VII. While the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking the FSYNC bit in the mode register high before the calibration register operation and taking it low after the operation is complete.

Full-Scale Calibration Register (RS2, RS1, RS0 = 1, 1, 1); Power-On/Reset Status: 5761AB Hex
The AD7705/AD7706 contains independent sets of full-scale registers, one for each of the input channels. Each of these registers is a 24-bit read/write register; 24 bits of data must be written otherwise no data will be transferred to the register. This register is used in conjunction with its associated zero-scale register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table VII. While the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking FSYNC bit in the mode register high before the calibration register operation and taking it low after the operation is complete.

CALIBRATION SEQUENCES

The AD7705/AD7706 contains a number of calibration options as previously outlined. Table XIII summarizes the calibration types, the operations involved and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor when $\overline{\text{DRDY}}$ returns low at the end of the sequence. $\overline{\text{DRDY}}$ not only indicates when the sequence is complete, but also that the part has a valid new sample in its data register. This valid new sample is the result of a normal conversion which follows the calibration sequence. The second method of determining when calibration is complete is to monitor the MD1 and MD0 bits of the Setup Register. When these bits return to 0 (0 following a calibration command), it indicates that the calibration sequence is complete. This method does not give any indication of there being a valid new result in the data register. However, it gives an earlier indication than $\overline{\text{DRDY}}$ that calibration is complete. The duration to when the Mode Bits (MD1 and MD0) return to 0 (0 represents the duration of the calibration carried out). The sequence to when $\overline{\text{DRDY}}$ goes low also includes a normal conversion and a pipeline delay, t_P, to correctly scale the results of this first conversion. t_P will never exceed $2000 \times t_{CLKIN}$. The time for both methods is given in the table.

Table XIII. Calibration Sequences

Calibration Type	MD1, MD0	Calibration Sequence	Duration to Mode Bits	Duration to $\overline{\text{DRDY}}$
Self-Calibration	0, 1	Internal ZS Cal @ Selected Gain + Internal FS Cal @ Selected Gain	6 × 1/Output Rate	9 × 1/Output Rate + t_P
ZS System Calibration	1, 0	ZS Cal on AIN @ Selected Gain	3 × 1/Output Rate	4 × 1/Output Rate + t_P
FS System Calibration	1, 1	FS Cal on AIN @ Selected Gain	3 × 1/Output Rate	4 × 1/Output Rate + t_P

CIRCUIT DESCRIPTION

The AD7705/AD7706 is a sigma-delta A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a sigma-delta (or charge-balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bi-directional serial communications port. The part consumes only 320 μA of power supply current, making it ideal for battery-powered or loop-powered instruments. These parts operate with a supply voltage of 2.7 V to 3.3 V or 4.75 V to 5.25 V.

The AD7705 contains two programmable-gain fully differential analog input channels, while the AD7706 contains three pseudo differential analog input channels. The selectable gains on these inputs are 1, 2, 4, 8, 16, 32, 64 and 128 allowing the part to accept unipolar signals of between 0 mV to +20 mV and 0 V to +2.5 V, or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals +2.5 V. With a reference voltage of +1.225 V, the input ranges are from 0 mV to +10 mV to 0 V to +1.225 V in unipolar mode, and from ±10 mV to ±1.225 V in bipolar mode. Note that the bipolar ranges are with respect to AIN(–) on the AD7705, and with respect to COMMON on the AD7706, and not with respect to GND.

The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing A/D converter (Sigma-Delta Modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this sigma-delta modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the sigma-delta modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and hence its –3 dB frequency) can be programmed via the Setup Register bits FS0 and FS1. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency is from 50 Hz to 500 Hz, giving a programmable range for the –3 dB frequency of 13.1 Hz to 131 Hz. With a master clock frequency of 1 MHz, the programmable range for this first notch frequency is from 20 Hz to 200 Hz, giving a programmable range for the –3 dB frequency of 5.24 Hz to 52.4 Hz.

The basic connection diagram for the AD7705 is shown in Figure 10. This shows the AD7705 being driven from the analog +5 V supply. An AD780, precision +2.5 V reference, provides the reference source for the part. On the digital side, the part is configured for three-wire operation with $\overline{CS}$ tied to GND. A quartz crystal or ceramic resonator provide the master clock source for the part. In most cases, it will be necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary, depending on the manufacturer's specifications. The same setup applies to the AD7706.

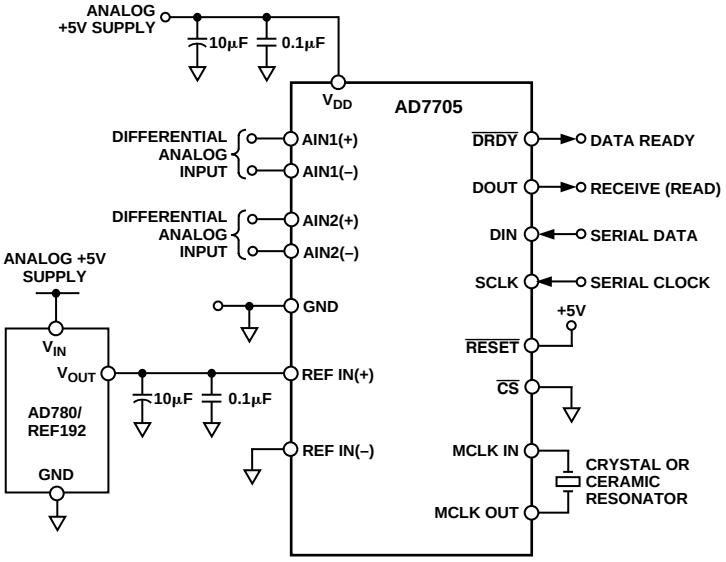


Figure 10. AD7705 Basic Connection Diagram

ANALOG INPUT

Analog Input Ranges

The AD7705 contains two differential analog input pairs AIN1(+), AIN1(–) and AIN2(+), AIN2(–). These input pairs provide programmable-gain, differential input channels that can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN(–) input of each input pair. The AD7706 contains three pseudo differential analog input pairs AIN1, AIN2 and AIN3, which are referenced to the COMMON input on the part.

In unbuffered mode, the common-mode range of the input is from GND to V_{DD}, provided that the absolute value of the analog input voltage lies between GND – 30 mV and V_{DD} + 30 mV. This means that in unbuffered mode the part can handle both unipolar and bipolar input ranges for all gains. Absolute voltages of GND – 200 mV can be accommodated on the analog inputs at 25°C without degradation in performance, but leakage current increases appreciably with increasing temperature. In buffered mode, the analog inputs can handle much larger source impedances, but the absolute input voltage range is restricted to between GND + 50 mV to V_{DD} – 1.5 V which also places restrictions on the common-mode range. This means that in buffered mode there are some restrictions on the allowable gains for bipolar input ranges. Care must be taken in setting up the common-mode voltage and input voltage range so that the above limits are not exceeded, otherwise there will be a degradation in linearity performance.

In unbuffered mode, the analog inputs look directly into the 7 pF input sampling capacitor, C_{SAMP}. The dc input leakage current in this unbuffered mode is 1 nA maximum. As a result, the analog inputs see a dynamic load that is switched at the input sample rate (see Figure 11). This sample rate depends on master clock frequency and selected gain. C_{SAMP} is charged to AIN(+) and discharged to AIN(–) every input sample cycle. The effective on-resistance of the switch, R_{SW}, is typically 7 kΩ.

C_{SAMP} must be charged through R_{SW} and through any external source impedances every input sample cycle. Therefore, in unbuffered mode, source impedances mean a longer charge time for C_{SAMP} and this may result in gain errors on the part. Table XIV shows the allowable external resistance/capacitance values, for unbuffered mode, such that no gain error to the 16-bit level is introduced on the part. Note that these capacitances are total capacitances on the analog input, external capacitance plus 10 pF capacitance from the pins and lead frame of the device.

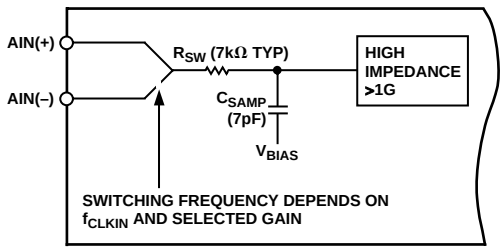


Figure 11. Unbuffered Analog Input Structure

Table XIV. External R, C Combination for No 16-Bit Gain Error (Unbuffered Mode Only)

	External Capacitance (pF)					
Gain	**0**	**50**	**100**	**500**	**1000**	**5000**
1	368 kΩ	90.6 kΩ	54.2 kΩ	14.6 kΩ	8.2 kΩ	2.2 kΩ
2	177.2 kΩ	44.2 kΩ	26.4 kΩ	7.2 kΩ	4 kΩ	1.12 kΩ
4	82.8 kΩ	21.2 kΩ	12.6 kΩ	3.4 kΩ	1.94 kΩ	540 Ω
8–128	35.2 kΩ	9.6 kΩ	5.8 kΩ	1.58 Ω	880 Ω	240 Ω

In buffered mode, the analog inputs look into the high-impedance inputs stage of the on-chip buffer amplifier. C_{SAMP} is charged via this buffer amplifier such that source impedances do not affect the charging of C_{SAMP}. This buffer amplifier has an offset leakage current of 1 nA. In this buffered mode, large source impedances result in a small dc offset voltage developed across the source impedance, but not in a gain error.

Input Sample Rate

The modulator sample frequency for the AD7705/AD7706 remains at $f_{CLKIN}/128$ (19.2 kHz @ f_{CLKIN} = 2.4576 MHz) regardless of the selected gain. However, gains greater than 1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table XV). In buffered mode, the input is buffered before the input sampling capacitor. In unbuffered mode, where the analog input looks directly into the sampling capacitor, the effective input impedance is $1/C_{SAMP} \times f_S$ where C_{SAMP} is the input sampling capacitance and f_S is the input sample rate.

Table XV. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLKIN}/64$ (38.4 kHz @ f_{CLKIN} = 2.4576 MHz)
2	$2 \times f_{CLKIN}/64$ (76.8 kHz @ f_{CLKIN} = 2.4576 MHz)
4	$4 \times f_{CLKIN}/64$ (76.8 kHz @ f_{CLKIN} = 2.4576 MHz)
8–128	$8 \times f_{CLKIN}/64$ (307.2 kHz @ f_{CLKIN} = 2.4576 MHz)

Bipolar/Unipolar Inputs

The analog inputs on the AD7705/AD7706 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages on its analog input, since the analog input cannot go more negative than –30 mV to ensure correct operation of these parts. The input channels are fully differential. As a result, on the AD7705, the voltage to which the unipolar and bipolar signals on the AIN(+) input are referenced is the voltage on the respective AIN(–) input. On the AD7706, the voltages applied to the analog input channels are referenced to the COMMON input. For example, if AIN1(–) is +2.5 V and the AD7705 is configured for unipolar operation with a gain of 2 and a V_{REF} of +2.5 V, the input voltage range on the AIN1(+) input is +2.5 V to +3.75 V. If AIN1(–) is +2.5 V and the AD7705 is configured for bipolar mode with a gain of 2 and a V_{REF} of +2.5 V, the analog input range on the AIN1(+) input is +1.25 V to +3.75 V (i.e., 2.5 V ± 1.25 V). If AIN1(–) is at GND, the part cannot be configured for bipolar ranges in excess of ±30 mV.

Bipolar or unipolar options are chosen by programming the $\overline{B}$/U bit of the Setup Register. This programs the channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change any of the input signal conditioning, it simply changes the data output coding and the points on the transfer function where calibrations occur.

REFERENCE INPUT

The AD7705/AD7706's reference inputs, REF IN(+) and REF IN(–), provide a differential reference input capability. The common-mode range for these differential inputs is from GND to V_{DD}. The nominal reference voltage, V_{REF} (REF IN(+) – REF IN(–)), for specified operation, is +2.5 V for the AD7705/AD7706 operated with a V_{DD} of 5 V and +1.225 V for the AD7705/AD7706 operated with a V_{DD} of 3 V. The part is functional with V_{REF} voltages down to 1 V, but with degraded performance as the output noise will, in terms of LSB size, be larger. REF IN(+) must always be greater than REF IN(–) for correct operation of the AD7705/AD7706.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs in unbuffered mode. The maximum dc input leakage current is ±1 nA over temperature, and source resistance may result in gain errors on the part. In this case, the sampling switch resistance is 5 kΩ typ and the reference capacitor (C_{REF}) varies with gain. The sample rate on the reference inputs is $f_{CLKIN}/64$ and does not vary with gain. For gains of 1 and 2, C_{REF} is 8 pF; for a gain of 16, it is 5.5 pF, for a gain of 32, it is 4.25 pF, for a gain of 64, it is 3.625 pF and for a gain of 128, it is 3.3125 pF.

The output noise performance outlined in Tables I through IV is for an analog input of 0 V, which effectively removes the effect of noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7705/AD7706. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7705/AD7706. In applications where the excitation voltage for the bridge transducer on the analog input also derives the reference voltage for the part, the effect of the noise in the excitation voltage will be removed as the application is ratiometric. Recommended reference voltage sources for the AD7705 with a V_{DD} of 5 V include the AD780, REF43 and REF192, while the recommended reference sources for the AD7705 operated with a V_{DD} of 3 V include the AD589 and AD1580. It is generally recommended to decouple the output of these references in order to further reduce the noise level.

DIGITAL FILTERING

The AD7705/AD7706 contains an on-chip low-pass digital filter which processes the output of the part's sigma-delta modulator. Therefore, the part not only provides the analog-to-digital conversion function but also provides a level of filtering. There are a number of system differences when the filtering function is provided in the digital domain rather than the analog domain and the user should be aware of these.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Also, the digital filter can be made programmable far more readily than an analog filter. Depending on the digital filter design, this gives the user the capability of programming cutoff frequency and output update rate.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7705/AD7706 has overrange headroom built into the sigma-delta modulator and digital filter, which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full-scale is half that of the analog input channel full-scale. This will provide an overrange capability greater than 100% at the expense of reducing the dynamic range by 1 bit (50%).

In addition, the digital filter does not provide any rejection at integer multiples of the digital filter's sample frequency. However, the input sampling on the part provides attenuation at multiples of the digital filter's sampling frequency so that the unattenuated bands actually occur around multiples of the sampling frequency f_S (as defined in Table XV). Thus the unattenuated bands occur at $n \times f_S$ (where n = 1, 2, 3 . . .). At these frequencies, there are frequency bands, $\pm f_{3\ dB}$ wide $f_{3\ dB}$ is the cutoff frequency of the digital filter) at either side where noise passes unattenuated to the output.

Filter Characteristics

The AD7705/AD7706's digital filter is a low-pass filter with a $(\sin x/x)^3$ response (also called sinc^3). The transfer function for this filter is described in the z-domain by:

$$H(z) = \left| \frac{1}{N} \times \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3$$

and in the frequency domain by:

$$H(f) = \left| \frac{1}{N} \times \frac{SIN(N \times \pi \times f/f_S)}{SIN(\pi \times f/f_S)} \right|^3$$

where N is the ratio of the modulator rate to the output rate.

Phase Response:

$$\angle H = -3\pi(N-2) \times f/f_S \ Rad$$

Figure 4 shows the filter frequency response for a cutoff frequency of 15.72 Hz, which corresponds to a first filter notch frequency of 60 Hz. The plot is shown from dc to 390 Hz. This response is repeated at either side of the digital filter's sample frequency and at either side of multiples of the filter's sample frequency.

The response of the filter is similar to that of an averaging filter, but with a sharper roll-off. The output rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Thus, for the plot of Figure 12 where the output rate is 60 Hz, the first notch of the filter is at 60 Hz. The notches of this $(\sin x/x)^3$ filter are repeated at multiples of the first notch. The filter provides attenuation of better than 100 dB at these notches.

The cutoff frequency of the digital filter is determined by the value loaded to bits FS0 to FS1 in the CLOCK Register. Programming a different cutoff frequency via FS0 and FS1 does not alter the profile of the filter response, it changes the frequency of the notches. The output update of the part and the frequency of the first notch correspond.

Since the AD7705/AD7706 contains this on-chip, low-pass filtering, a settling time is associated with step function inputs and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the output rate chosen for the filter. The settling time of the filter to a full-scale step input can be up to four times the output data period. For a synchronized step input (using the FSYNC function), the settling time is three times the output data period.

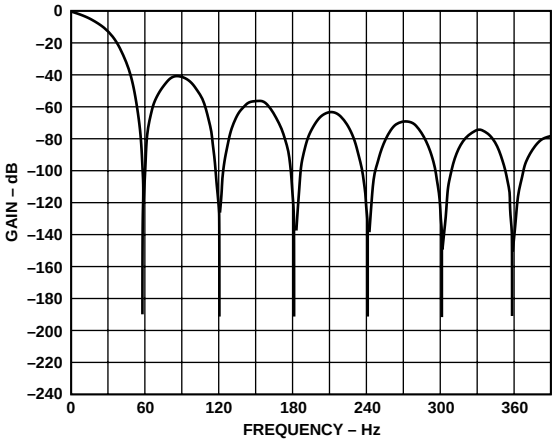


Figure 12. Frequency Response of AD7705 Filter

Post-Filtering

The on-chip modulator provides samples at a 19.2 kHz output rate with f_{CLKIN} at 2.4576 MHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Since the output data rate is higher than the Nyquist criterion, the output rate for a given bandwidth will satisfy most application requirements. There may, however, be some applications which require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate will require some post-filtering following the digital filter of the AD7705/AD7706.

For example, if the required bandwidth is 7.86 Hz, but the required update rate is 100 Hz, the data can be taken from the AD7705/AD7706 at the 100 Hz rate giving a –3 dB bandwidth of 26.2 Hz. Post-filtering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Post-filtering can also be used to reduce the output noise from the device for bandwidths below 13.1 Hz. At a gain of 128 and a bandwidth of 13.1 Hz, the output rms noise is 450 nV. This is essentially device noise or white noise and since the input is chopped, the noise has a primarily flat frequency response. By reducing the bandwidth below 13.1 Hz, the noise in the resultant passband can be reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately 1.25 in the output rms noise. This additional filtering will result in a longer settling-time.

ANALOG FILTERING

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency, as outlined earlier. However, due to the AD7705/AD7706's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. This means that the analog filtering requirements in front of the AD7705/AD7706 are considerably reduced versus a conventional converter with no on-chip filtering. In addition, because the part's common-mode rejection performance of 100 dB extends out to several kHz, common-mode noise in this frequency range will be substantially reduced.

Depending on the application, however, it may be necessary to provide attenuation prior to the AD7705/AD7706 in order to eliminate unwanted frequencies from these bands which the digital filter will pass. It may also be necessary in some applications to provide analog filtering in front of the AD7705/AD7706 to ensure that differential noise signals outside the band of interest do not saturate the analog modulator.

If passive components are placed in front of the AD7705/AD7706 in unbuffered mode, care must be taken to ensure that the source impedance is low enough not to introduce gain errors in the system. This significantly limits the amount of passive antialiasing filtering which can be provided in front of the AD7705/AD7706 when it is used in unbuffered mode. However, when the part is used in buffered mode, large source impedances will simply result in a small dc offset error (a 10 kΩ source resistance will cause an offset error of less than 10 μV). Therefore, if the system requires any significant source impedances to provide passive analog filtering in front of the AD7705/AD7706, it is recommended that the part be operated in buffered mode.

CALIBRATION

The AD7705/AD7706 provides a number of calibration options which can be programmed via the MD1 and MD0 bits of the Setup Register. The different calibration options are outlined in the Setup Register and Calibration Sequences sections. A calibration cycle may be initiated at any time by writing to these bits of the Setup Register. Calibration on the AD7705/AD7706 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch or bipolar/unipolar input range.

The AD7705/AD7706 offers self-calibration and system calibration facilities. For full calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. As a result, the accuracy of the calibration can only be as good as the noise level that it provides in normal mode. The result of the "zero-scale" calibration conversion is stored in the Zero-Scale Calibration Register while the result of the "full-scale" calibration conversion is stored in the Full-Scale Calibration Register. With these readings, the microcontroller can calculate the offset and the gain slope for the input-to-output transfer function of the converter. Internally, the part works with a resolution of 33 bits to determine its conversion result of 16 bits.

Self-Calibration

A self-calibration is initiated on the AD7705/AD7706 by writing the appropriate values (0, 1) to the MD1 and MD0 bits of the Setup Register. In the self-calibration mode with a unipolar input range, the zero scale point used in determining the calibration coefficients is with the inputs of the differential pair internally shorted on the part (i.e., AIN(+) = AIN(–) = Internal Bias Voltage in the case of the AD7705 and AIN = COMMON = Internal Bias voltage on the AD7706). The PGA is set for the selected gain (as per G1 and G0 bits in the Communications Register) for this zero-scale calibration conversion. The full-scale calibration conversion is performed at the selected gain on an internally-generated voltage of V_{REF}/Selected Gain.

The duration time for the calibration is 6 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the zero-scale calibration and 3 × 1/Output Rate for the full-scale calibration. At this time the MD1 and MD0 bits in the Setup Register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{DRDY}$ going low is 9 × 1/Output Rate. This is made up of 3 × 1/Output Rate for the zero-scale calibration, 3 × 1/Output Rate for the full-scale calibration, 3 × 1/Output Rate for a conversion on the analog input and some overhead to correctly set up the coefficients. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Setup Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit is written to the Setup Register in the calibration command.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points are exactly the same as above but, since the part is configured for bipolar operation, the shorted inputs point is actually midscale of the transfer function.

System Calibration

System calibration allows the AD7705/AD7706 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration, but uses voltage values presented by the system to the AIN inputs for the zero- and full-scale points. Full system calibration requires a two-step process, a ZS System Calibration followed by an FS System Calibration.

For a full system calibration, the zero-scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated and remain stable until the step is complete. Once the system zero-scale voltage has been set up, a ZS System Calibration is then initiated by writing the appropriate values (1, 0) to the MD1 and MD0 bits of the Setup Register. The zero-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/Output Rate. At this time, the MD1 and MD0 bits in the Setup Register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{DRDY}$ going low is 4 × 1/Output Rate as the part performs a normal conversion on the AIN voltage before $\overline{DRDY}$ goes low. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Setup Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit is written to the Setup Register in the calibration command.

After the zero-scale point is calibrated, the full-scale point is applied to AIN and the second step of the calibration process is initiated by again writing the appropriate values (1, 1) to MD1 and MD0. Again, the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. The full-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/Output Rate. At this time, the MD1 and MD0 bits in the Setup Register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{DRDY}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{DRDY}$ going low is 4 × 1/Output Rate as the part performs a normal conversion on the AIN voltage before $\overline{DRDY}$ goes low. If $\overline{DRDY}$ is low before (or goes low during) the calibration command write to the Setup Register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{DRDY}$ goes high to indicate that calibration is in progress. Therefore, $\overline{DRDY}$ should be ignored for up to one modulator cycle after the last bit is written to the Setup Register in the calibration command.

In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale (zero differential voltage) and positive full-scale.

The fact that the system calibration is a two-step calibration offers another feature. After the sequence of a full system calibration has been completed, additional offset or gain calibrations can be performed by themselves to adjust the system zero reference point or the system gain. Calibrating one of the parameters, either system offset or system gain, will not affect the other parameter.

System calibration can also be used to remove any errors from source impedances on the analog input when the part is used in unbuffered mode. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage, but the system calibration can be used to remove this error.

Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset and span which can be accommodated. The overriding requirement in determining the amount of offset and gain that can be accommodated by the part is the requirement that the positive full-scale calibration limit is < 1.05 × V_{REF}/GAIN. This allows the input range to go 5% above the nominal range. The built-in headroom in the AD7705/AD7706's analog modulator ensures that the part will still operate correctly with a positive full-scale voltage that is 5% beyond the nominal.

The range of input span in both the unipolar and bipolar modes has a minimum value of 0.8 × V_{REF}/GAIN and a maximum value of 2.1 × V_{REF}/GAIN. However, the span (which is the difference between the bottom of the AD7705/AD7706's input

range and the top of its input range) has to take into account the limitation on the positive full-scale voltage. The amount of offset which can be accommodated depends on whether the unipolar or bipolar mode is being used. Once again, the offset has to take into account the limitation on the positive full-scale voltage. In unipolar mode, there is considerable flexibility in handling negative (with respect to AIN(–) on the AD7705 and with respect to COMMON on the AD7706) offsets. In both unipolar and bipolar modes, the range of positive offsets that can be handled by the part depends on the selected span. Therefore, in determining the limits for system zero-scale and full-scale calibrations, the user has to ensure that the offset range plus the span range does exceed $1.05 \times V_{REF}/GAIN$. This is best illustrated by looking at a few examples.

If the part is used in unipolar mode with a required span of $0.8 \times V_{REF}/GAIN$, the offset range the system calibration can handle is from $-1.05 \times V_{REF}/GAIN$ to $+0.25 \times V_{REF}/GAIN$. If the part is used in unipolar mode with a required span of $V_{REF}/GAIN$, the offset range the system calibration can handle is from $-1.05 \times V_{REF}/GAIN$ to $+0.05 \times V_{REF}/GAIN$. Similarly, if the part is used in unipolar mode and required to remove an offset of $0.2 \times V_{REF}/GAIN$, the span range the system calibration can handle is $0.85 \times V_{REF}/GAIN$.

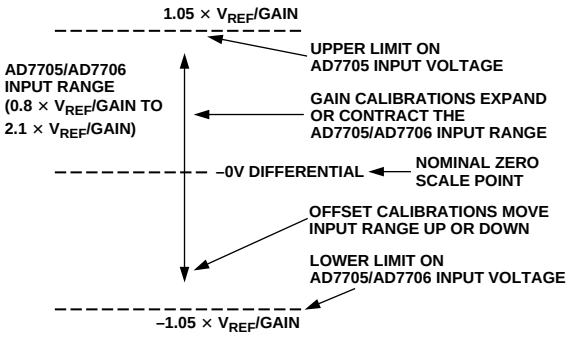


Figure 13. Span and Offset Limits

If the part is used in bipolar mode with a required span of $\pm 0.4 \times V_{REF}/GAIN$, the offset range the system calibration can handle is from $-0.65 \times V_{REF}/GAIN$ to $+0.65 \times V_{REF}/GAIN$. If the part is used in bipolar mode with a required span of $\pm V_{REF}/GAIN$, then the offset range which the system calibration can handle is from $-0.05 \times V_{REF}/GAIN$ to $+0.05 \times V_{REF}/GAIN$. Similarly, if the part is used in bipolar mode and required to remove an offset of $\pm 0.2 \times V_{REF}/GAIN$, the span range the system calibration can handle is $\pm 0.85 \times V_{REF}/GAIN$.

Power-Up and Calibration

On power-up, the AD7705/AD7706 performs an internal reset that sets the contents of the internal registers to a known state. There are default values loaded to all registers after power-on or reset. The default values contain nominal calibration coefficients for the calibration registers. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up.

The power dissipation and temperature drift of the AD7705/AD7706 are low and no warm-up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must have stabilized before calibration is initiated. Similarly, if the clock source for the part is generated from a crystal or resonator across the MCLK pins, the start-up time for the oscillator circuit should elapse before a calibration is initiated on the part (see below).

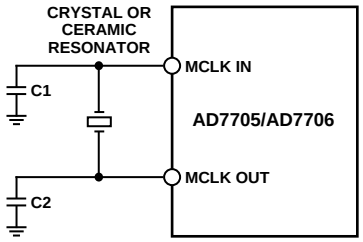


Figure 14. Crystal/Resonator Connection for the AD7705/AD7706

USING THE AD7705/AD7706

Clocking and Oscillator Circuit

The AD7705/AD7706 requires a master clock input, which may be an external CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal or ceramic resonator of the correct frequency can be connected between MCLK IN and MCLK OUT as shown in figure 6, in which case the clock circuit will function as an oscillator, providing the clock source for the part. The input sampling frequency, the modulator sampling frequency, the –3 dB frequency, output update rate and calibration time are all directly related to the master clock frequency, f_{CLKIN}. Reducing the master clock frequency by a factor of 2 will halve the above frequencies and update rate and double the calibration time. The current drawn from the V_{DD} power supply is also related to f_{CLKIN}. Reducing f_{CLKIN} by a factor of 2 will halve the digital part of the total V_{DD} current but will not affect the current drawn by the analog circuitry.

Using the part with a crystal or ceramic resonator between the MCLK IN and MCLK OUT pins generally causes more current to be drawn from V_{DD} than when the part is clocked from a driven clock signal at the MCLK IN pin. This is because the on-chip oscillator circuit is active in the case of the crystal or ceramic resonator. Therefore, the lowest possible current on the AD7705/AD7706 is achieved with an externally applied clock at the MCLK IN pin with MCLK OUT unconnected, unloaded and disabled.

The amount of additional current taken by the oscillator depends on a number of factors—first, the larger the value of capacitor (C1 and C2) placed on the MCLK IN and MCLK OUT pins, the larger the current consumption on the AD7705/AD7706. Care should be taken not to exceed the capacitor values recommended by the crystal and ceramic resonator manufacturers to avoid consuming unnecessary current. Typical values for C1 and C2 are recommended by crystal or ceramic resonator manufacturers, these are in the range of 30 pF to 50 pF and if the capacitor values on MCLK IN and MCLK OUT are kept in this range they will not result in any excessive current. Another factor that influences the current is the effective series resistance (ESR) of the crystal that appears between the MCLK IN and MCLK OUT pins of the AD7705/AD7706. As a general rule, the lower the ESR value the lower the current taken by the oscillator circuit.

When operating with a clock frequency of 2.4576 MHz, there is 50 μA difference in the current between an externally applied clock and a crystal resonator when operating with a V_{DD} of +3 V. With V_{DD} = +5 V and f_{CLKIN} = 2.4576 MHz, the typical current increases by 250 μA for a crystal/resonator supplied clock versus an externally applied clock. The ESR values for crystals and resonators at this frequency tend to be low and as a result there tends to be little difference between different crystal and resonator types.

When operating with a clock frequency of 1 MHz, the ESR value for different crystal types varies significantly. As a result, the current drain varies across crystal types. When using a crystal with an ESR of 700 Ω or when using a ceramic resonator, the increase in the typical current over an externally-applied clock is 20 μA with V_{DD} = +3 V and 200 μA with V_{DD} = +5 V. When using a crystal with an ESR of 3 kΩ, the increase in the typical current over an externally applied clock is again 100 μA with V_{DD} = +3 V but 400 μA with V_{DD} = +5 V.

The on-chip oscillator circuit also has a start-up time associated with it before it is oscillating at its correct frequency and correct voltage levels. Typical start-up times with V_{DD} = 5 V are 6 ms using a 4.9512 MHz crystal, 16 ms with a 2.4576 MHz crystal and 20 ms with a 1 MHz crystal oscillator. Start-up times are typically 20% slower when the power supply voltage is reduced to 3 V. At 3 V supplies, depending on the loading capacitances on the MCLK pins, a 1 MΩ feedback resistor may be required across the crystal or resonator in order to keep the start up times around the 20 ms duration.

The AD7705/AD7706's master clock appears on the MCLK OUT pin of the device. The maximum recommended load on this pin is one CMOS load. When using a crystal or ceramic resonator to generate the AD7705/AD7706's clock, it may be desirable to use this clock as the clock source for the system. In this case, it is recommended that the MCLK OUT signal is buffered with a CMOS buffer before being applied to the rest of the circuit.

System Synchronization

The FSYNC bit of the Setup Register allows the user to reset the modulator and digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, i.e., when the FSYNC is changed from 1 to 0.

With a 1 in the FSYNC bit of the Setup Register, the digital filter and analog modulator are held in a known reset state and the part is not processing any input samples. When a 0 is then written to the FSYNC bit, the modulator and filter are taken out of this reset state and the part starts to gather samples again on the next master clock edge.

The FSYNC input can also be used as a software start convert command allowing the AD7705/AD7706 to be operated in a conventional converter fashion. In this mode, writing to the FSYNC bit starts conversion and the falling edge of $\overline{DRDY}$ indicates when conversion is complete. The disadvantage of this scheme is that the settling time of the filter has to be taken into account for every data register update. This means that the rate at which the data register is updated is three times slower in this mode.

Since the FSYNC bit resets the digital filter, the full settling time of 3 × 1/Output Rate has to elapse before there is a new word loaded to the output register on the part. If the $\overline{DRDY}$ signal is low when FSYNC goes to a 0, the $\overline{DRDY}$ signal will not be reset high by the FSYNC command. This is because the AD7705/AD7706 recognizes that there is a word in the data register which has not been read. The $\overline{DRDY}$ line will stay low until an update of the data register takes place, at which time it will go high for 500 × t_{CLKIN} before returning low again. A read from the data register resets the $\overline{DRDY}$ signal high and it will not return low until the settling time of the filter has elapsed (from the FSYNC command) and there is a valid new word in the data register. If the $\overline{DRDY}$ line is high when the FSYNC command is issued, the $\overline{DRDY}$ line will not return low until the settling time of the filter has elapsed.

Reset Input

The $\overline{RESET}$ input on the AD7705/AD7706 resets all the logic, the digital filter and the analog modulator, while all on-chip registers are reset to their default state. $\overline{DRDY}$ is driven high and the AD7705/AD7706 ignores all communications to any of its registers while the $\overline{RESET}$ input is low. When the $\overline{RESET}$ input returns high, the AD7705/AD7706 starts to process data and $\overline{DRDY}$ will return low in 3 × 1/Output Rate indicating a valid new word in the data register. However, the AD7705/AD7706 operates with its default setup conditions after a $\overline{RESET}$ and it is generally necessary to set up all registers and carry out a calibration after a $\overline{RESET}$ command.

The AD7705/AD7706's on-chip oscillator circuit continues to function even when the $\overline{RESET}$ input is low. The master clock signal continues to be available on the MCLK OUT pin. Therefore, in applications where the system clock is provided by the AD7705/AD7706's clock, the AD7705/AD7706 produces an uninterrupted master clock during $\overline{RESET}$ commands.

Standby Mode

The STBY bit in the Communications Register of the AD7705/AD7706 allows the user to place the part in a power-down mode when it is not required to provide conversion results. The AD7705/AD7706 retains the contents of all its on-chip registers (including the data register) while in standby mode. When released from standby mode, the part starts to process data and a new word is available in the data register in 3 × 1/Output rate from when a 0 is written to the STBY bit.

The STBY bit does not affect the digital interface, nor does it affect the status of the $\overline{DRDY}$ line. If $\overline{DRDY}$ is high when the STBY bit is brought low, it will remain high until there is a valid new word in the data register. If $\overline{DRDY}$ is low when the STBY bit is brought low, it will remain low until the data register is updated, at which time the $\overline{DRDY}$ line will return high for 500 × t_{CLKIN} before returning low again. If $\overline{DRDY}$ is low when the part enters its standby mode (indicating a valid unread word in the data register), the data register can be read while the part is in standby. At the end of this read operation, the $\overline{DRDY}$ will be reset high as normal.

Placing the part in standby mode reduces the total current to 9 μA typical with V_{DD} = 5 V and 4 μA with V_{DD} = 3 V when the part is operated from an external master clock provided this master clock is stopped. If the external clock continues to run in standby mode, the standby current increases to 150 μA typical with 5 V supplies and 75 μA typical with 3.3 V supplies. If a crystal or ceramic resonator is used as the clock source, the total current in standby mode is 400 μA typical with 5 V supplies and 90 μA with 3.3 V supplies. This is because the on-chip oscillator circuit continues to run when the part is in its standby mode. This is important in applications where the system clock is provided by the AD7705/AD7706's clock, so that the AD7705/AD7706 produces an uninterrupted master clock even when it is in its standby mode.

Accuracy

Sigma-Delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7705/AD7706 achieves excellent linearity by the use of high quality, on-chip capacitors, which have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7705/AD7706 uses digital calibration techniques that minimize offset and gain error.

Drift Considerations

The AD7705/AD7706 uses chopper stabilization techniques to minimize input offset drift. Charge injection in the analog switches and dc leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES

The AD7705/AD7706 operates with a V_{DD} power supply between 2.7 V and 5.25 V. While the latch-up performance of the AD7705/AD7706 is good, it is important that power is applied to the AD7705/AD7706 before signals at REF IN, AIN or the logic input pins in order to avoid excessive currents. If this is not possible, the current that flows in any of these pins should be limited. If separate supplies are used for the AD7705/AD7706 and the system digital circuitry, the AD7705/AD7706 should be powered up first. If it is not possible to guarantee this, current limiting resistors should be placed in series with the logic inputs to again limit the current. Latch-up current is greater than 100 mA.

Supply Current

The current consumption on the AD7705/AD7706 is specified for supplies in the range +2.7 V to +3.3 V and in the range +4.75 V to +5.25 V. The part operates over a +2.7 V to +5.25 V supply range and the I_{DD} for the part varies as the supply voltage varies over this range. There is an internal current boost bit on the AD7705/AD7706 that is set internally in accordance with the operating conditions. This affects the current drawn by the analog circuitry within these devices. Minimum power consumption is achieved when the AD7705/AD7706 is operated with an f_{CLKIN} of 1 MHz or at gains of 1 to 4 with f_{CLKIN} = 2.4575 MHz as the internal boost bit is off reducing the analog current consumption. Figure 15 shows the variation of the typical I_{DD} with V_{DD} voltage for both a 1 MHz crystal oscillator and a 2.4576 MHz crystal oscillator at +25°C. The AD7705/AD7706 is operated in unbuffered mode. The relationship shows that the I_{DD} is minimized by operating the part with lower V_{DD} voltages. I_{DD} on the AD7705/AD7706 is also minimized by using an external master clock or by optimizing external components when using the on-chip oscillator circuit. Figures 3, 4, 6 and 7 show variations in I_{DD} with gain, V_{DD} and clock frequency using an external clock.

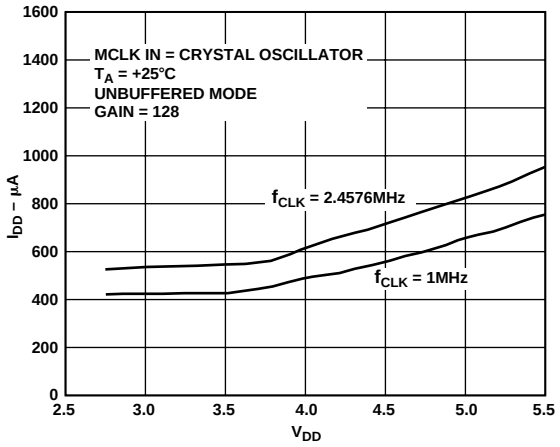


Figure 15. I_{DD} vs. Supply Voltage

Grounding and Layout

Since the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided those noise sources do not saturate the analog modulator. As a result, the AD7705/AD7706 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7705/AD7706 is so high, and the noise levels from the AD7705/AD7706 so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7705 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place to avoid ground loops. If the AD7705/AD7706 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point which should be established as close as possible to the AD7705 GND.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7705/AD7706 to avoid noise coupling. The power supply lines to the AD7705/AD7706 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF ceramic capacitors to GND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 μF disc ceramic capacitors to DGND.

Evaluating the AD7705/AD7706 Performance

The recommended layout for the AD7705 and AD7706 is outlined in their associated evaluation. These evaluation board packages include a fully assembled and tested evaluation board, documentation, software for controlling the board over the printer port of a PC and software for analyzing their performance on the PC.

Noise levels in the signals applied to the AD7705/AD7706 may also affect performance of the part. The AD7705/AD7706 software evaluation package allows the user to evaluate the true performance of the part, independent of the analog input signal. The scheme involves using a test mode on the part where the inputs to the AD7705 are internally shorted together to provide a zero differential voltage for the analog modulator. External to the device, the AIN1(–) input on the AD7705 should be connected to a voltage that is within the allowable common-mode range of the part. Similarly, on the AD7706 the COMMON input should be connected to a voltage within its allowable common-mode range for evaluation purposes. This scheme should be used after a calibration has been performed on the part.

DIGITAL INTERFACE

As previously outlined, the AD7705/AD7706's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications to the part must start with a write operation to the Communications Register. After power-on or RESET, the device expects a write to its Communications Register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications Register followed by a write to the selected register. A read operation from any other register on the part (including the output data register) starts with a write operation to the Communications Register followed by a read operation from the selected register.

The AD7705/AD7706's serial interface consists of five signals, $\overline{CS}$, SCLK, DIN, DOUT and $\overline{DRDY}$. The DIN line is used for transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the AD7705/AD7706's data register. $\overline{DRDY}$ goes low when a new data word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when *not* to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select the device. It can be used to decode the AD7705/AD7706 in systems where a number of parts are connected to the serial bus.

Figures 16 and 17 show timing diagrams for interfacing to the AD7705/AD7706 with $\overline{CS}$ used to decode the part. Figure 16 is for a read operation from the AD7705/AD7706's output shift register while Figure 17 shows a write operation to the input shift register. It is possible to read the same data twice from the output register even though the $\overline{DRDY}$ line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The AD7705/AD7706 serial interface can operate in three-wire mode by tying the $\overline{CS}$ input low. In this case, the SCLK, DIN and DOUT lines are used to communicate with the AD7705/AD7706 and the status of $\overline{DRDY}$ can be obtained by interrogating the MSB of the Communications Register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that the SCLK idles high between data transfers.

The AD7705/AD7706 can also be operated with $\overline{CS}$ used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$ since $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided the timing numbers are obeyed.

The serial interface can be reset by exercising the $\overline{RESET}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7705/AD7706 DIN line for at least 32 serial clock cycles the serial interface is reset. This ensures that in three-wire systems, if the interface gets lost either via a software error or by some glitch in the system, it can be reset back to a known state. This state returns the interface to where the AD7705/AD7706 is expecting a write operation to its Communications Register. This operation in itself does not reset the contents of any registers but since the interface was lost, the information written to any of the registers is unknown and it is advisable to set up all registers again.

Some microprocessor or microcontroller serial interfaces have a single serial data line. In this case, it is possible to connect the AD7705/AD7706's DATA OUT and DATA IN lines together and connect them to the single data line of the processor. A 10 kΩ pull-up resistor should be used on this single data line. In this case, if the interface gets lost, because the read and write operations share the same line the procedure to reset it back to a known state is somewhat different than previously described. It requires a read operation of 24 serial clocks followed by a write operation where a Logic 1 is written for at least 32 serial clock cycles to ensure that the serial interface is back into a known state.

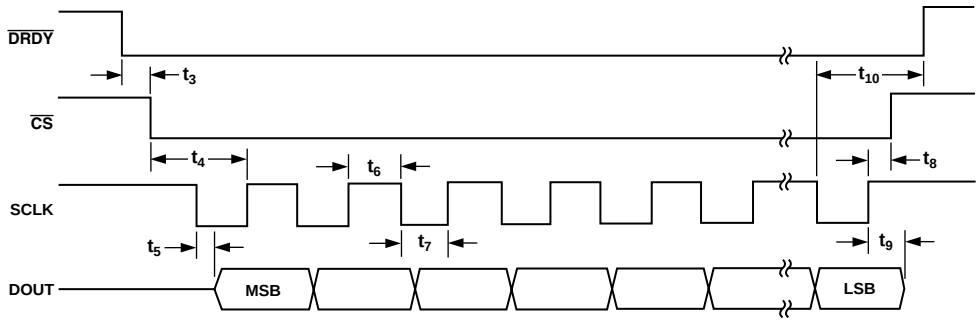


Figure 16. Read Cycle Timing Diagram

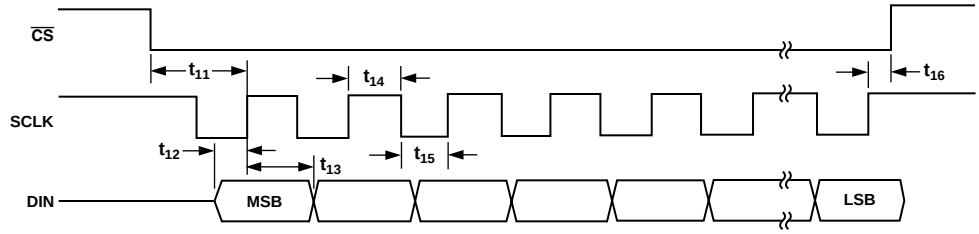


Figure 17. Write Cycle Timing Diagram

CONFIGURING THE AD7705/AD7706

The AD7705/AD7706 contains six on-chip registers that the user can accesses via the serial interface. Communication with any of these registers is initiated by writing to the Communications Register first. Figure 18 outlines a flow diagram of the sequence used to configure all registers after a power-up or reset on the AD7705, similar procedures apply to the AD7706. The flowchart also shows two different read options—the first where the $\overline{\text{DRDY}}$ pin is polled to determine when an update of the data register has taken place, the second where the $\overline{\text{DRDY}}$ bit of the Communications Register is interrogated to see if a data register update has taken place. Also included in the flowing diagram is a series of words that should be written to the registers for a particular set of operating conditions. These conditions are gain of one, no filter sync, bipolar mode, buffer off, clock of 4.9512 MHz and an output rate of 50 Hz.

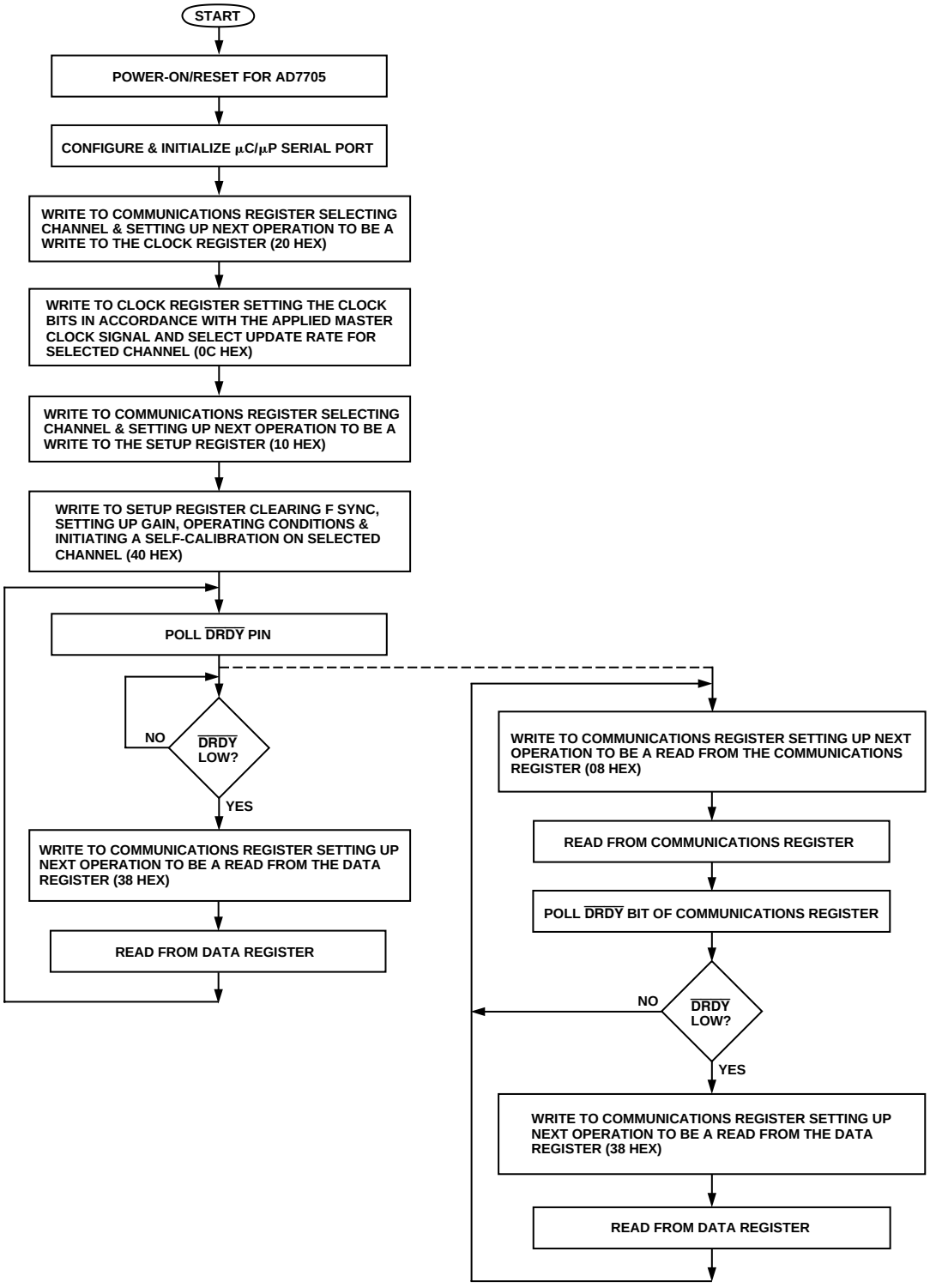


Figure 18. Flowchart for Setting Up and Reading from the AD7705

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7705/AD7706's flexible serial interface allows for easy interface to most microcomputers and microprocessors. The flowchart of Figure 10 outlines the sequence that should be followed when interfacing a microcontroller or microprocessor to the AD7705/AD7706. Figures 19, 20 and 21 show some typical interface circuits.

The serial interface on the AD7705/AD7706 is capable of operating from just three wires and is compatible with SPI interface protocols. The three-wire operation makes the part ideal for isolated systems where minimizing the number of interface lines minimizes the number of opto-isolators required in the system. The serial clock input is a Schmitt triggered input to accommodate slow edges from opto-couplers. The rise and fall times of other digital inputs to the AD7705/AD7706 should be no longer than 1 µs.

Most of the registers on the AD7705/AD7706 are 8-bit registers, which facilitates easy interfacing to the 8-bit serial ports of microcontrollers. The Data Register on the AD7705/AD7706 is 16 bits, and the offset and gain registers are 24-bit registers but data transfers to these registers can consist of multiple 8-bit transfers to the serial port of the microcontroller. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7705/AD7706.

Even though some of the registers on the AD7705/AD7706 are only eight bits in length, communicating with two of these registers in successive write operations can be handled as a single 16-bit data transfer if required. For example, if the Setup Register is to be updated, the processor must first write to the Communications Register (saying that the next operation is a write to the Setup Register) and then write eight bits to the Setup Register. If required, this can all be done in a single 16-bit transfer because once the eight serial clocks of the write operation to the Communications Register have been completed, the part immediately sets itself up for a write operation to the Setup Register.

AD7705/AD7706 to 68HC11 Interface

Figure 19 shows an interface between the AD7705/AD7706 and the 68HC11 microcontroller. The diagram shows the minimum (three-wire) interface with $\overline{CS}$ on the AD7705/AD7706 hard-wired low. In this scheme, the $\overline{DRDY}$ bit of the Communications Register is monitored to determine when the Data Register is updated. An alternative scheme, which increases the number of interface lines to four, is to monitor the $\overline{DRDY}$ output line from the AD7705/AD7706. The monitoring of the $\overline{DRDY}$ line can be done in two ways. First, $\overline{DRDY}$ can be connected to one of the 68HC11's port bits (such as PC0), which is configured as an input. This port bit is then polled to determine the status of $\overline{DRDY}$. The second scheme is to use an interrupt driven system, in which case the $\overline{DRDY}$ output is connected to the $\overline{IRQ}$ input of the 68HC11. For interfaces that require control of the $\overline{CS}$ input on the AD7705/AD7706, one of the port bits of the 68HC11 (such as PC1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

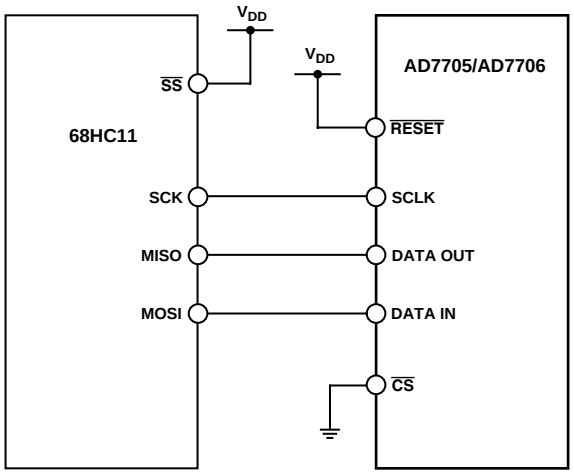


Figure 19. AD7705/AD7706 to 68HC11 Interface

The 68HC11 is configured in the master mode with its CPOL bit set to a logic one and its CPHA bit set to a logic one. When the 68HC11 is configured like this, its SCLK line idles high between data transfers. The AD7705/AD7706 is not capable of full duplex operation. If the AD7705/AD7706 is configured for a write operation, no data appears on the DATA OUT lines even when the SCLK input is active. Similarly, if the AD7705/AD7706 is configured for a read operation, data presented to the part on the DATA IN line is ignored even when SCLK is active.

Coding for an interface between the 68HC11 and the AD7705/AD7706 is given in Table XV. In this example, the $\overline{DRDY}$ output line of the AD7705/AD7706 is connected to the PC0 port bit of the 68HC11 and is polled to determine its status.

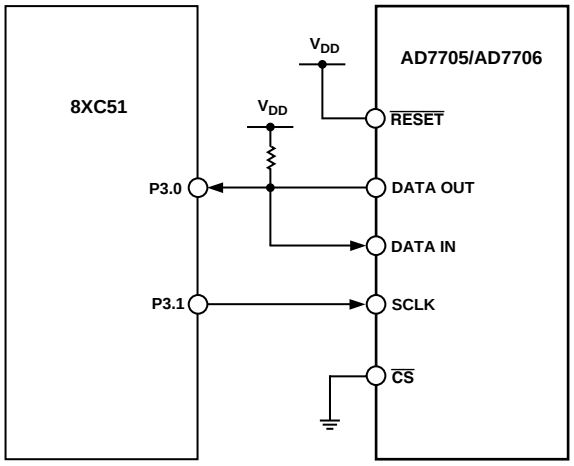


Figure 20. AD7705/AD7706 to 8XC51 Interface

AD7705/AD7706 to 8051 Interface

An interface circuit between the AD7705/AD7706 and the 8XC51 microcontroller is shown in Figure 20. The diagram shows the minimum number of interface connections with $\overline{CS}$ on the AD7705/AD7706 hard-wired low. In the case of the 8XC51 interface the minimum number of interconnects is just two. In this scheme, the $\overline{DRDY}$ bit of the Communications Register is monitored to determine when the Data Register is updated. The alternative scheme, which increases the number of

interface lines to three, is to monitor the $\overline{DRDY}$ output line from the AD7705/AD7706. The monitoring of the $\overline{DRDY}$ line can be done in two ways. First, $\overline{DRDY}$ can be connected to one of the 8XC51's port bits (such as P1.0) which is configured as an input. This port bit is then polled to determine the status of $\overline{DRDY}$. The second scheme is to use an interrupt-driven system, in which case the $\overline{DRDY}$ output is connected to the $\overline{INT1}$ input of the 8XC51. For interfaces that require control of the $\overline{CS}$ input on the AD7705/AD7706, one of the port bits of the 8XC51 (such as P1.1), which is configured as an output, can be used to drive the $\overline{CS}$ input. The 8XC51 is configured in its Mode 0 serial interface mode. Its serial interface contains a single data line. As a result, the DATA OUT and DATA IN pins of the AD7705/AD7706 should be connected together with a 10 kΩ pull-up resistor. The serial clock on the 8XC51 idles high between data transfers. The 8XC51 outputs the LSB first in a write operation, while the AD7705/AD7706 expects the MSB first so the data to be transmitted has to be rearranged before being written to the output serial register. Similarly, the AD7705/AD7706 outputs the MSB first during a read operation while the 8XC51 expects the LSB first. Therefore, the data read into the serial buffer needs to be rearranged before the correct data word from the AD7705/AD7706 is available in the accumulator.

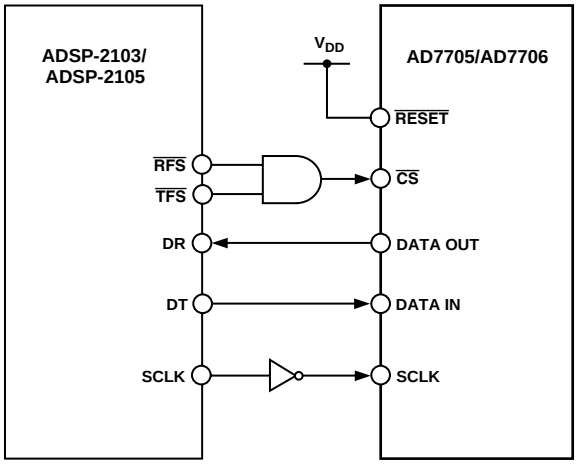


Figure 21. AD7705/AD7706 to ADSP-2103/ADSP-2105 Interface

AD7705/AD7706 to ADSP-2103/ADSP-2105 Interface

Figure 21 shows an interface between the AD7705/AD7706 and the ADSP-2103/ADSP-2105 DSP processor. In the interface shown, the $\overline{DRDY}$ bit of the Communications Register is again monitored to determine when the Data Register is updated. The alternative scheme is to use an interrupt-driven system, in which case the $\overline{DRDY}$ output is connected to the IRQ2 input of the ADSP-2103/ADSP-2105. The serial interface of the ADSP-2103/ADSP-2105 is set up for alternate framing mode. The $\overline{RFS}$ and $\overline{TFS}$ pins of the ADSP-2103/ADSP-2105 are configured as active low outputs and the ADSP-2103/ADSP-2105 serial clock line, SCLK, is also configured as an output. The $\overline{CS}$ for the AD7705/AD7706 is active when either the $\overline{RFS}$ or $\overline{TFS}$ outputs from the ADSP-2103/ADSP-2105 are active. The serial clock rate on the ADSP-2103/ADSP-2105 should be limited to 3 MHz to ensure correct operation with the AD7705/AD7706.

CODE FOR SETTING UP THE AD7705/AD7706

Table XVII gives a set of read and write routines in C code for interfacing the 68HC11 microcontroller to the AD7705. The sample program sets up the various registers on the AD7705 and reads 1000 samples from the part into the 68HC11. The setup conditions on the part are exactly the same as those outlined for the flowchart of Figure 18. In the example code given here, the $\overline{DRDY}$ output is polled to determine if a new valid word is available in the data register. The very same sequence is applicable for the AD7706.

The sequence of the events in this program are as follows:

1. Write to the Communications Register, selecting channel one as the active channel and setting the next operation to be a write to the clock register.
2. Write to Clock Register setting the CLK DIV bit which divides the external clock internally by two. This assumes that the external crystal is 4.9512 MHz. The update rate is selected to be 50 Hz.
3. Write to Communication Register selecting Channel 1 as the active channel and setting the next operation to be a write to the Setup Register.
4. Write to the Setup Register, setting the gain to 1, setting bipolar mode, buffer off, clearing the filter synchronization and initiating a self-calibration.
5. Poll the $\overline{DRDY}$ output.
6. Read the data from the Data Register.
7. Loop around doing Steps 5 and 6 until the specified number of samples have been taken from the selected channel.

Table XVII. C Code for Interfacing AD7705 to 68HC11

```
/* This program has read and write routines for the 68HC11 to interface to the AD7705 and the sample program sets the various
registers and then reads 1000 samples from one channel. */
#include <math.h>
#include <io6811.h>
#define NUM_SAMPLES 1000 /* change the number of data samples */
#define MAX_REG_LENGTH 2 /* this says that the max length of a register is 2 bytes */
Writetoreg (int);
Read (int,char);
char *datapointer = store;
char store[NUM_SAMPLES*MAX_REG_LENGTH + 30];
void main()
{
        /* the only pin that is programmed here from the 68HC11 is the /CS and this is why the PC2 bit of PORTC is made as
an output */
char a;
DDRC = 0x04; /* PC2 is an output the rest of the port bits are inputs */
PORTC | = 0x04;  /* make the /CS line high */
Writetoreg(0x20); /* Active Channel is Ain1(+)/Ain1(-), next operation as write to the clock register */
Writetoreg(0x0C); /* master clock enabled, 4.9512MHz Clock, set output rate to 50Hz*/
Writetoreg(0x10); /* Active Channel is Ain1(+)/Ain1(-), next operation as write to the setup register */
Writetoreg(0x40); /* gain = 1, bipolar mode, buffer off, clear FSYNC and perform a Self Calibration*/
while(PORTC & 0x10); /* wait for /DRDY to go low */
for(a=0;a<NUM_SAMPLES;a++);
        {
        Writetoreg(0x38); /*set the next operation for 16 bit read from the data register */
        Read(NUM_SAMPES,2);
        }
}
Writetoreg(int byteword);
{
int q;
SPCR = 0x3f;
SPCR = 0X7f; /* this sets the WiredOR mode(DWOM=1), Master mode(MSTR=1), SCK idles high(CPOL=1), /SS can be low
always (CPHA=1), lowest clock speed(slowest speed which is master clock /32 */
DDRD = 0x18; /* SCK, MOSI outputs */
q = SPSR;
q = SPDR;  /* the read of the staus register and of the data register is needed to clear the interrupt which tells the user that the
data transfer is complete */
PORTC &= 0xfb; /* /CS is low */
SPDR = byteword;  /* put the byte into data register */
while(!(SPSR & 0x80));  /* wait for /DRDY to go low */
PORTC |= 0x4;  /* /CS high */
}
Read(int amount, int reglength)
{
int q;
SPCR = 0x3f;
SPCR = 0x7f;  /* clear the interupt */
DDRD = 0x10;  /* MOSI output, MISO input, SCK output */
while(PORTC & 0x10);  /* wait for /DRDY to go low */
PORTC & 0xfb ; /* /CS is low */
for(b=0;b<reglength;b++)
        {
        SPDR = 0;
        while(!(SPSR & 0x80));  /* wait until port ready before reading */
        *datapointer++=SPDR;  /* read SPDR into store array via datapointer */
        }
PORTC|=4; /* /CS is high */
}
```

APPLICATIONS

The AD7705 provides a dual channel, low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a sigma-delta architecture, it makes the part more immune to noisy environments thus making the part ideal for use in industrial and process control applications. It also provides a programmable gain amplifier, a digital filter and calibration options. Thus, it provides far more system level functionality than off-the-shelf integrating ADCs without the disadvantage of having to supply a high quality integrating capacitor. In addition, using the AD7705 in a system allows the system designer to achieve a much higher level of resolution because noise performance of the AD7705 is better than that of the integrating ADCs.

The on-chip PGA allows the AD7705 to handle an analog input voltage range as low as 10 mV full-scale with V_{REF} = +1.25 V. The differential inputs of the part allow this analog input range to have an absolute value anywhere between GND and V_{DD} when the part is operated in unbuffered mode. It allows the user to connect the transducer directly to the input of the AD7705. The programmable gain front end on the AD7705 allows the part to handle unipolar analog input ranges from 0 mV to +20 mV to 0 V to +2.5 V and bipolar inputs of ±20 mV to ±2.5 V. Because the part operates from a single supply these bipolar ranges are with respect to a biased-up differential input.

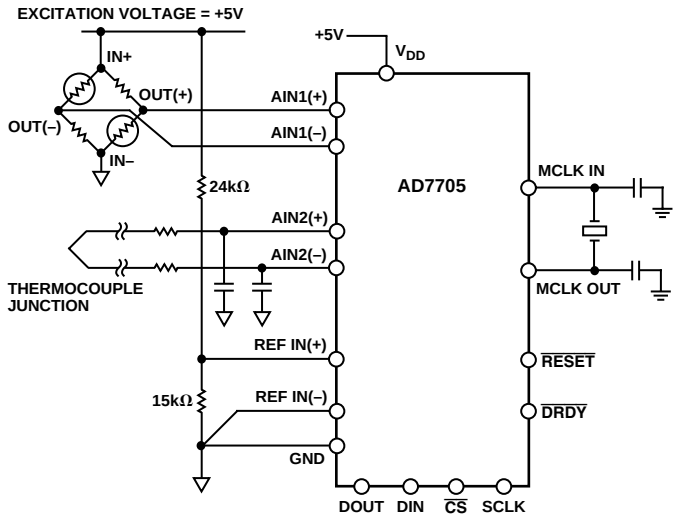


Figure 22. Pressure Measurement Using the AD7705

Pressure Measurement

One typical application of the AD7705 is pressure measurement. Figure 22 shows the AD7705 used with a pressure transducer, the BP01 from Sensym. The pressure transducer is arranged in a bridge network and gives a differential output voltage between its OUT(+) and OUT(–) terminals. With rated full-scale pressure (in this case 300 mmHg) on the transducer, the differential output voltage is 3 mV/V of the input voltage (i.e., the voltage between its IN(+) and IN(–) terminals). Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 15 mV. The excitation voltage for the bridge is also used to generate the reference voltage for the AD7705. Therefore, variations in the excitation voltage do not introduce errors in the system. Choosing resistor values of 24 kΩ and 15 kΩ, as per Figure 22, gives a 1.92 V reference voltage for the AD7705 when the excitation voltage is 5 V.

Using the part with a programmed gain of 128 results in the full-scale input span of the AD7705 being 15 mV, which corresponds with the output span from the transducer. The second channel on the AD7705 can be used as an auxiliary channel to measure a secondary variable such as temperature as shown in Figure 22. This secondary channel can be used as a means of adjusting the output of the primary channel, thus removing temperature effects in the system.

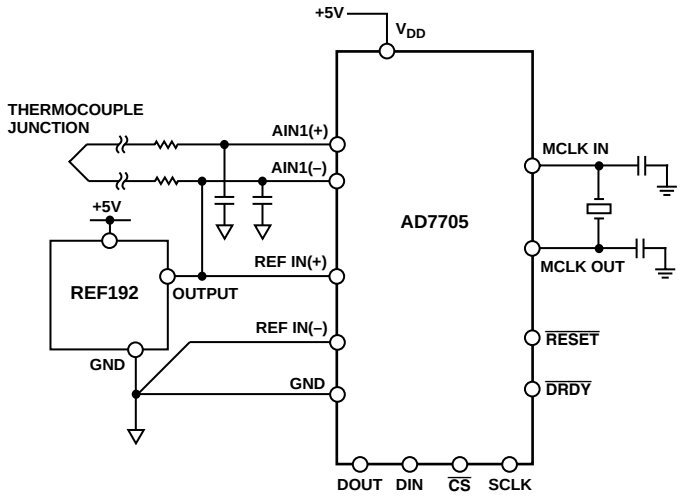


Figure 23. Temperature Measurement Using the AD7705

Temperature Measurement

Another application area for the AD7705 is in temperature measurement. Figure 23 outlines a connection from a thermocouple to the AD7705. In this application, the AD7705 is operated in its buffered mode to allow large decoupling capacitors on the front end to eliminate any noise pickup that may have been in the thermocouple leads. When the AD7705 is operated in buffered mode, it has a reduced common-mode range. In order to place the differential voltage from the thermocouple on a suitable common-mode voltage, the AIN1(–) input of the AD7705 is biased up at the reference voltage, +2.5 V.

Figure 23 shows another temperature measurement application for the AD7705. In this case, the transducer is an RTD (Resistive Temperature Device), a PT100. The arrangement is a 4-lead RTD configuration. There are voltage drops across the lead resistances R_{L1} and R_{L4} but these simply shift the common-mode voltage. There is no voltage drop across lead resistances R_{L2} and R_{L3} as the input current to the AD7705 is very low. The lead resistances present a small source impedance so it would not generally be necessary to turn on the buffer on the AD7705. If the buffer is required, the common-mode voltage should be set accordingly by inserting a small resistance between the bottom end of the RTD and GND of the AD7705. In the application shown, an external 400 μA current source provides the excitation current for the PT100 and also generates the reference voltage for the AD7705 via the 6.25 kΩ resistor. Variations in the excitation current do not affect the circuit as both the input voltage and the reference voltage vary radiometrically with the excitation current. However, the 6.25 kΩ resistor must have a low temperature coefficient to avoid errors in the reference voltage over temperature.

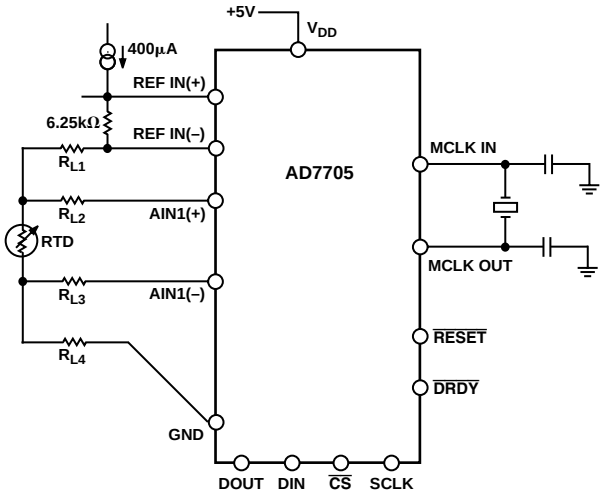


Figure 24. RTD Measurement Using the AD7705

Smart Transmitters

Another area where the low power, single supply, three-wire interface capabilities is of benefit is in smart transmitters. Here, the entire smart transmitter must operate from the 4 mA to 20 mA loop. Tolerances in the loop mean that the amount of current available to power the transmitter is as low as 3.5 mA. The AD7705 consumes only 320 μA, leaving at least 3 mA available for the rest of the transmitter. Figure 25 shows a block diagram of a smart transmitter which includes the AD7705. The AD7705 with its dual input channel is ideally suited to systems requiring an auxiliary channel whose measured variable is used to correct that of the primary channel.

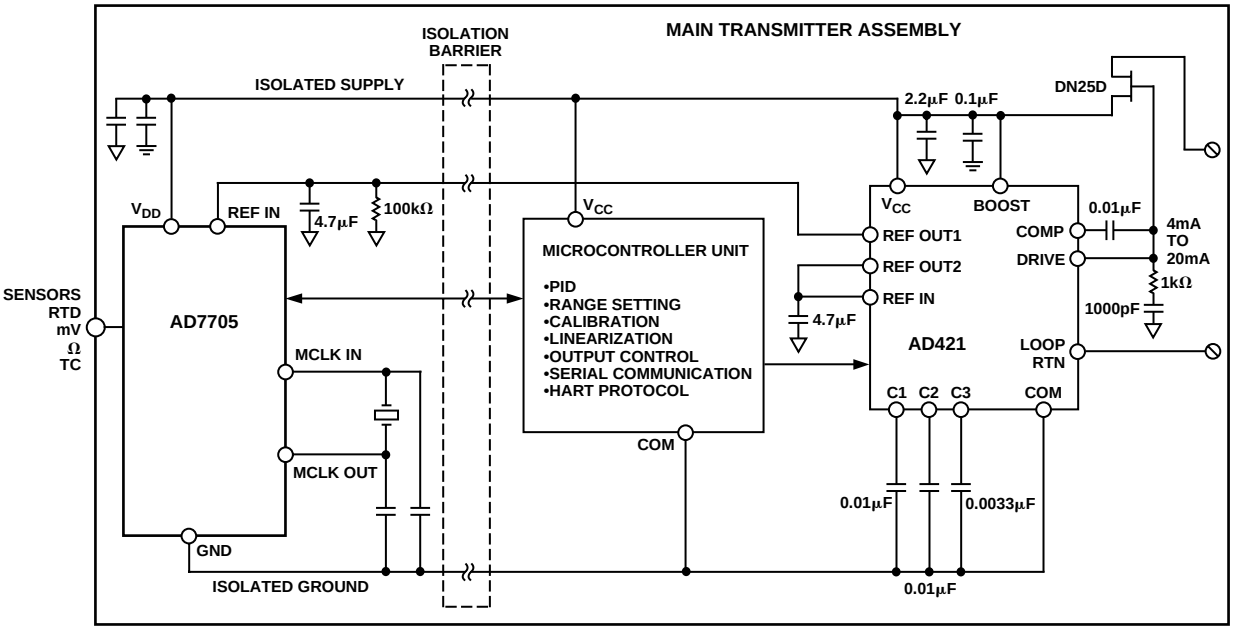


Figure 25. Smart Transmitter Using the AD7705

Battery Monitoring

Another area where the low power, single supply operation is a requirement is battery monitoring in portable equipment applications. Figure 26 shows a block diagram of a battery monitor that includes the AD7705 and an external multiplexer used to differentially measure the voltage across a single cell. The second channel on the AD7705 is used to monitor current drain from the battery. The AD7705 with its dual input channel is ideally suited to measurement systems requiring two input channels, as in this case, to monitor voltage and current. Since the AD7705 can accommodate very low input signals the R_{SENSE} can be kept low reducing undesired power dissipation. Operating with a gain of 128, a ±9.57 mV full-scale signal can be measured with a resolution of 2 μV, giving 13.5 bits of flicker-free performance in such a system. In order to obtain specified performance in unbuffered mode, the common mode range of the input is from GND to V_{DD} provided that the absolute value of the analog input voltage lies between GND – 30 mV and V_{DD} + 30 mV. Absolute voltages of GND – 200 mV can be accommodated on the AD7705 at 25°C without any degradation in performance, but leakage current increases significantly at elevated temperatures.

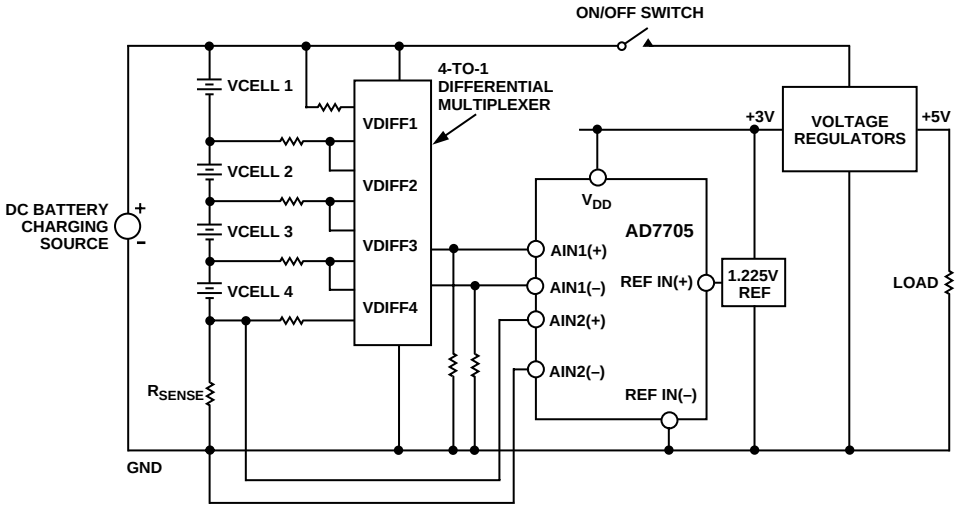
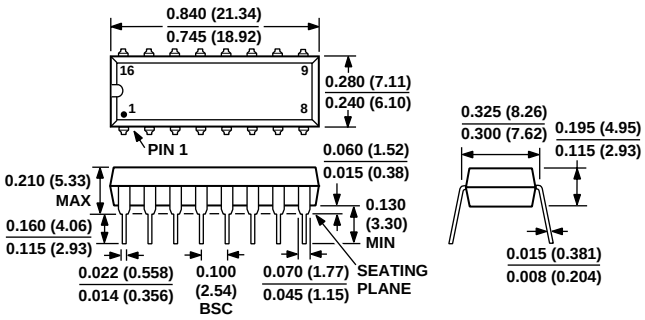


Figure 26. Battery Monitoring Using the AD7705

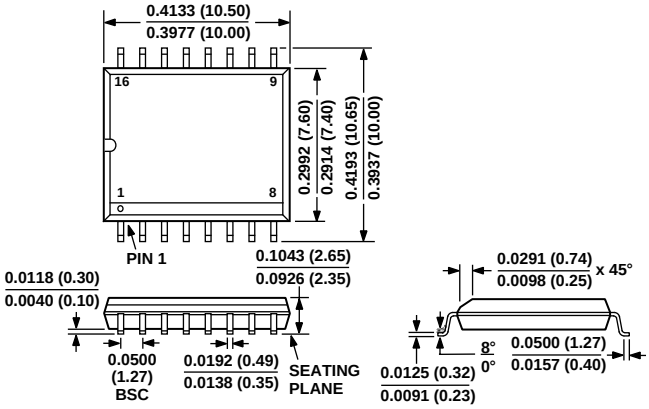
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

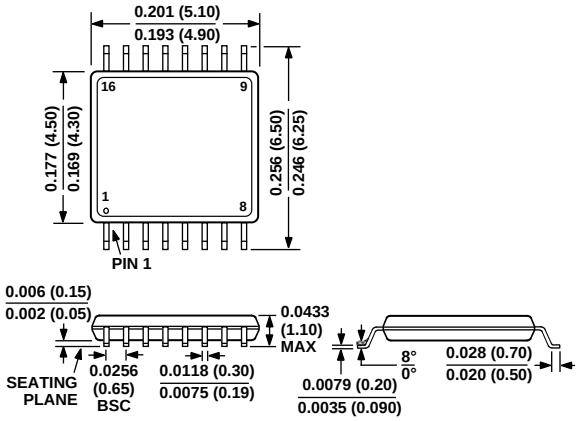
16-Pin Plastic DIP
(N-16)



16-Lead SOIC
(R-16)



16-Lead TSSOP
(RU-16)



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