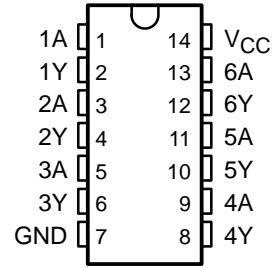


CD54ACT05, CD74ACT05 HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

SCHS311B – JANUARY 2001 – REVISED JUNE 2002

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT05 . . . F PACKAGE
CD74ACT05 . . . E OR M PACKAGE
(TOP VIEW)



description

The 'ACT05 devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$. The open-drain outputs require pullup resistors to perform correctly, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

ORDERING INFORMATION

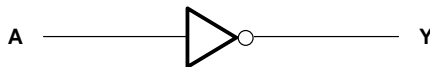
TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74ACT05E	CD74ACT05E
	SOIC – M	Tube	CD74ACT05M	ACT05M
		Tape and reel	CD74ACT05M96	
	CDIP – F	Tube	CD54ACT05F3A	CD54ACT05F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	Z

logic diagram, each inverter (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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CD54ACT05, CD74ACT05
HEX INVERTERS
WITH OPEN-DRAIN OUTPUTS
 SCHS311B – JANUARY 2001 – REVISED JUNE 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	80°C/W
M package	86°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C TO } 85^\circ\text{C}$		$-55^\circ\text{C TO } 125^\circ\text{C}$		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		2		V
V_{IL} Low-level input voltage		0.8		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	5.5	0	5.5	0	5.5	V
I_{OH} High-level output current		-24		-24		-24	mA
I_{OL} Low-level output current		24		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C TO } 85^\circ\text{C}$		$-55^\circ\text{C TO } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$	4.5 V	0.1	0.1	0.1		V	
		$I_{OL} = 24 \text{ mA}$	4.5 V	0.36	0.44	0.5			
		$I_{OL} = 50 \text{ mA}^\ddagger$	5.5 V			1.65			
		$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V		1.65				
I_I	$V_I = V_{CC}$ or GND	5.5 V	± 0.1	± 1	± 1	μA			
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	4	40	80	μA			
ΔI_{CC}	$V_I = V_{CC} - 2.1 \text{ V}$	4.5 V to 5.5 V	2.4	2.8	3	mA			
C_i			10	10	10	pF			

‡ Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- Ω transmission-line drive capability at 85°C and 75- Ω transmission-line drive capability at 125°C.



ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
A	0.18

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

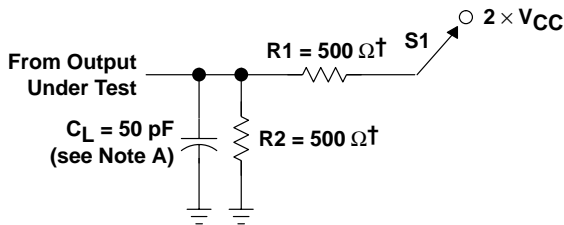
switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C		-55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PZL}	A or B	Y	2.4	8.5	2.3	9.3	ns
t_{PLZ}			2.8	9.8	2.7	10.8	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

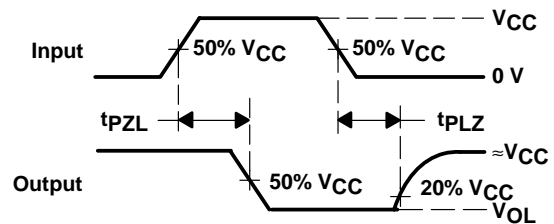
PARAMETER	TYP	UNIT
C_{pd} Power dissipation capacitance	105	pF

PARAMETER MEASUREMENT INFORMATION



† When $V_{CC} = 1.5\text{ V}$, $R1 = R2 = 1\text{ k}\Omega$

LOAD CIRCUIT



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9068601QCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD54ACT05F3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD74ACT05E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74ACT05M	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT05M96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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