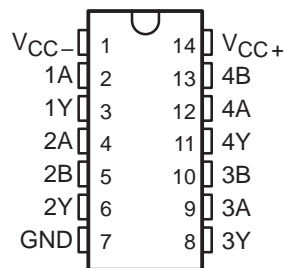


# SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS033F – JANUARY 1988 – REVISED MARCH 1997

- **Bi-MOS Technology With TTL and CMOS Compatibility**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Quiescent Current . . . 95  $\mu$ A Typ**  
 **$V_{CC\pm} = \pm 12$  V**
- **Current-Limited Outputs . . . 10 mA Typ**
- **CMOS-and TTL-Compatible Inputs**
- **On-Chip Slew Rate Limited to 30 V/ $\mu$ s max**
- **Flexible Supply Voltage Range**
- **Characterized at  $V_{CC\pm}$  of  $\pm 4.5$  V and  $\pm 15$  V**
- **Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88**

**D, DB†, OR N PACKAGE  
(TOP VIEW)**



† The DB package is only available left-end taped and reeled, i.e., order device SN75C188DBLE.

## description

The SN75C188 is a monolithic, low-power, quadruple line driver that interfaces data terminal equipment with data communications equipment. This device is designed to conform to ANSI Standard EIA/TIA-232-E.

An external diode in series with each supply-voltage terminal is needed to protect the SN75C188 under certain fault conditions to comply with EIA/TIA-232-E.

The SN75C188 is characterized for operation from 0°C to 70°C.

## Function Tables

**DRIVER 1**

B	Y
H	L
L	H

**DRIVERS 2 – 4**

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,  
X = don't care



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

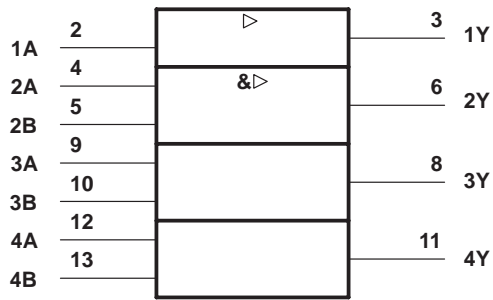
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# SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

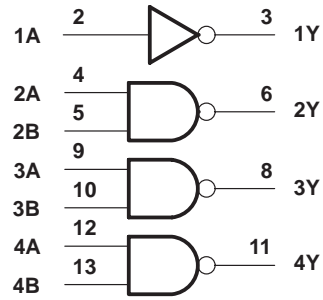
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## logic symbol†



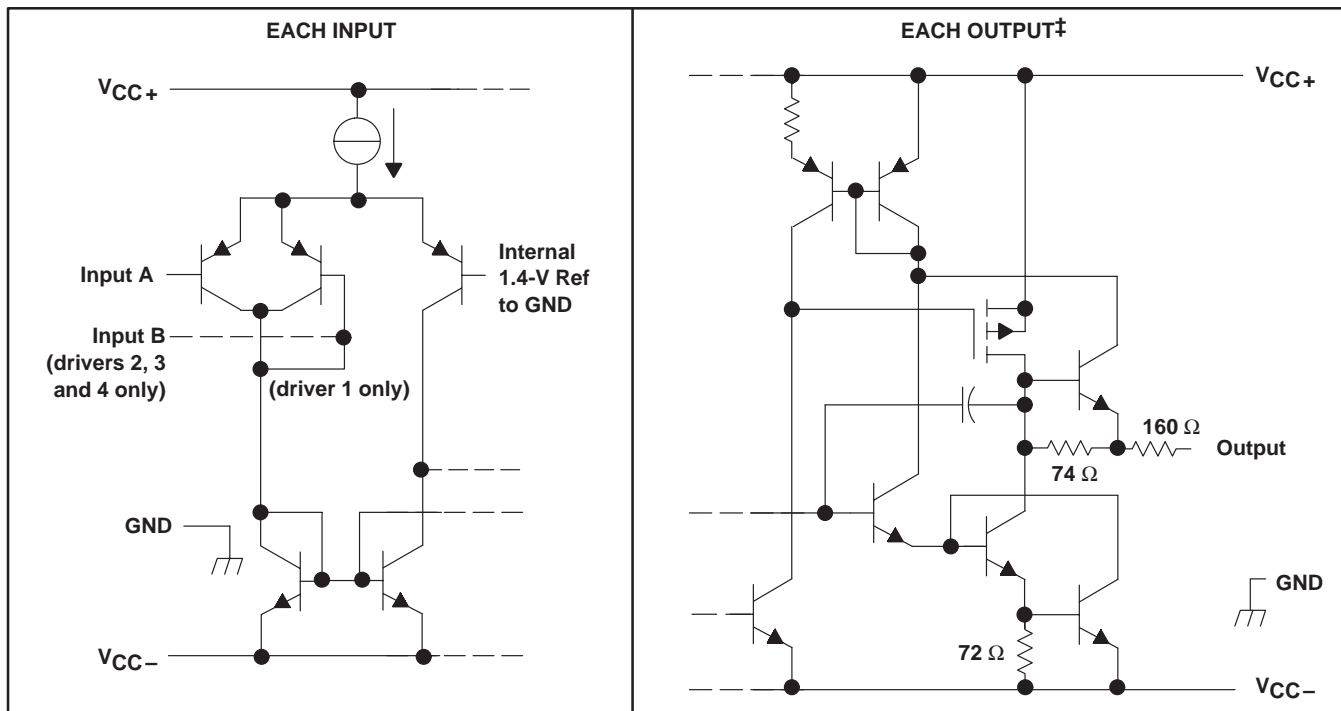
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



positive logic  
 $Y = \bar{A}$  (driver 1)  
 $Y = \bar{A}\bar{B}$  or  $\bar{A} + \bar{B}$  (drivers 2 through 4)

## schematics of inputs and outputs



‡ All resistor values shown are nominal.

# SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1) .....	15 V
Supply voltage, $V_{CC-}$ (see Note 1) .....	-15 V
Input voltage range, $V_I$ .....	$V_{CC-}$ to $V_{CC+}$
Output voltage range, $V_O$ .....	$V_{CC-} - 6\text{ V}$ to $V_{CC+} + 6\text{ V}$
Continuous total power dissipation .....	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ .....	0°C to 70°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
DB	525 mW	4.2 mW/°C	336 mW
N	1150 mW	9.2 mW/°C	736 mW

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC+}$	4.5	12	15	V
Supply voltage, $V_{CC-}$	-4.5	-12	-15	V
Input voltage, $V_I$	$V_{CC-} + 2$		$V_{CC+}$	V
High-level Input voltage, $V_{IH}$	2			V
Low-level Input voltage, $V_{IL}$			0.8	V
Operating free-air temperature, $T_A$	0		70	°C



# SN75C188

## QUADRUPLE LOW-POWER LINE DRIVERS

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**electrical characteristics over operating free-air temperature range,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = -12\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
$V_{OH}$	High-level output voltage	$V_{IL} = 0.8\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	4			V	
			$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	10				
$V_{OL}$	Low-level output voltage (see Note 2)	$V_{IH} = 2\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	-4			V	
			$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	-10				
$I_{IH}$	High-level input current	$V_I = 5\text{ V}$		10			$\mu\text{A}$	
$I_{IL}$	Low-level input current	$V_I = 0$		-10			$\mu\text{A}$	
$I_{OS(H)}$	High-level short-circuit output current‡	$V_I = 0.8\text{ V}$ , $V_O = 0$ or $V_{CC-}$			-5.5	-10	-19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	$V_I = 2\text{ V}$ , $V_O = 0$ or $V_{CC+}$			5.5	10	19.5	mA
$r_O$	Output resistance, power off	$V_{CC+} = 0$ , $V_{CC-} = 0$ , $V_I = -2\text{ V}$ to $2\text{ V}$			300			$\Omega$
$I_{CC+}$	Supply current from $V_{CC+}$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$ , No load	All inputs at 2 V or 0.8 V		90	160		$\mu\text{A}$
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$ , No load	All inputs at 2 V or 0.8 V		95	160		
$I_{CC-}$	Supply current from $V_{CC-}$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$ , No load	All inputs at 2 V or 0.8 V		-90	-160		$\mu\text{A}$
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$ , No load	All inputs at 2 V or 0.8 V		-95	-160		

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only; e.g., if  $-4\text{ V}$  is a maximum, the typical value is a more negative voltage.

**switching characteristics,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = -12\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$t_{PLH}$	Propagation delay time, low- to high-level output§	$R_L = 3\text{ k}\Omega$ , See Figure 1	$C_L = 15\text{ pF}$	3			$\mu\text{s}$	
$t_{PHL}$	Propagation delay time, high- to low-level output§			3.5			$\mu\text{s}$	
$t_{TLH}$	Transition time, low- to high-level output¶			0.53	3.2		$\mu\text{s}$	
$t_{THL}$	Transition time, high- to low-level output¶			0.53	3.2		$\mu\text{s}$	
$t_{TLH}^{\#}$	Transition time, low- to high-level output#	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See Figure 1	$C_L = 2500\text{ pF}$	1.5			$\mu\text{s}$	
$t_{THL}^{\#}$	Transition time, high- to low-level output#			1.5			$\mu\text{s}$	
SR	Output slew rate§	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 15\text{ pF}$			6	15	30	$\text{V}/\mu\text{s}$

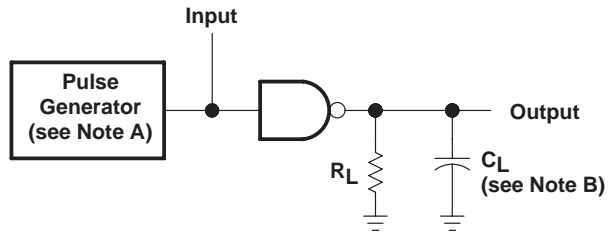
§ Measured at the 50% level

¶ Measured between the 10% and 90% points on the output waveform

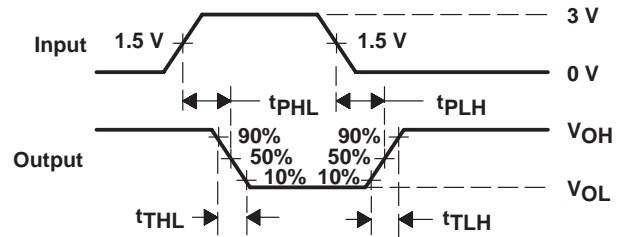
# Measured between the 3-V and  $-3\text{ V}$  points on the output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low



PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f \leq 50 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

# SN75C188 QUADRUPLE LOW-POWER LINE DRIVERS

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## TYPICAL CHARACTERISTICS

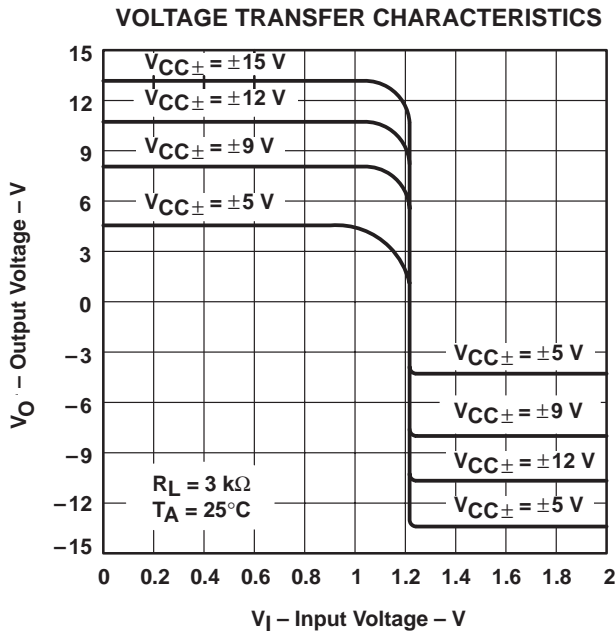


Figure 2

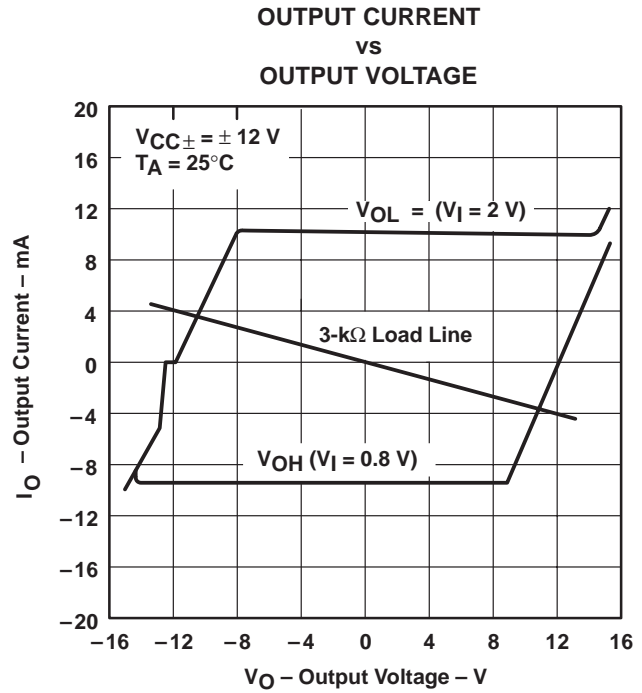


Figure 3

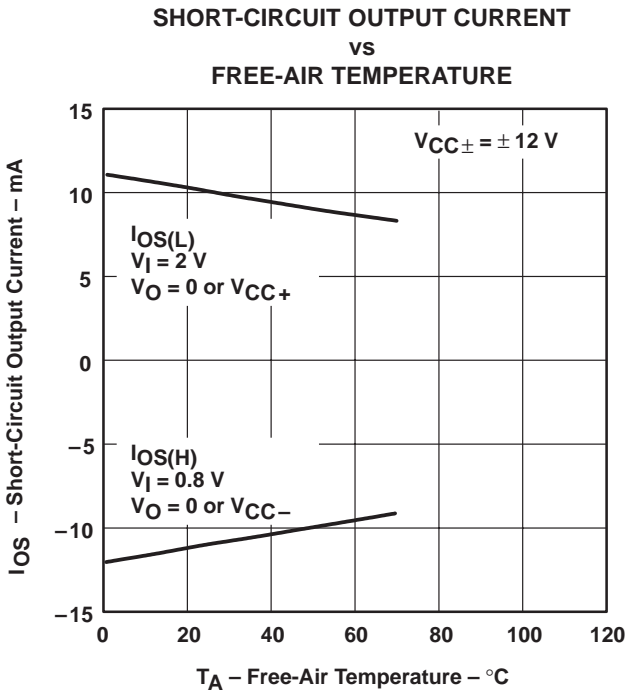


Figure 4

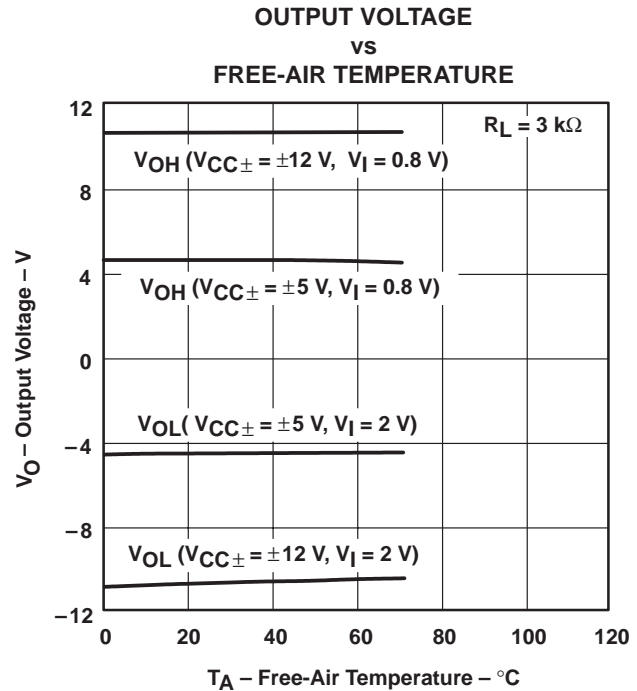


Figure 5



TYPICAL CHARACTERISTICS

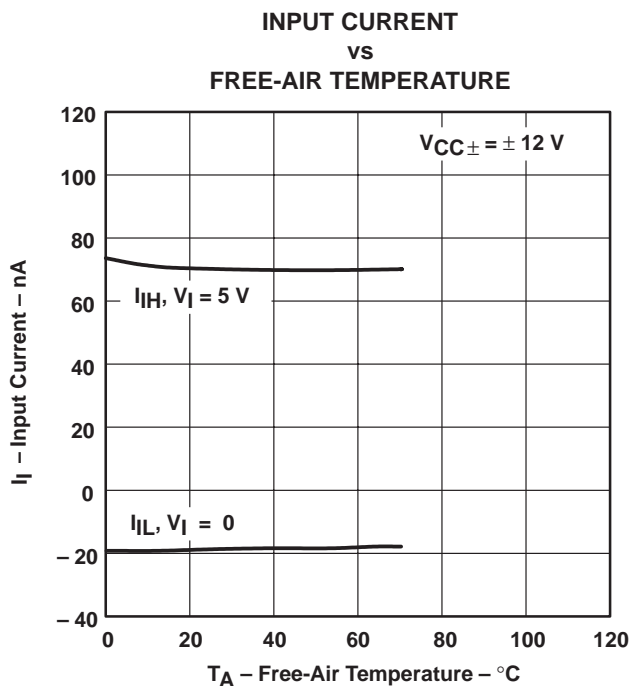


Figure 6

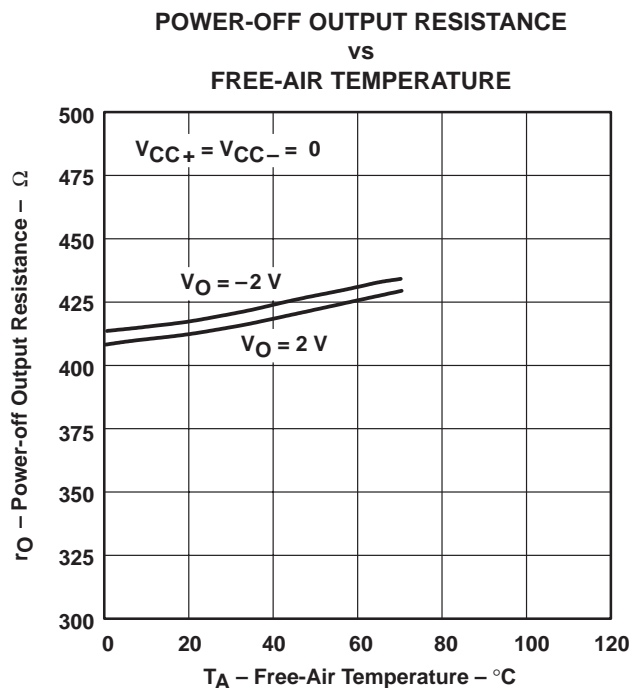


Figure 7

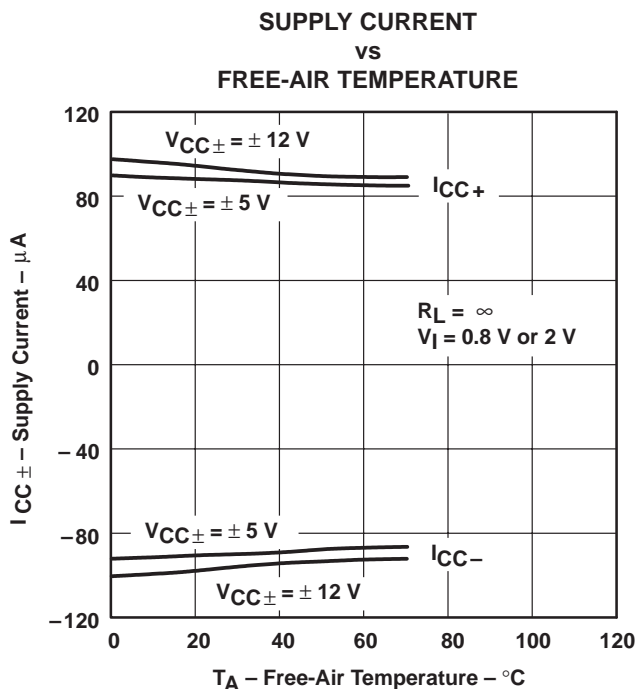


Figure 8

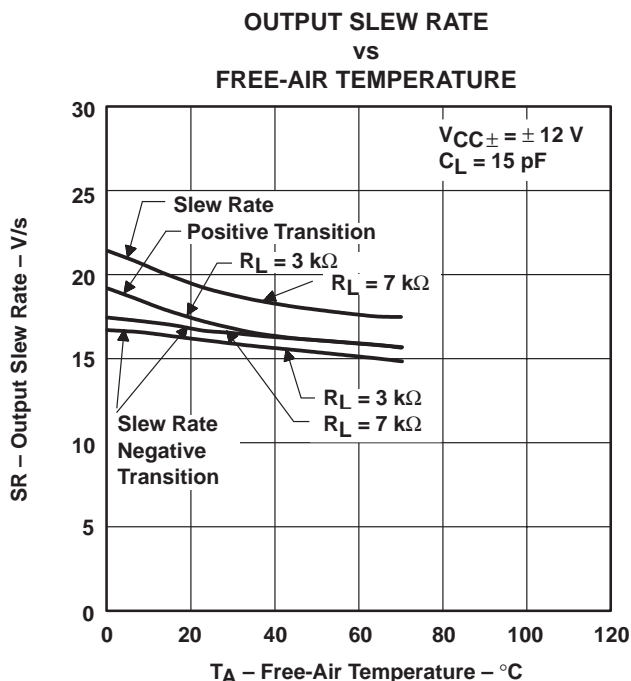


Figure 9

TYPICAL CHARACTERISTICS

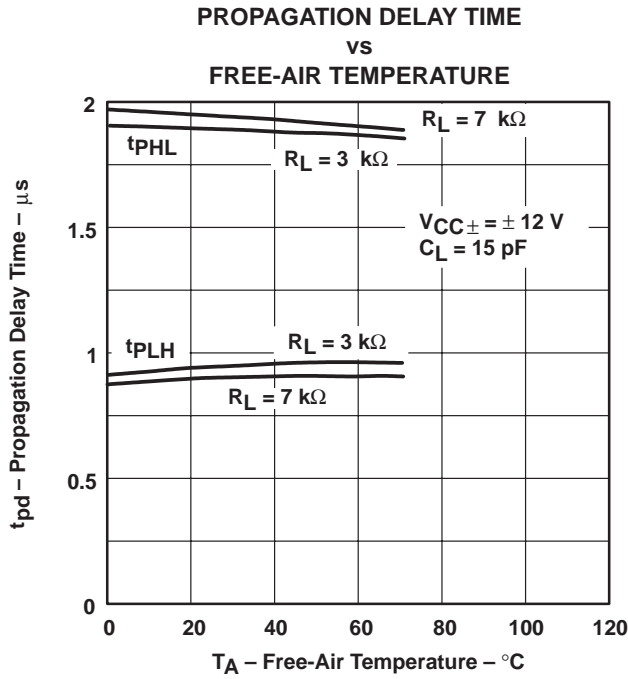


Figure 10

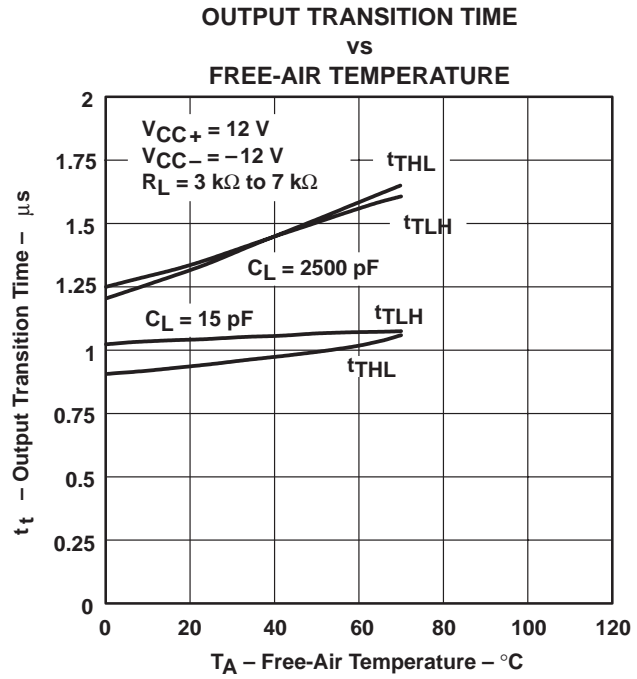


Figure 11

APPLICATION INFORMATION

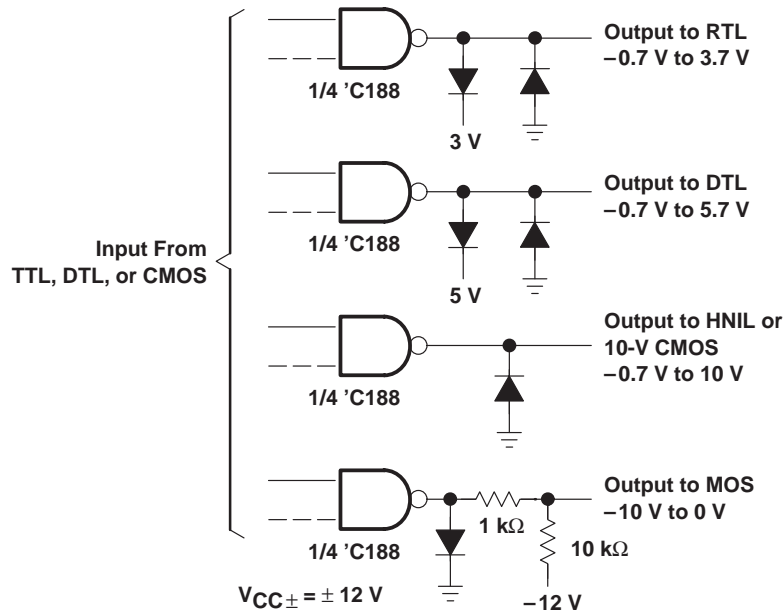
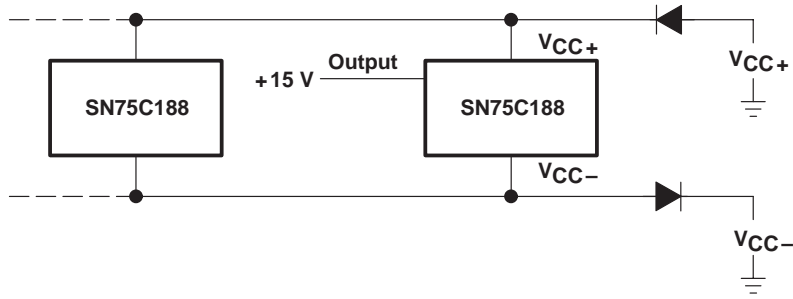


Figure 12. Logic Translator Applications



APPLICATION INFORMATION



NOTE A: External diodes placed in series with the  $V_{CC+}$  and  $V_{CC-}$  leads protect the SN75C188 in the fault condition where the device outputs are shorted to  $\pm 15$  V and the power supplies are at low voltage and provide low-impedance paths to GND.

Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA/TIA-232-E

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