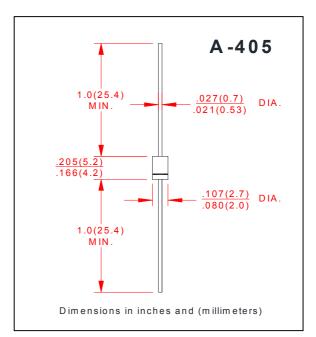


## DB3 - DB4

## **FEATURES**

 The three layer, two terminal, axial lead, hermetically sealed diacs are designed Specifically for triggering thyristors. They demonstrate low breakover current at breakover voltage as they withstand peak pulse current. The breakover symmetry is within three volts. These diacs are intended for use in thyristors phase control, circuits for lamp dimming, universal motor speed control, and heat control. TY'S DB3/DB4 are bidirectional trigged diode designed to operate in conjunction

With Triacs and SCR's.



## MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

• Ratings at 25°C ambient temperature unless otherwise specified

Parameters	<b>Test Conditions</b>	SYMBOLS		DB3	DB4	UNITS
Power Dissipation on Printed Circuit(L=10mm)	T <sub>A</sub> =50°C	P <sub>C</sub>		150		mW
Repetitive Peak in-state Current	tp=10µS, F=100Hz	I <sub>TRM</sub>		2.0		А
Breakover Voltage(Note2)	c=22nF(Note2) See diagram1	$V_{BO}$	Min	28	35	V
			Тур	32	40	
			Max	36	45	
Breakover Voltage Symmetry	c=22nF(Note2) See diagram1	$\begin{array}{c}  + V_{BO} -\\  -V_{BO}  \end{array}$	Max	±3		V
Dynamic Breakover Voltage (Note1)	$ \begin{array}{c} & \Delta I = (I_{BO} \text{ to} \\ & I_F = 10 \text{ mA}) \\ \text{See diagram1} \end{array} $	$ \pm \Delta \mathbf{V} $	Min	5		V
Output Voltage(Note1)	See diagram2	Vo	Min	5		V
Breakover Current (Note1)	c=22nF (Note2)	I <sub>BO</sub>	Max	100		μA
Rise Time(Note1)	See diagram 3	tr	Тур	1.5		μS
Leakage Current(Note1)	V <sub>B</sub> =0.5V <sub>BO</sub> max see diagram1	I <sub>B</sub>	Max	10		μΑ
Operating and Storage Temperature Range		T <sub>J</sub> ,T <sub>STG</sub>		-40 to +110/-40 to +125		C
Thermal Resistance Junction to ambient		$R_{\theta JA}$		400		°C/W
Thermal Resistance Junction to Lead		$R_{\theta JL}$		150		°C/W

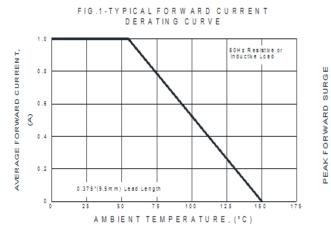
## Notes:

1. Eiectrical characteristics applicable in both forward and reverse directions

2.Connected in parallel with the devices



DB3 - DB4



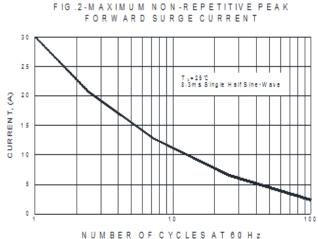


FIG .3 - TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

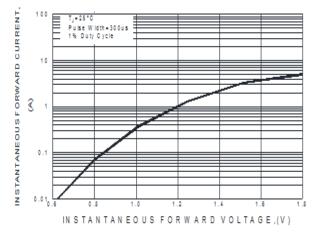
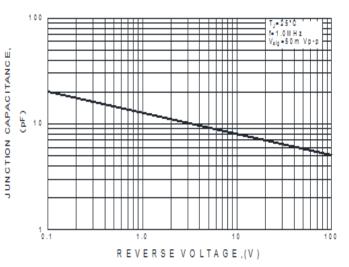


FIG.5-TYPICAL JUNCTION CAPACITANCE



F1G.6-TEST CIRCUIT DIAGRAM AND FORWARD SURGE CURRENT

