ANALOG DEVICES

Single Supply, Rail to Rail Low Power FET-Input Op Amp

AD820

FEATURES
True Single Supply Operation
- **Output Swings Rail-to-Rail**
- **Input Voltage Range Extends Below Ground**
- **Single Supply Capability from +3 V to +36 V**
- **Dual Supply Capability from ±1.5 V to ±18 V**

Excellent Load Drive
- **Capacitive Load Drive Up to 350 pF**
- **Minimum Output Current of 15 mA**

Excellent AC Performance for Low Power
- **800 μA Max Quiescent Current**
- **Unity Gain Bandwidth: 1.8 MHz**
- **Slew Rate of 3.0 V/μs**

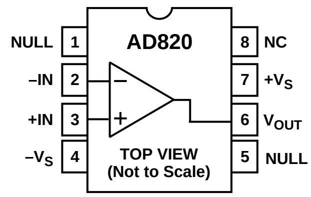
Excellent DC Performance
- **800 μV Max Input Offset Voltage**
- **1 μV/°C Typ Offset Voltage Drift**
- **25 pA Max Input Bias Current**

Low Noise
- **13 nV/√Hz @ 10 kHz**

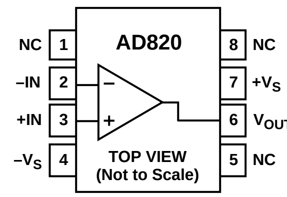
APPLICATIONS
Battery Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

CONNECTION DIAGRAMS

8-Lead Plastic Mini-DIP



8-Lead SOIC



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD820 is a precision, low power FET input op amp that can operate from a single supply of +3.0 V to 36 V, or dual supplies of ±1.5 V to ±18 V. It has true single supply capability with an input voltage range extending below the negative rail, allowing the AD820 to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.

Offset voltage of 800 μV max, offset voltage drift of 1 μV/°C, typ input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz and 3 V/μs slew rate are provided for a low supply current of 800 μA. The AD820 drives up to 350 pF of direct capacitive load and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

The AD820 is available in three performance grades. The A and B grades are rated over the industrial temperature range of –40°C to +85°C. There is 3 V grade—the AD820A-3V, rated over the industrial temperature range.

The AD820 is offered in two varieties of 8-lead package: plastic DIP, and surface mount (SOIC).

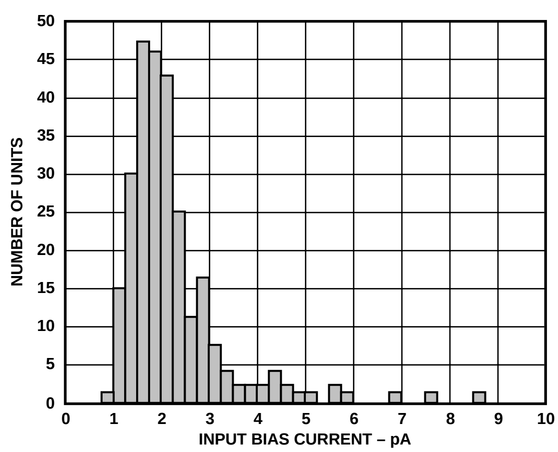


Figure 1. Typical Distribution of Input Bias Current

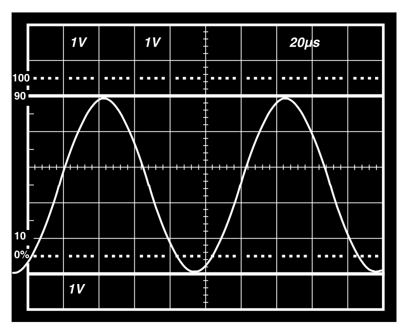


Figure 2. Gain of +2 Amplifier; V_S = +5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 Volts

REV. B

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AD820–SPECIFICATIONS (V_S = 0, 5 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_O = 0 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V							
	R_L = 100k	400	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10k	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1k	15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k to 2.5 V							
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4		μs
to 0.01%			1.8			1.8		μs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–0.2		4	–0.2		4	V
T_{MIN} to T_{MAX}		–0.2		4	–0.2		4	V
CMRR	V_{CM} = 0 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω‖pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL}–V_{EE}$	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL}–V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL}–V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			25			25		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		620	800		620	800	μA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		dB
T_{MIN} to T_{MAX}		70			66			dB

(V_S = +5 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.3	0.4	mV
Max Offset over Temperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_{CM} = –5 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 4 V to –4 V							
	R_L = 100k	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10k	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1k	20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k							
f = 10 kHz	V_O = ±4.5 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.8		MHz
Full Power Response	V_O p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4		μs
to 0.01%			1.8			1.8		μs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–5.2		4	–5.2		4	V
T_{MIN} to T_{MAX}		–5.2		4	–5.2		4	V
CMRR	V_{CM} = –5 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω‖pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL}–V_{EE}$	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL}–V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL}–V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			30			30		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		650	800		620	800	μA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

AD820–SPECIFICATIONS (V_S = ±15 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.0	mV
Max Offset over Temperature			0.5	3		0.5	2	mV
Offset Drift			2			2		μV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	10	pA
	V_{CM} = –10 V		40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = +10 V to –10 V							
	R_L = 100k	500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}		500			500			V/mV
	R_L = 10k	100	500		100	500		V/mV
T_{MIN} to T_{MAX}		100			100			V/mV
	R_L = 1k	30	45		30	45		V/mV
T_{MIN} to T_{MAX}		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		μV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k							
f = 10 kHz	V_O = ±10 V		–85			–85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/μs
Settling Time								
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1		μs
to 0.01%			4.5			4.5		μs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–15.2		14	–15.2		14	V
T_{MIN} to T_{MAX}		–15.2		14	–15.2		14	V
CMRR	V_{CM} = –15 V to 12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}		70			74			dB
Input Impedance								
Differential			10^{13}‖0.5			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
$V_{OL}–V_{EE}$	I_{SINK} = 20 μA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 20 μA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
$V_{OL}–V_{EE}$	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
$V_{OL}–V_{EE}$	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
$V_{CC}–V_{OH}$	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Short Circuit Current			45			45		mA
Capacitive Load Drive			350			350		
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		700	900		700	900	μA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

(V_S = 0, 3 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A-3V Min	Typ	Max	Units
DC PERFORMANCE					
Initial Offset			0.2	1	mV
Max Offset over Temperature			0.5	1.5	mV
Offset Drift			1		µV/°C
Input Bias Current	V_{CM} = 0 V to +2 V		2	25	pA
at T_{MAX}			0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 2 V				
	R_L = 100k	300	1000		V/mV
T_{MIN} to T_{MAX}		400			V/mV
	R_L = 10k	60	150		V/mV
T_{MIN} to T_{MAX}		80			V/mV
	R_L = 1k	10	30		V/mV
T_{MIN} to T_{MAX}		8			V/mV
NOISE/HARMONIC PERFORMANCE					
Input Voltage Noise					
0.1 Hz to 10 Hz			2		µV p-p
f = 10 Hz			25		nV/√Hz
f = 100 Hz			21		nV/√Hz
f = 1 kHz			16		nV/√Hz
f = 10 kHz			13		nV/√Hz
Input Current Noise					
0.1 Hz to 10 Hz			18		fA p-p
f = 1 kHz			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k to 1.5 V				
f = 10 kHz	V_O = ±1.25 V		–92		dB
DYNAMIC PERFORMANCE					
Unity Gain Frequency			1.5		MHz
Full Power Response	V_O p-p = 2.5 V		240		kHz
Slew Rate			3		V/µs
Settling Time					
to 0.1%	V_O = 0.2 V to 2.5 V		1		µs
to 0.01%			1.4		µs
INPUT CHARACTERISTICS					
Common-Mode Voltage Range[1]		–0.2		2	V
T_{MIN} to T_{MAX}		–0.2		2	V
CMRR	V_{CM} = 0 V to +1 V	60	74		dB
T_{MIN} to T_{MAX}		60			dB
Input Impedance					
Differential			10^{13}‖0.5		Ω‖pF
Common Mode			10^{13}‖2.8		Ω‖pF
OUTPUT CHARACTERISTICS					
Output Saturation Voltage[2]					
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7	mV
T_{MIN} to T_{MAX}				10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14	mV
T_{MIN} to T_{MAX}				20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55	mV
T_{MIN} to T_{MAX}				80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110	mV
T_{MIN} to T_{MAX}				160	mV
V_{OL}–V_{EE}	I_{SINK} = 10 mA		200	400	mV
T_{MIN} to T_{MAX}				400	mV
V_{CC}–V_{OH}	I_{SOURCE} = 10 mA		500	1000	mV
T_{MIN} to T_{MAX}				1000	mV
Operating Output Current		15			mA
T_{MIN} to T_{MAX}		12			mA
Short Circuit Current		18	25		mA
T_{MIN} to T_{MAX}		15			mA
Capacitive Load Drive			350		pF
POWER SUPPLY					
Quiescent Current	T_{MIN} to T_{MAX}		620	800	µA
Power Supply Rejection	V_S+ = 3 V to 15 V	70	80		dB
T_{MIN} to T_{MAX}		70			dB

AD820–SPECIFICATIONS

NOTES

[1]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range (+ V_S – 1 V) to +V_S. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 volt below the positive supply.

[2]V_{OL}–V_{EE} is defined as the difference between the lowest possible output voltage (V_{OL}) and the minus voltage supply rail (V_{EE}). V_{CC}–V_{OH} is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V

Internal Power Dissipation[2]

  Plastic DIP (N) . . . . 1.6 Watts

  SOIC (R) . . . . 1.0 Watts

Input Voltage . . . . (+V_S + 0.2 V) to – (20 V + V_S)

Output Short Circuit Duration . . . . Indefinite

Differential Input Voltage . . . . ±30 V

Storage Temperature Range (N) . . . . –65°C to +125°C

Storage Temperature Range (R) . . . . –65°C to +150°C

Operating Temperature Range

  AD820A/B . . . . –40°C to +85°C

Lead Temperature Range

  (Soldering 60 sec) . . . .+260°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Lead Plastic DIP Package: θ_{JA} = 90°C/Watt
8-Lead SOIC Package: θ_{JA} = 160°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD820AN	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8
AD820BN	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8
AD820AR	–40°C to +85°C	8-Lead SOIC	R-8
AD820BR	–40°C to +85°C	8-Lead SOIC	R-8
AD820AR-3V	–40°C to +85°C	8-Lead SOIC	R-8
AD820AN-3V	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

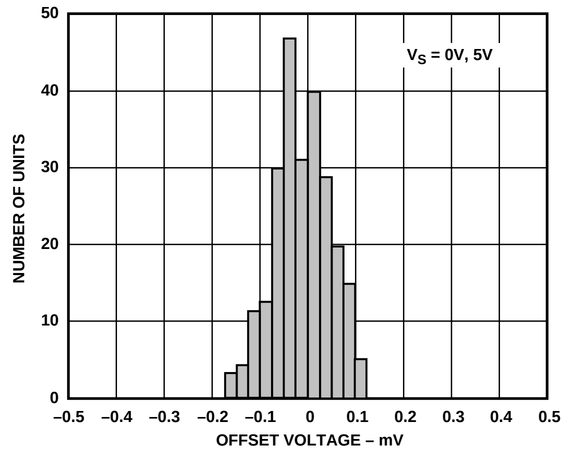


Figure 3. Typical Distribution of Offset Voltage (248 Units)

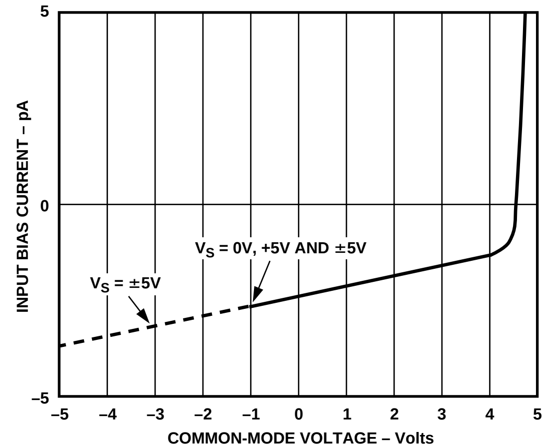


Figure 6. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V

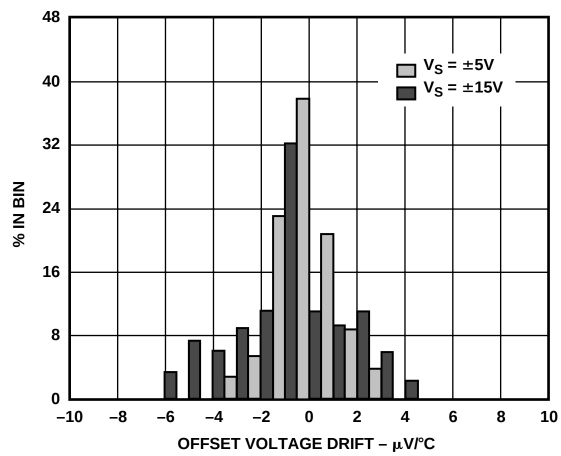


Figure 4. Typical Distribution of Offset Voltage Drift (120 Units)

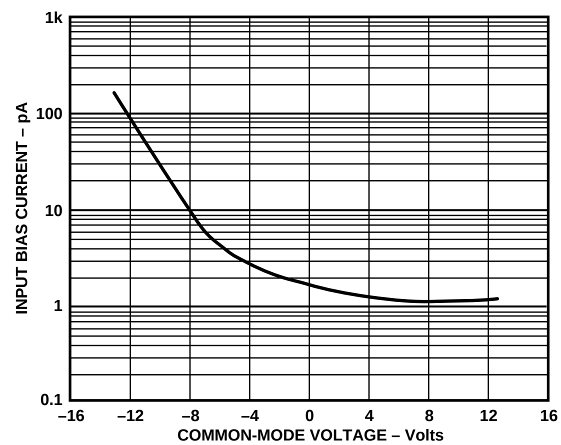


Figure 7. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V

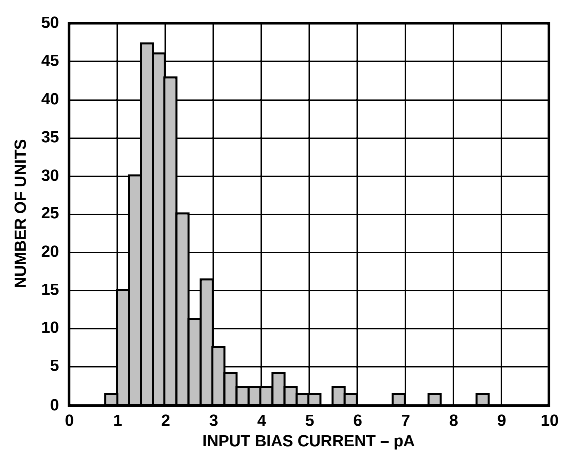


Figure 5. Typical Distribution of Input Bias Current (213 Units)

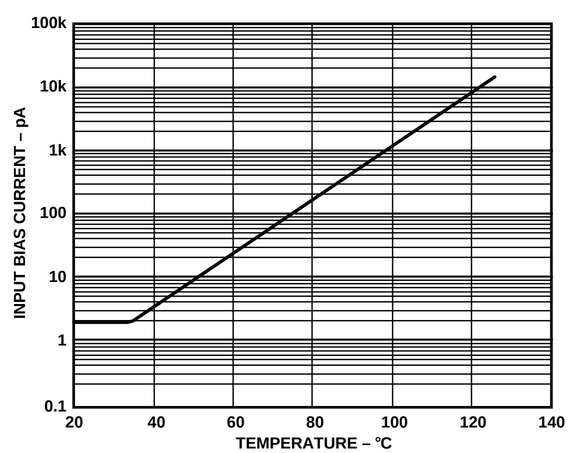


Figure 8. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0

AD820–Typical Characteristics

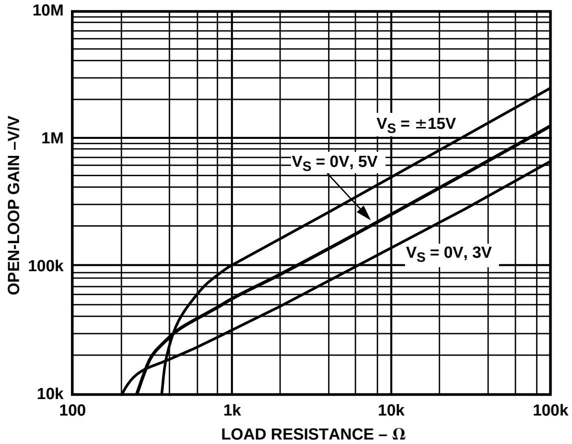


Figure 9. Open-Loop Gain vs. Load Resistance

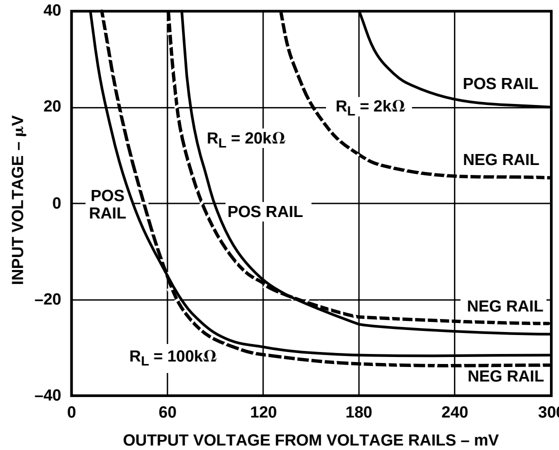


Figure 12. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; V_S = ±5 V

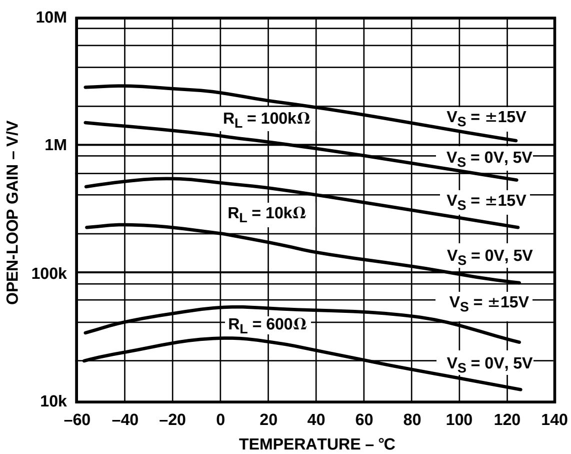


Figure 10. Open-Loop Gain vs. Temperature

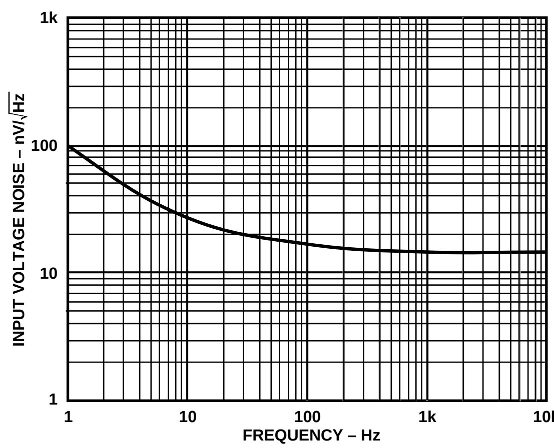


Figure 13. Input Voltage Noise vs. Frequency

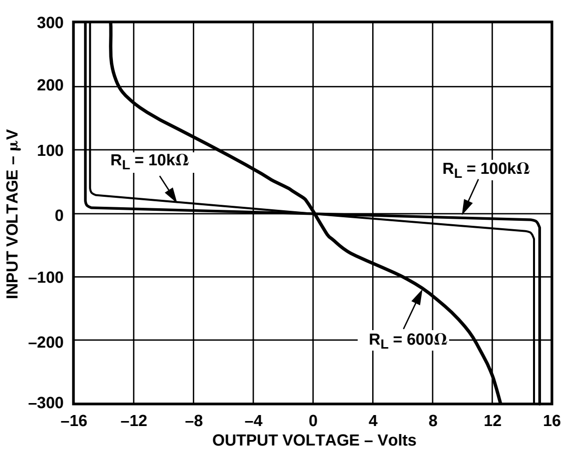


Figure 11. Input Error Voltage vs. Output Voltage for Resistive Loads

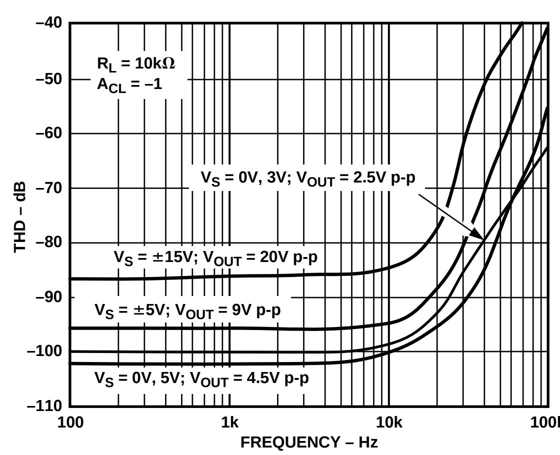


Figure 14. Total Harmonic Distortion vs. Frequency

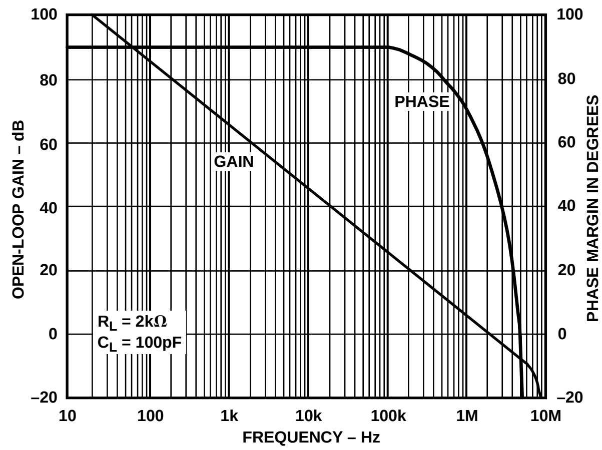


Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

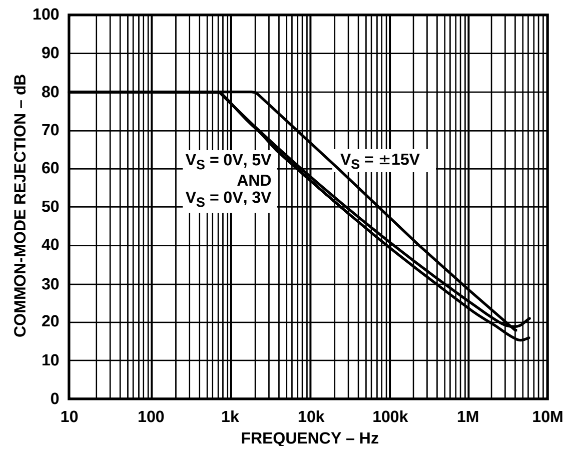


Figure 18. Common-Mode Rejection vs. Frequency

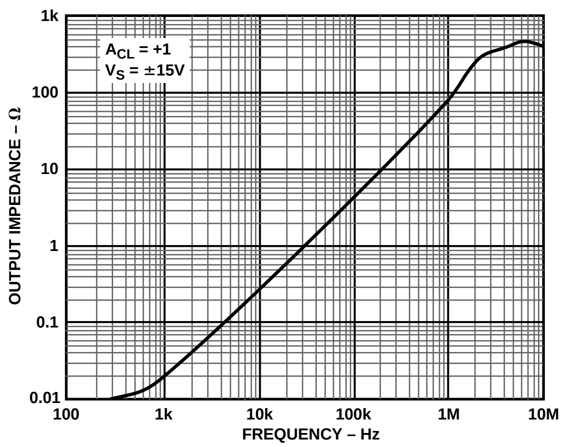


Figure 16. Output Impedance vs. Frequency

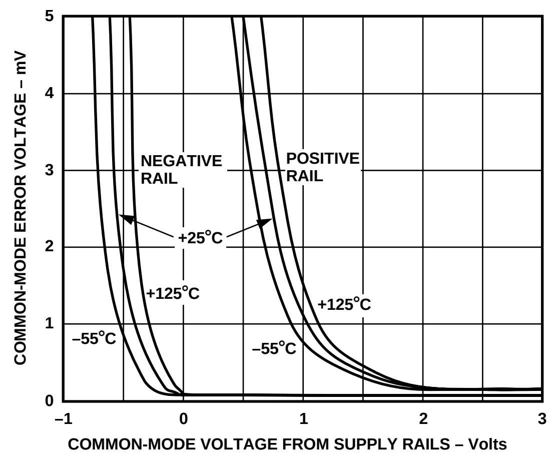


Figure 19. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S - V_{CM}$)

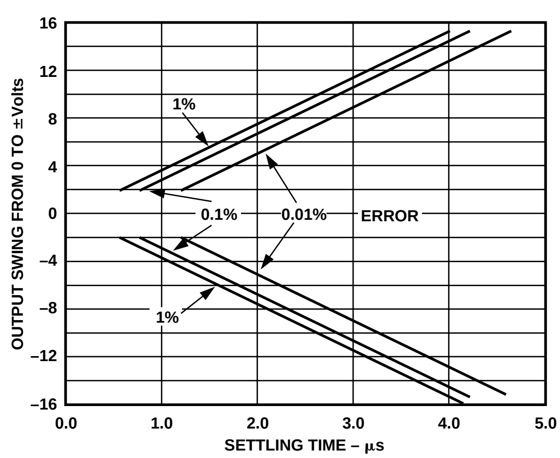


Figure 17. Output Swing and Error vs. Settling Time

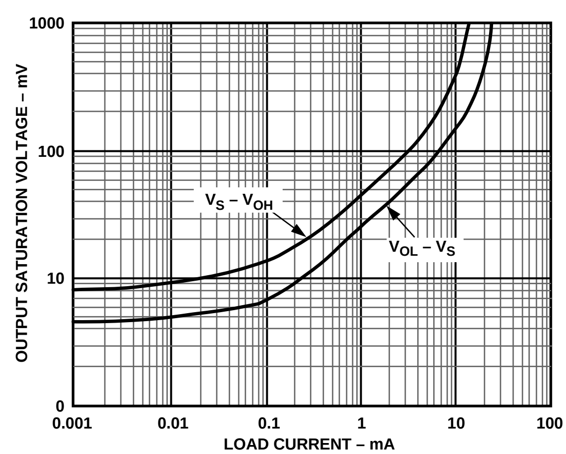


Figure 20. Output Saturation Voltage vs Load Current

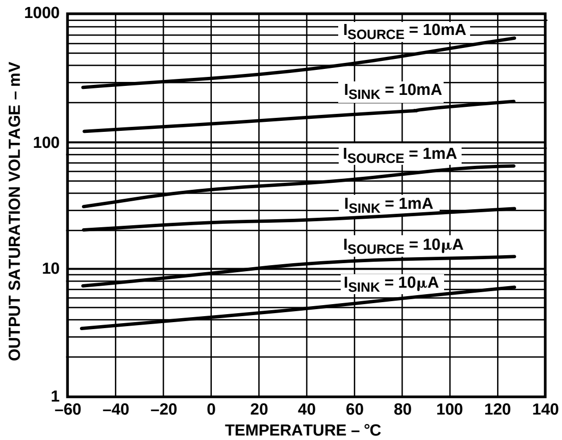


Figure 21. Output Saturation Voltage vs. Temperature

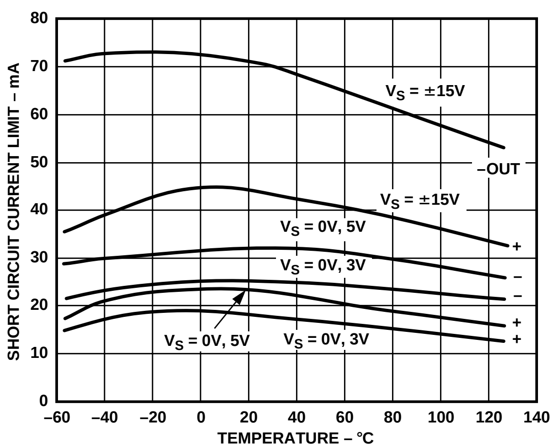


Figure 22. Short Circuit Current Limit vs. Temperature

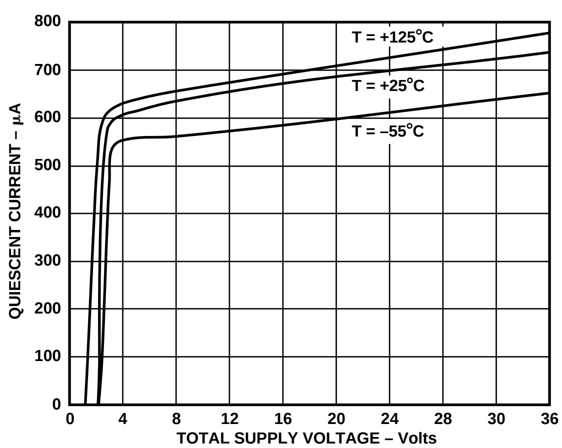


Figure 23. Quiescent Current vs. Supply Voltage vs. Temperature

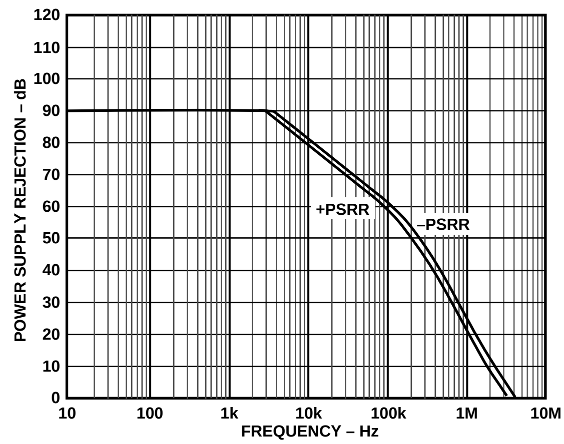


Figure 24. Power Supply Rejection vs. Frequency

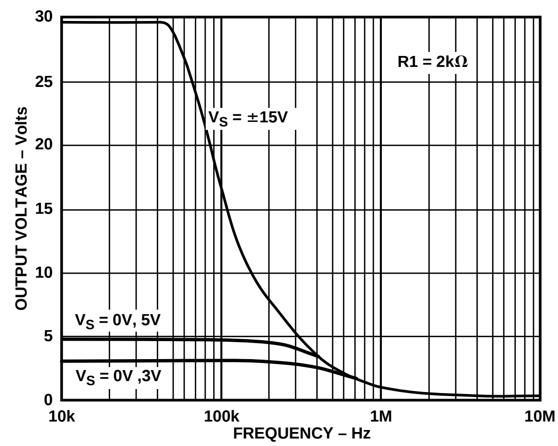


Figure 25. Large Signal Frequency Response

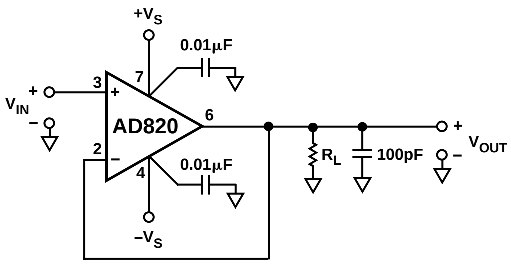


Figure 26. Unity-Gain Follower

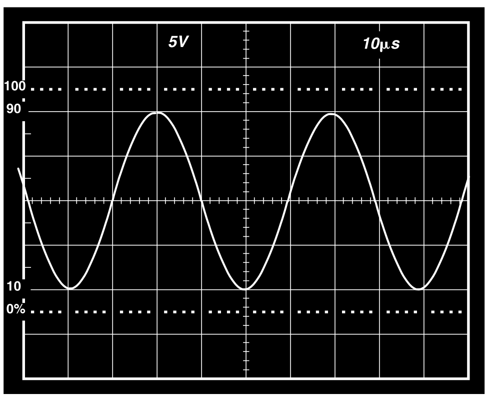


Figure 27. 20 V, 25 kHz Sine Input; Unity Gain Follower; R_L = 600 Ω, V_S = ±15 V

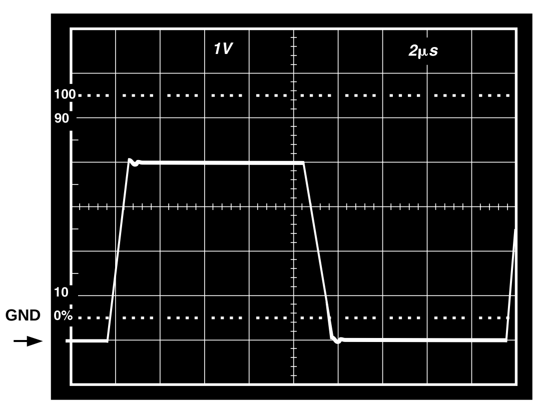


Figure 28. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step

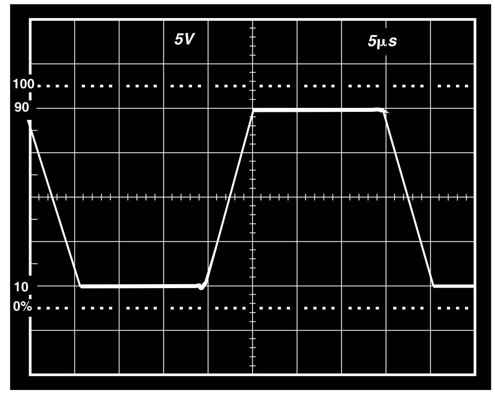


Figure 29. Large Signal Response Unity Gain Follower; V_S = ±15 V, R_L = 10 kΩ

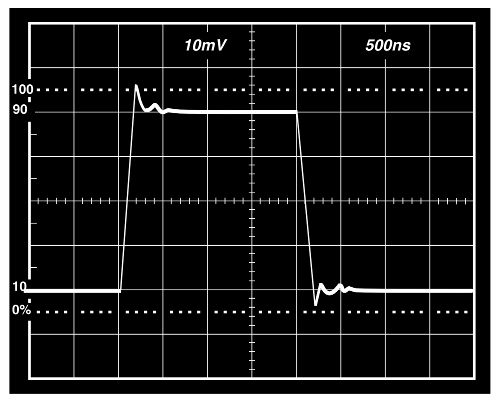


Figure 30. Small Signal Response Unity Gain Follower; V_S = ±15 V, R_L = 10 kΩ

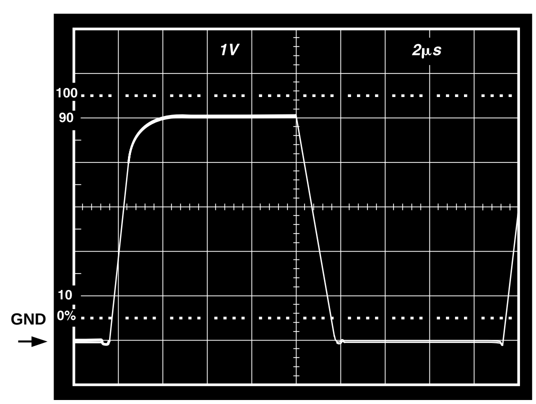


Figure 31. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

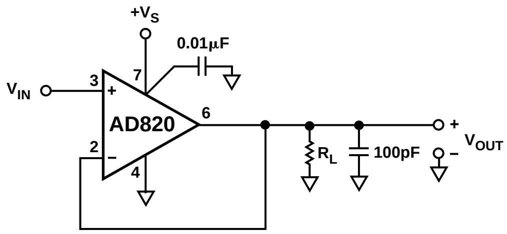


Figure 32. Unity-Gain Follower

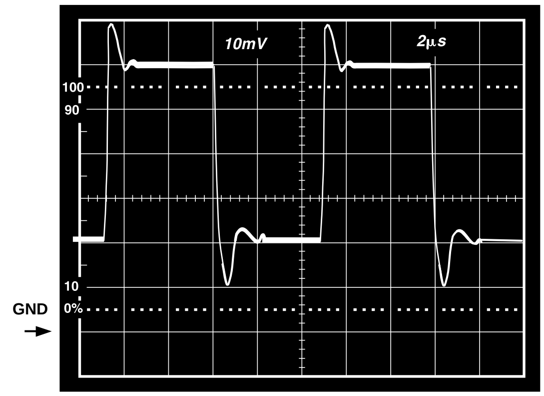


Figure 35. V_S = +5 V, 0 V; Unity Gain Follower Response to 40 mV Step Centered 40 mV Above Ground

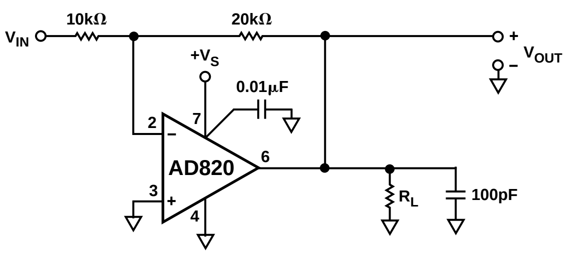


Figure 33. Gain of Two Inverter

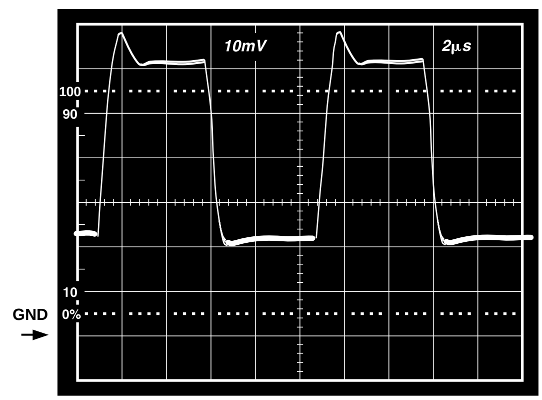


Figure 36. V_S = +5 V, 0 V; Gain of Two Inverter Response to 20 mV Step, Centered 20 mV Below Ground

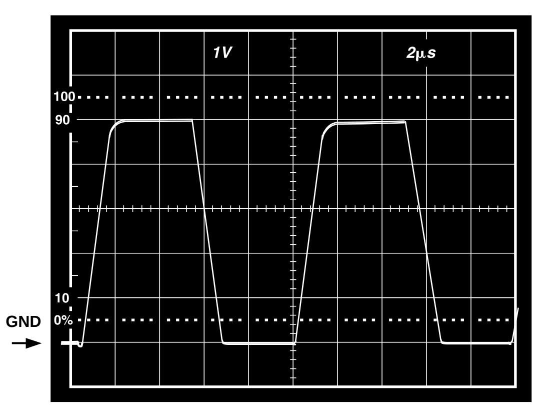


Figure 34. V_S = +5 V, 0 V; Gain of Two Inverter Response to 2.5 V Step Centered –1.25 V Below Ground

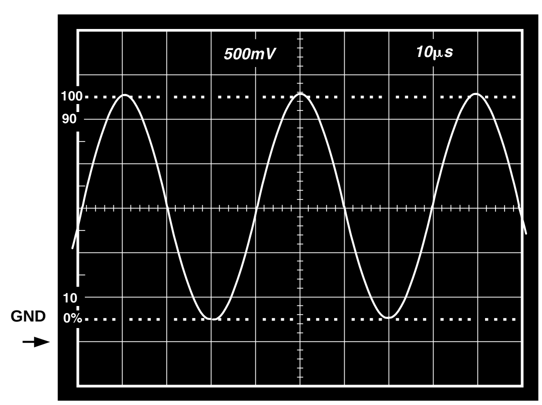


Figure 37. V_S = 3 V, 0 V; Gain of Two Inverter, V_{IN} = 1.25 V, 25 kHz, Sine Wave Centered at –0.75 V, R_L = 600 Ω

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD820, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figures 28 and 31) and increased common-mode voltage error as illustrated in Figure 19.

The AD820 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 38a shows the response of an AD820 voltage follower to a 0 V to +5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$—no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD820's plus input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 38b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in Figure 6.

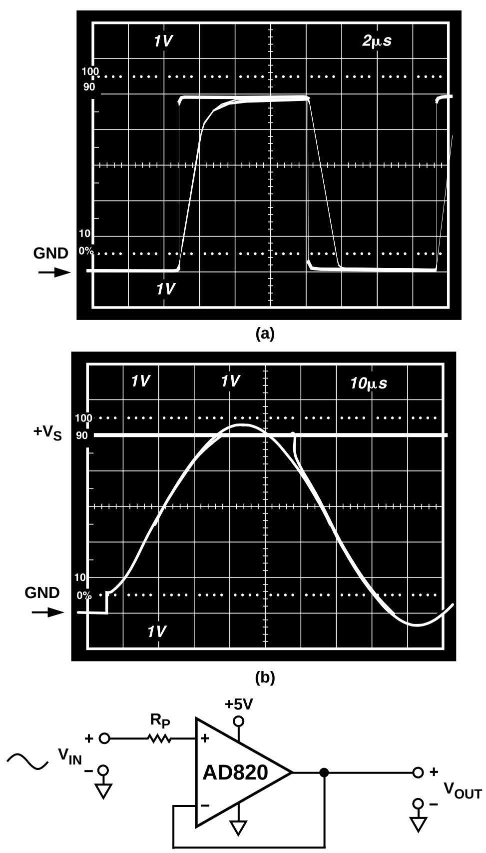


Figure 38. (a) Response with $R_P = 0$; V_{IN} from 0 to $+V_S$
(b) $V_{IN} = 0$ to $+V_S + 200$ mV
$V_{OUT} = 0$ to $+V_S$
$R_P = 49.9$ kΩ

A current limiting resistor should be used in series with the input of the AD820 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD820 when $\pm V_S = 0$. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 volts below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 volts. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD820 is designed for 13 nV/$\sqrt{\text{Hz}}$ wideband input voltage noise and maintains low noise performance to low frequencies (refer to Figure 13). This noise performance, along with the AD820's low input current and current noise means that the AD820 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 39.

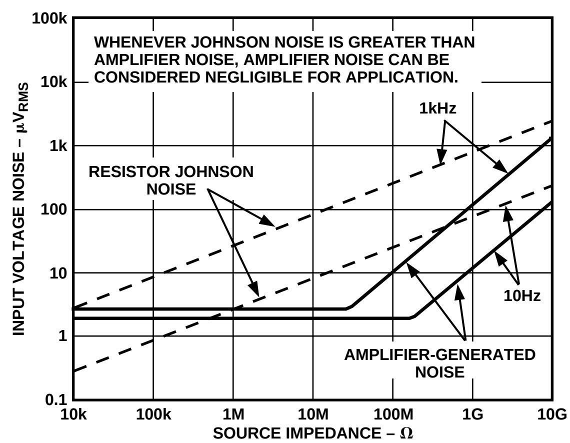


Figure 39. Total Noise vs. Source Impedance

OUTPUT CHARACTERISTICS

The AD820's unique bipolar rail-to-rail output stage swings within 5 mV of the minus supply and 10 mV of the positive supply with no external resistive load. The AD820's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV, when sinking 5 mA, the saturation voltage to the minus rail will he 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in Figures 9 through 12. For load resistances over 20 kΩ, the AD820's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD820's output is driven hard against the output saturation voltage, it will recover within 2 μs of the input returning to the amplifier's linear operating region.

Direct capacitive load will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 40 shows the AD820's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Figure 41 is a plot of capacitive load that will result in a 20 degree phase margin versus noise gain for the AD820. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

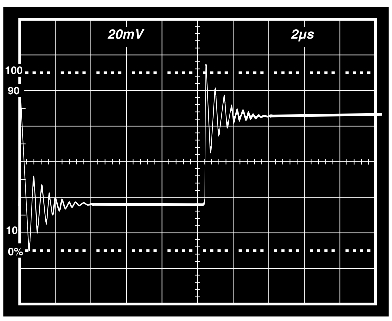


Figure 40. Small Signal Response of AD820 as Unity Gain Follower Driving 350 pF Capacitive Load

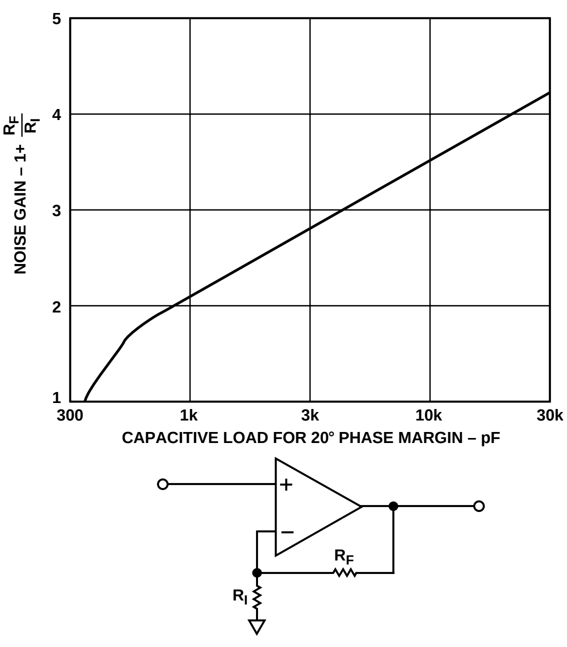


Figure 41. Capacitive Load Tolerance vs. Noise Gain

Figure 42 shows a possible configuration for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

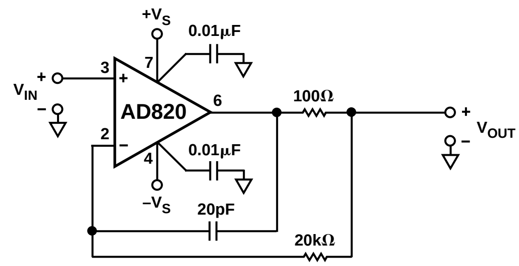


Figure 42. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

OFFSET VOLTAGE ADJUSTMENT

The AD820's offset voltage is low, so external offset voltage nulling is not usually required. Figure 43 shows the recommended technique for AD820's packaged in plastic DIPs. Adjusting offset voltage in this manner will change the offset voltage temperature drift by 4 µV/°C for every millivolt of induced offset. The null pins are not functional for AD820s in the SO-8 "R" package.

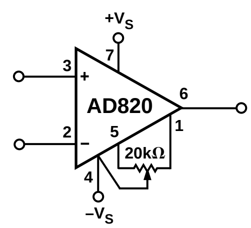


Figure 43. Offset Null

APPLICATIONS

Single Supply Half-Wave and Full-Wave Rectifiers

An AD820 configured as a unity gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD820's inputs maintain picoamp level input currents even when driven well below the minus supply. The rectifier puts that behavior to good use, maintaining an input impedance of over 10^{11} Ω for input voltages from 1 volt from the positive supply to 20 volts below the negative supply.

The full and half-wave rectifier shown in Figure 44 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity gain follower A1 and the loop of amplifier A2. This forces the inputs of A2 to be equal, thus no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The non-inverting input of amplifier A2 sees the ground level output of A1, therefore A2 operates as a unity gain inverter. The output at node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltages up to ±18 volts can be rectified, depending on the voltage supply used.

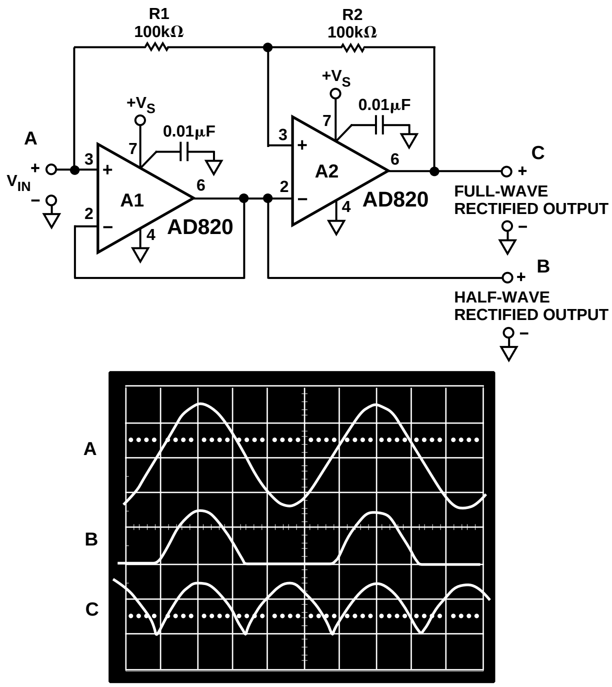


Figure 44. Single Supply Half- and Full-Wave Rectifier

4.5 Volt Low Dropout, Low Power Reference

The rail-to-rail performance of the AD820 can be used to provide low dropout performance for low power reference circuits powered with a single low voltage supply. Figure 45 shows a 4.5 volt reference using the AD820 and the AD680, a low power 2.5 volt bandgap reference. R2 and R3 set up the required gain of 1.8 to develop the 4.5 volt output. R1 and C2 form a low-pass RC filter to reduce the noise contribution of the AD680.

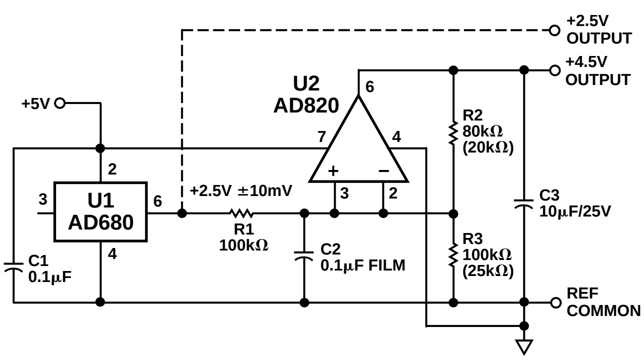


Figure 45. Single Supply 4.5 Volt Low Dropout Reference

With a 1 mA load, this reference maintains the 4.5 volt output with a supply voltage down to 4.7 volts. The amplitude of the recovery transient for a 1 mA to 10 mA step change in load current is under 20 mV, and settles out in a few microseconds. Output voltage noise is less than 10 µV rms in a 25 kHz noise bandwidth.

Low Power Three-Pole Sallen Key Low-Pass Filter

The AD820's high input impedance makes it a good selection for active filters. High value resistors can be used to construct low frequency filters with capacitors much less than 1 µF. The AD820's picoamp level input currents contribute minimal dc errors.

Figure 46 shows an example, a 10 Hz three-pole Sallen Key Filter. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the two-pole section of the filter. This eliminates any peaking of the noise contribution of resistors R1, R2, and R3, thus minimizing the inherent output voltage noise of the filter.

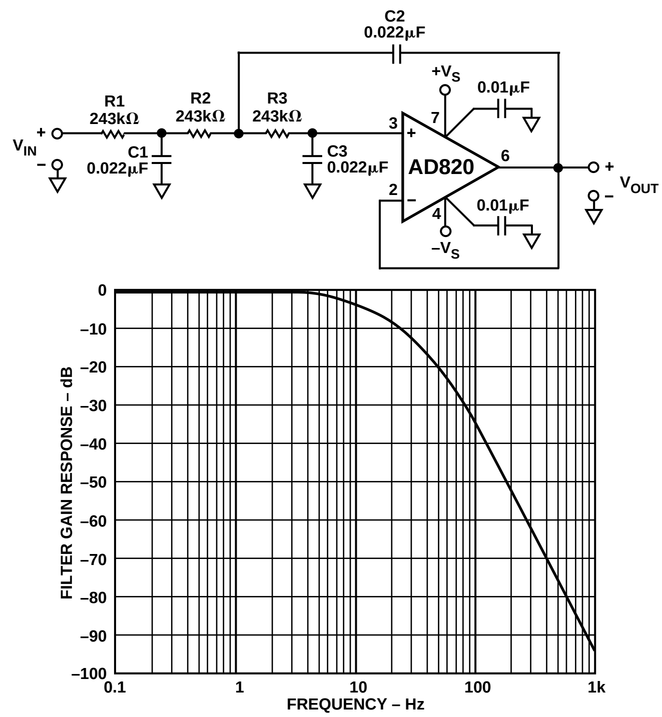
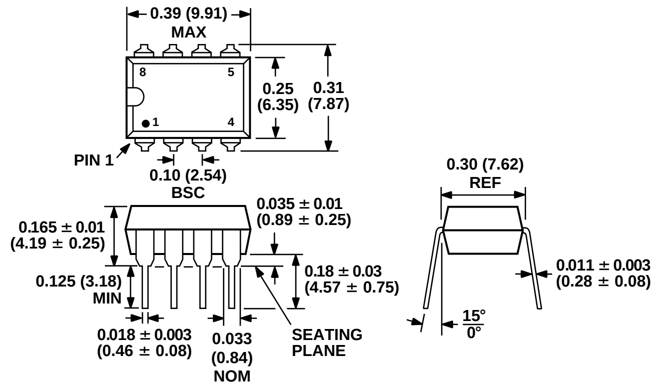


Figure 46. 10 Hz Sallen Key Low-Pass Filter

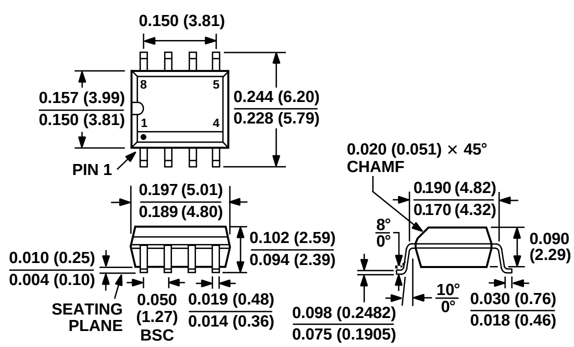
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Mini-DIP Package (N-8)



SOIC Package (R-8)



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