

# AN3310K, AN3310S

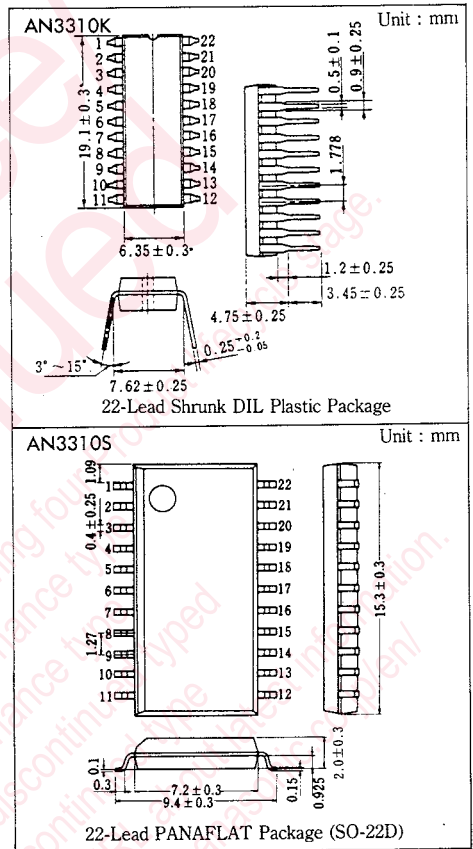
## Head Amplifier Circuits for VTR (4-Head Type)

### ■ Outline

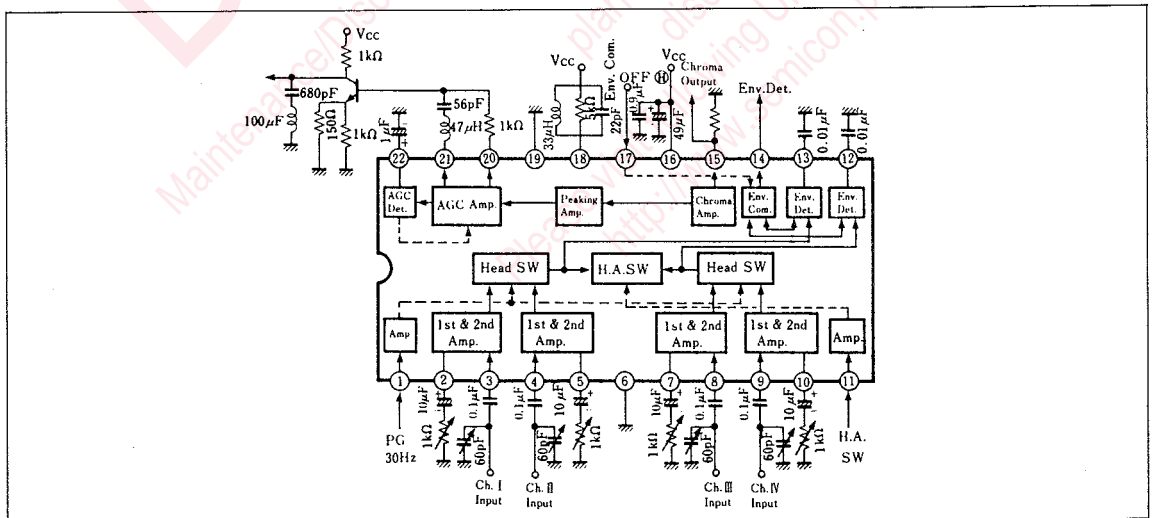
The AN3310K and the AN3310S are integrated circuits designed for head amplifier circuits for VTR (4-head type).

### ■ Features

- Built-in enveloped comparing circuit
- Built-in peaking amplifier circuit
- Less noise voltage referred to input :  $1 \mu \text{ Vrms}$
- Supply voltage :  $V_{cc}=5\text{V}$



### ■ Block Diagram



### ■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Head SW Changeover	12	Ch. I, II Side Envelope Detection
2	Initial Stage Bias(Ch. I)	13	Ch. III, IV Side Envelope Detection
3	Initial Stage Input(Ch. I)	14	Envelope Comparative Output
4	Initial Stage Input(Ch. II)	15	Chroma Output
5	Initial Stage Bias(Ch. II)	16	V <sub>CC</sub>
6	Input Stage GND	17	Envelope Comparative Circuit Stop SW
7	Initial Stage Bias(Ch. III)	18	Peaking Circuit Peak Constant
8	Initial Stage Input(Ch. III)	19	Output Stage GND
9	Initial Stage Input(Ch. IV)	20	AGC Output
10	Initial Stage Bias(Ch. IV)	21	AGC Reverse Phase Output
11	Head Amp. SW Changeover	22	AGC Control Signal Detection

### ■ Absolute Maximum Ratings (T<sub>a</sub>=25°C)

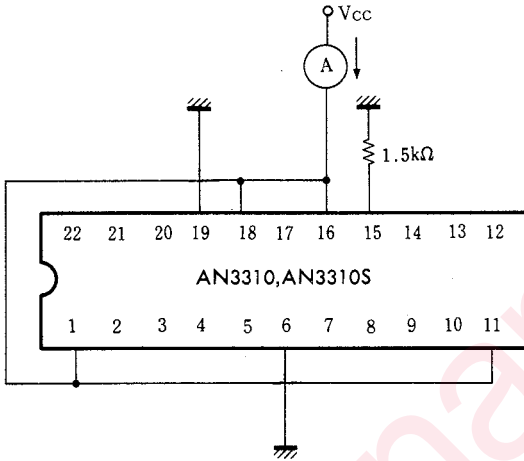
Item	Symbol	Rating	Unit
Supply Voltage	V <sub>C</sub>	6.0	V
Power Dissipation(T <sub>a</sub> =70°C)	P <sub>D</sub>	250	mW
Operating Ambient Temperature	T <sub>opr</sub>	-20~+70	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

### ■ Electrical Characteristics (T<sub>a</sub>=25°C)

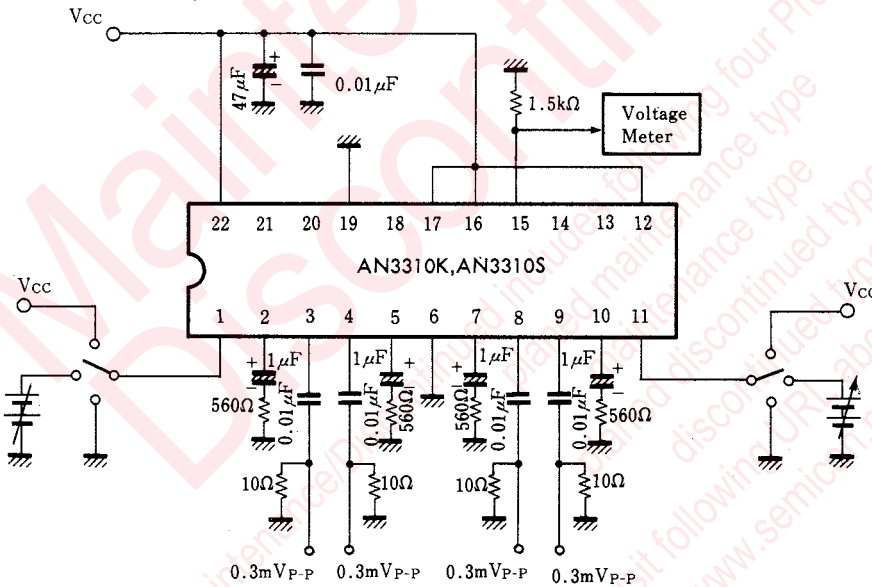
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I <sub>16</sub>	1	V <sub>CC</sub> =5V	16		40	mA
Ch. I Gain	G <sub>3-15</sub>	2	V <sub>CC</sub> =5V, f=1MHz	50.5		60.5	dB
Ch. II Gain	G <sub>4-15</sub>	2	V <sub>CC</sub> =5V, f=1MHz	50.5		60.5	dB
Ch. III Gain	G <sub>8-15</sub>	2	V <sub>CC</sub> =5V, f=1MHz	50.5		60.5	dB
Ch. IV Gain	G <sub>9-15</sub>	2	V <sub>CC</sub> =5V, f=1MHz	50.5		60.5	dB
AGC Output Amplitude	v <sub>20</sub>	3	V <sub>CC</sub> =5V, f=4MHz	100		190	mV <sub>P-P</sub>
AGC Control Sensitivity	v <sub>20</sub>	3	V <sub>CC</sub> =5V, f=4MHz			3	dB
H.SW Changeover Sensitivity	S <sub>1</sub>	2	V <sub>CC</sub> =5V			1	V
H.A.SW Changeover Sensitivity	S <sub>11</sub>	2	V <sub>CC</sub> =5V			1	V
Noise voltage Referred to Input(I)	V <sub>ni3-15</sub>	4	V <sub>CC</sub> =5V, 1MHz BPF			1	μV <sub>rms</sub>
Noise voltage Referred to Input(II)	V <sub>ni4-15</sub>	4	V <sub>CC</sub> =5V, 1MHz BPF			1	μV <sub>rms</sub>
Noise voltage Referred to Input(III)	V <sub>ni8-15</sub>	4	V <sub>CC</sub> =5V, 1MHz BPF			1	μV <sub>rms</sub>
Noise voltage Referred to Input(IV)	V <sub>ni9-15</sub>	4	V <sub>CC</sub> =5V, 1MHz BPF			1	μV <sub>rms</sub>
Envelope Comparative Output Amplitude	v <sub>14</sub>	5	V <sub>CC</sub> =5V	4.3			V <sub>P-P</sub>
Envelope Comparative Output Stop Sensitivity	S <sub>17</sub>	5	V <sub>CC</sub> =5V			1.2	V

Note : Operating Supply Voltage Range : V<sub>CC(oper)</sub>=4.5~5.5V

Test Circuit 1 (I<sub>16</sub>)



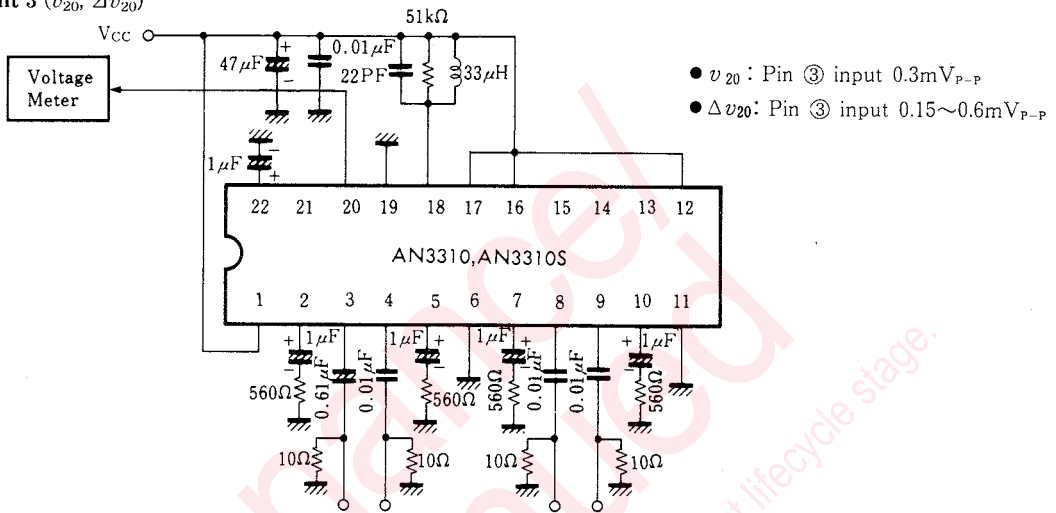
Test Circuit 2 (G<sub>3-15</sub>, G<sub>4-15</sub>, G<sub>8-15</sub>, G<sub>9-15</sub>, S<sub>1</sub>, S<sub>11</sub>)



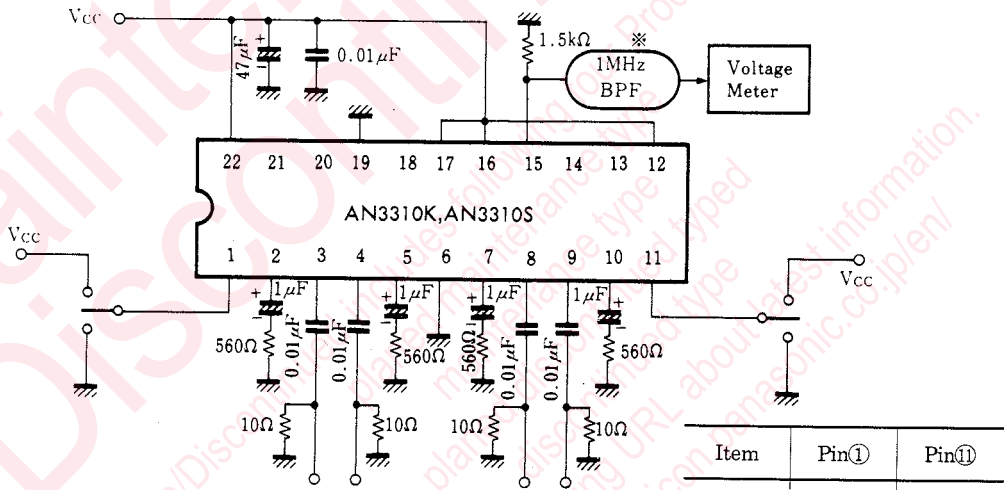
Item	①Pin	⑩Pin	Input Pin
G <sub>3-15</sub>	V <sub>CC</sub>	GND	③
G <sub>4-15</sub>	GND	GND	④
G <sub>8-15</sub>	V <sub>CC</sub>	V <sub>CC</sub>	⑧
G <sub>9-15</sub>	GND	V <sub>CC</sub>	⑨

- S<sub>1</sub>, S<sub>11</sub> : Pin ④ 0.3mV<sub>P-P</sub> input (f<sub>in</sub>=1MHz)
- S<sub>1</sub> : Decreasing the electric potential of Pin ① from V<sub>CC</sub>, measure the electric potential of Pin ① when Pin ⑮ output appears.
- S<sub>11</sub> : Decreasing the electric potential of Pin ⑩ from V<sub>CC</sub>, measure the electric potential of Pin ⑩ when Pin ⑮ output appears.

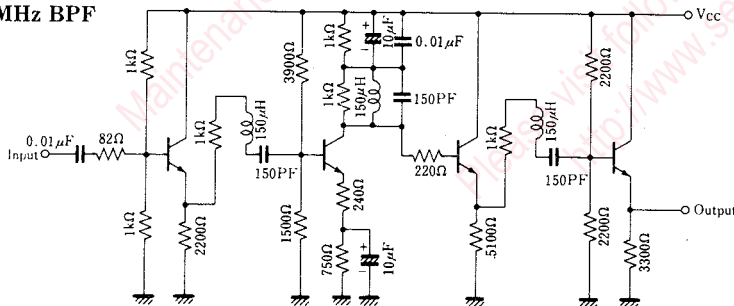
Test Circuit 3 ( $v_{20}$ ,  $\Delta v_{20}$ )



Test Circuit 4 ( $V_{ni3-15}$ ,  $V_{ni4-15}$ ,  $V_{ni8-15}$ ,  $V_{ni9-15}$ )



※1MHz BPF

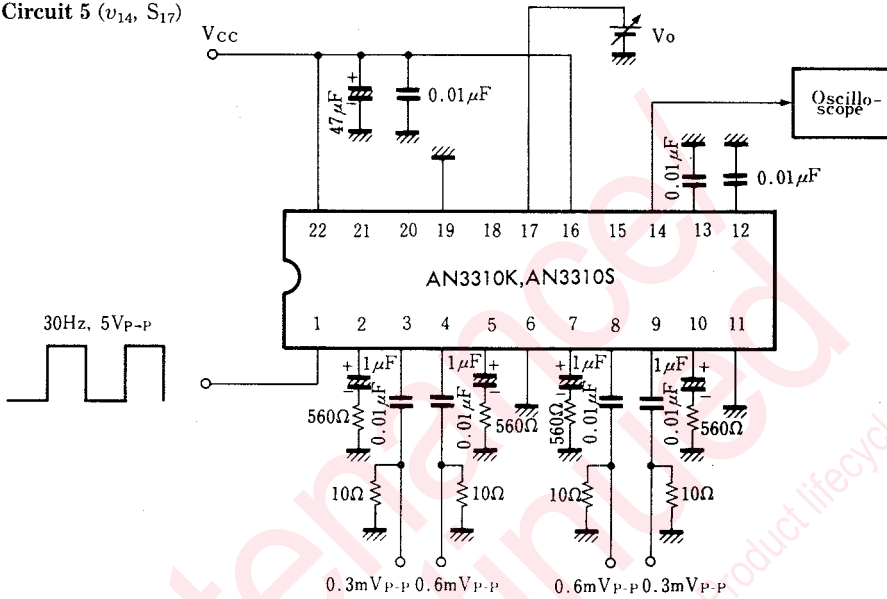


Item	Pin①	Pin②
$V_{ni3-15}$	$V_{CC}$	GND
$V_{ni4-15}$	GND	GND
$V_{ni8-15}$	$V_{CC}$	$V_{CC}$
$V_{ni9-15}$	GND	$V_{CC}$

◎ Notes for Handling

Since deterioration or destroy of characteristics may occur due to flow of overcurrent caused by the wrong insertion careful attention should be taken to handling.

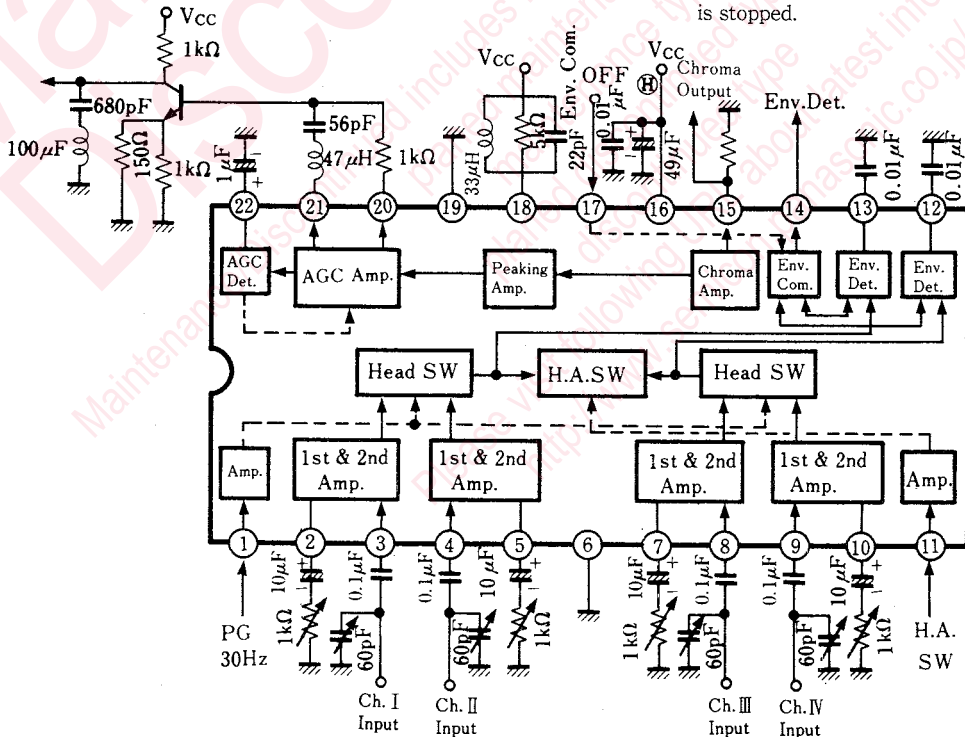
Test Circuit 5 ( $v_{14}$ ,  $S_{17}$ )



$V_{14} : V_0 = 0V$

$S_{17}$  : Increasing the electric potential of  $V_0$  from 0V, measure the electric potential of  $V_0$  when Pin ⑭ output is stopped.

■ Application Circuit



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