

# QUAD DIGITAL ISOLATORS

## FEATURES

- 1, 25, and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1 ns Max
  - Low Pulse-Width Distortion (PWD); 2 ns Max
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (see application note SLLA197 and Figure 14)
- 4000-$V_{peak}$ Isolation, 560-$V_{peak}$ Working Voltage
- UL 1577 Certified
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see application report SLLA181)
- –40°C to 125°C Operating Range

## APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

## DESCRIPTION

The ISO7240, ISO7241 and ISO7242 are quad-channel digital isolators with multiple channel configurations with output enable function. These devices have logic input and output buffers separated by TI's silicon dioxide ($SiO_2$) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7240 has all four channels in the same direction while the ISO7241 has three channels the same direction and one channel in opposition. The ISO7242 has two channels in each direction.

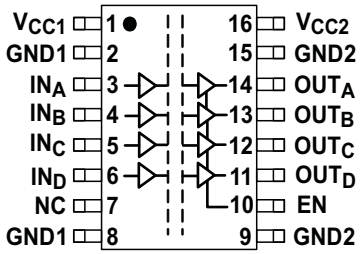
The A and C option devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The M option devices have CMOS Vcc/2 input thresholds and do not have the input noise-filter or the additional propagation delay.

A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

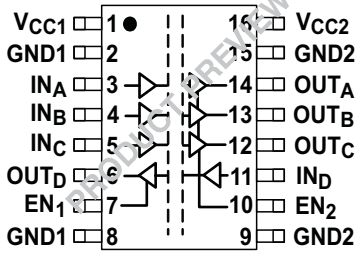
These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

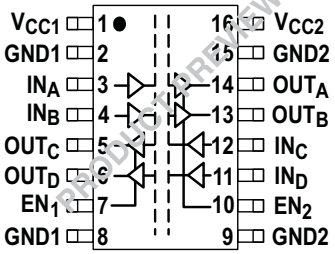
**ISO7240**




**ISO7241**




**ISO7242**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## FUNCTION DIAGRAM

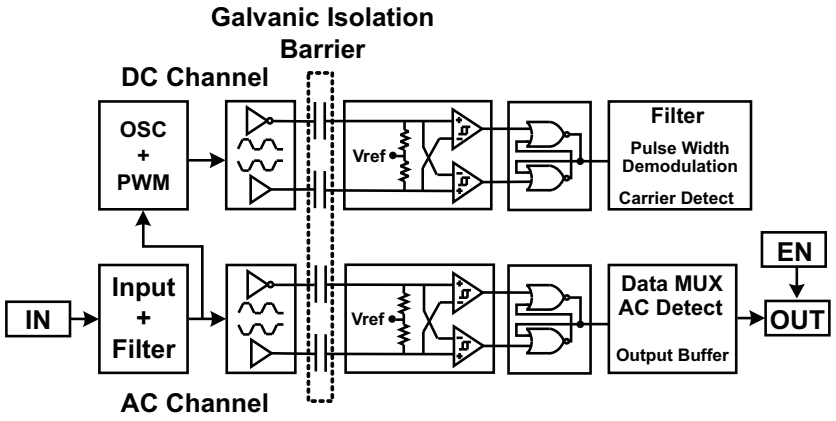



**Table 1. Device Function Table ISO724x (1)**

| $V_{CC1}$ | $V_{CC2}$ | INPUT (IN) | OUTPUT ENABLE (EN) | OUTPUT (OUT) |
|---|---|---|---|---|
| PU | PU | H | H or Open | H |
| | | L | H or Open | L |
| | | X | L | Z |
| | | Open | H or Open | H |
| PD | PU | X | H or Open | H |
| PD | PU | X | L | Z |

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

## AVAILABLE OPTIONS

| PRODUCT | SIGNALING RATE | INPUT THRESHOLD | CHANNEL CONFIGURATION | MARKED AS | ORDERING NUMBER |
|---|---|---|---|---|---|
| ISO7240ADW | 1 Mbps | ~1.5 V (TTL) (CMOS compatible) | 4/0 | ISO7240A | ISO7240ADW (rail) |
| | | | | | ISO7240ADWR (reel) |
| ISO7240CDW | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | | ISO7240C | ISO7240CDW (rail) |
| | | | | | ISO7240CDWR (reel) |
| ISO7240MDW | 150 Mbps | Vcc/2 (CMOS) | | ISO7240M | ISO7240MDW (rail) |
| | | | | | ISO7240MDWR (reel) |
| ISO7241ADW(1) | 1 Mbps | ~1.5 V (TTL) (CMOS compatible) | 3/1 | ISO7241A | ISO7241ADW (rail) |
| | | | | | ISO7241ADWR (reel) |
| ISO7241CDW(1) | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | | ISO7241C | ISO7241CDW (rail) |
| | | | | | ISO7241CDWR (reel) |
| ISO7241MDW(1) | 150 Mbps | Vcc/2 (CMOS) | | ISO7241M | ISO7241MDW (rail) |
| | | | | | ISO7241MDWR (reel) |
| ISO7242ADW(1) | 1 Mbps | ~1.5 V (TTL) (CMOS compatible) | 2/2 | ISO7242A | ISO7242ADW (rail) |
| | | | | | ISO7242ADWR (reel) |
| ISO7242CDW(1) | 25 Mbps | ~1.5 V (TTL) (CMOS compatible) | | ISO7242C | ISO7242CDW (rail) |
| | | | | | ISO7242CDWR (reel) |
| ISO7242MDW(1) | 150 Mbps | Vcc/2 (CMOS) | | ISO7242M | ISO7242MDW (rail) |
| | | | | | ISO7242MDWR (reel) |

(1) Product Preview

## ABSOLUTE MAXIMUM RATINGS(1)

| | | | | | VALUE | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(2), $V_{CC1}$, $V_{CC2}$ | | | | –0.5 to 6 | V |
| $V_I$ | Voltage at IN, OUT, EN | | | | –0.5 to 6 | V |
| $I_O$ | Output current | | | | ±15 | mA |
| ESD | Electrostatic discharge | Human Body Model | JEDEC Standard 22, Test Method A114-C.01 | All pins | ±4 | kV |
| | | Field-Induced-Charged Device Model | JEDEC Standard 22, Test Method C101 | | ±1 | |
| | | Machine Model | ANSI/ESDS5.2-1996 | | ±200 | V |
| $T_J$ | Maximum junction temperature | | | | 170 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage, $V_{CC1}$, $V_{CC2}$ | | 4.5 | | 5.5 | V |
| | | | 3 | | 3.6 | |
| $I_{OH}$ | High-level output current | | | | 4 | mA |
| $I_{OL}$ | Low-level output current | | –4 | | | mA |
| $t_{ui}$ | Input pulse width | ISO724xA | 1 | | | µs |
| | | ISO724xC | 40 | | | ns |
| | | ISO724xM | 6.67 | 5 | | |
| $1/t_{ui}$ | Signaling rate | ISO724xA | 0 | 250 | 1000 | kbps |
| | | ISO724xC | 0 | 30(1) | 25 | Mbps |
| | | ISO724xM | 0 | 200(1) | 150 | |
| $V_{IH}$ | High-level input voltage (IN) | ISO724xM | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (IN) | | 0 | | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage (IN) (EN on all devices) | ISO724xA, ISO724xC | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (IN) (EN on all devices) | | 0 | | 0.8 | V |
| $T_J$ | Junction temperature | | | | 150 | °C |
| H | External magnetic field-strength immunity per IEC 61000-4-8 & IEC 61000-4-9 certification | | | | 1000 | A/m |

(1) Typical value at room temperature and well-regulated power supply.

## ELECTRICAL CHARACTERISTICS

$V_{CC1}$ and $V_{CC2}$ at 5-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{CC1}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | 1 | 3 | mA |
| | ISO7240A | 1 Mbps | | | 1 | 3 | |
| | ISO7240C/M | 25 Mbps | | | 7 | 10.5 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | mA |
| | ISO7242A | 1 Mbps | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | TBD | |
| $I_{CC2}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | 15 | 22 | mA |
| | ISO7240A | 1 Mbps | | | 16 | 22 | |
| | ISO7240C/M | 25 Mbps | | | 17 | 25 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | mA |
| | ISO7242A | 1 Mbps | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | TBD | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at VCC, Single channel | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | $V_{CC}$ – 0.4 | | | V |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V to $V_{CC}$ | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | 1 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | 25 | 50 | | kV/µs |

## SWITCHING CHARACTERISTICS

$V_{CC1}$ and $V_{CC2}$ at 5-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xA | See Figure 1 | 40 | | 80 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xA | See Figure 1 | | | 10 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 18 | | 42 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xC | See Figure 1 | | | 2.5 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 10 | | 22 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xM | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xA/C | | | | 9 | ns |
| | | ISO724xM | | | 0 | | |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xA/C | | | | 2 | ns |
| | | ISO724xM | | | 0 | 1 | |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 12 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps NRZ data input, Same polarity input on all channels, See Figure 5 | | 1 | | ns |

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS

$V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 1 | 3 | mA |
| | ISO7240A | 1 Mbps | | | | 1 | 3 | |
| | ISO7240C/M | 25 Mbps | | | | 7 | 10.5 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7242A | 1 Mbps | | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | | TBD | |
| $I_{CC2}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 9.5 | 15 | mA |
| | ISO7240A | 1 Mbps | | | | 10 | 15 | |
| | ISO7240C/M | 25 Mbps | | | | 10.5 | 17 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7242A | 1 Mbps | | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | | TBD | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at VCC, Single channel | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | ISO7240 | $V_{CC}$ – 0.4 | | | V |
| | | | | ISO724x (5-V side) | $V_{CC}$ – 0.8 | | | |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V to $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | 1 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/µs |

## SWITCHING CHARACTERISTICS

$V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xA | See Figure 1 | 40 | | 80 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xA | See Figure 1 | | | 11 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 20 | | 46 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xC | See Figure 1 | | | 3 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 12 | | 28 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xA/C | | | | 7.5 | ns |
| | | ISO724xM | | | 0 | | |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xA/C | | | | 2.5 | ns |
| | | ISO724xM | | | 0 | 1 | |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 18 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5 | | 1 | | ns |

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS

$V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 0.5 | 1 | mA |
| | ISO7240A | 1 Mbps | | | | 1 | 2 | |
| | ISO7240C/M | 25 Mbps | | | | 3 | 5 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7242A | 1 Mbps | | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | | TBD | |
| $I_{CC2}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 15 | 22 | mA |
| | ISO7240A | 1 Mbps | | | | 16 | 22 | |
| | ISO7240C/M | 25 Mbps | | | | 17 | 25 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | | TBD | mA |
| | ISO7242A | 1 Mbps | | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | | TBD | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at VCC, Single channel | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | ISO7240 | $V_{CC}$ – 0.4 | | | V |
| | | | | ISO724x (5-V side) | $V_{CC}$ – 0.8 | | | |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V to $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | 1 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/µs |

## SWITCHING CHARACTERISTICS

$V_{CC1}$ at 3.3-V and $V_{CC2}$ at 5-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xA | See Figure 1 | 40 | | 80 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xA | See Figure 1 | | | 11 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 22 | | 51 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xC | See Figure 1 | | | 3 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 12 | | 26 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | ISO724xM | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xA/C | | | | 10 | ns |
| | | ISO724xM | | | 0 | | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xA/C | | | | 2.5 | ns |
| | | ISO724xM | | | 0 | 1 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | ns |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 12 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps NRZ data input, Same polarity input on all channels, See Figure 5 | | 1 | | ns |

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS

$V_{CC1}$ and $V_{CC2}$ at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{CC1}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_2$ at 3 V | | 0.5 | 1 | mA |
| | ISO7240A | 1 Mbps | | | 1 | 2 | |
| | ISO7240C/M | 25 Mbps | | | 3 | 5 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | |
| | ISO7242A | 1 Mbps | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | TBD | |
| $I_{CC2}$ | ISO7240A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_2$ at 3 V | | 9.5 | 15 | mA |
| | ISO7240A | 1 Mbps | | | 10 | 15 | |
| | ISO7240C/M | 25 Mbps | | | 10.5 | 17 | |
| | ISO7241A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | mA |
| | ISO7241A | 1 Mbps | | | | TBD | |
| | ISO7241C/M | 25 Mbps | | | | TBD | |
| | ISO7242A/C/M | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | TBD | |
| | ISO7242A | 1 Mbps | | | | TBD | |
| | ISO7242C/M | 25 Mbps | | | | TBD | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at $V_{CC}$, single channel | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | $V_{CC}$ – 0.4 | | | V |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V or $V_{CC}$ | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | 1 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | 25 | 50 | | kV/µs |

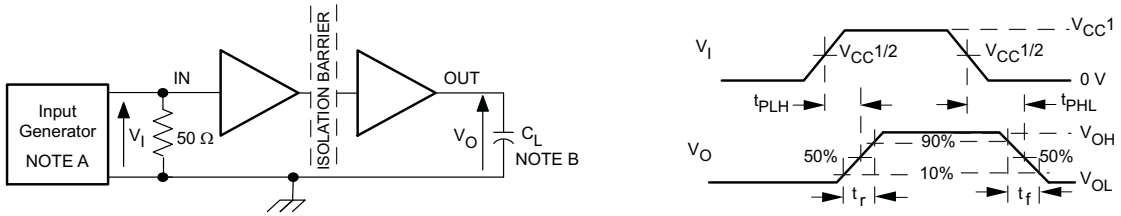
## SWITCHING CHARACTERISTICS

$V_{CC1}$ and $V_{CC2}$ at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xA | See Figure 1 | 45 | | 85 | ns |
| PWD | Pulse-width distortion $\|t_{PHL} - t_{PLH}\|$ (1) | ISO724xA | See Figure 1 | | | 12 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xC | See Figure 1 | 25 | | 56 | ns |
| PWD | Pulse-width distortion $\|t_{PHL} - t_{PLH}\|$ (1) | ISO724xC | See Figure 1 | | | 4 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | ISO724xM | See Figure 1 | 12 | | 32 | ns |
| PWD | Pulse-width distortion $\|t_{PHL} - t_{PLH}\|$ (1) | ISO724xM | See Figure 1 | | 1 | 2 | ns |
| $t_{sk(pp)}$ | Part-to-part skew (2) | ISO724xA/C | | | | 9 | ns |
| | | ISO724xM | | | 0 | | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew (3) | ISO724xA/C | | | | 3 | ns |
| | | ISO724xM | | | 0 | 1 | ns |
| $t_r$ | Output signal rise time | | See Figure 1 | | 2 | | |
| $t_f$ | Output signal fall time | | See Figure 1 | | 2 | | |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | See Figure 2 | | 15 | 20 | ns |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | See Figure 2 | | 15 | 20 | ns |
| $t_{fs}$ | Failsafe output delay time from input power loss | | See Figure 3 | | 18 | | µs |
| $t_{jit(pp)}$ | Peak-to-peak eye-pattern jitter | ISO724xM | 150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 5 | | 1 | | ns |

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

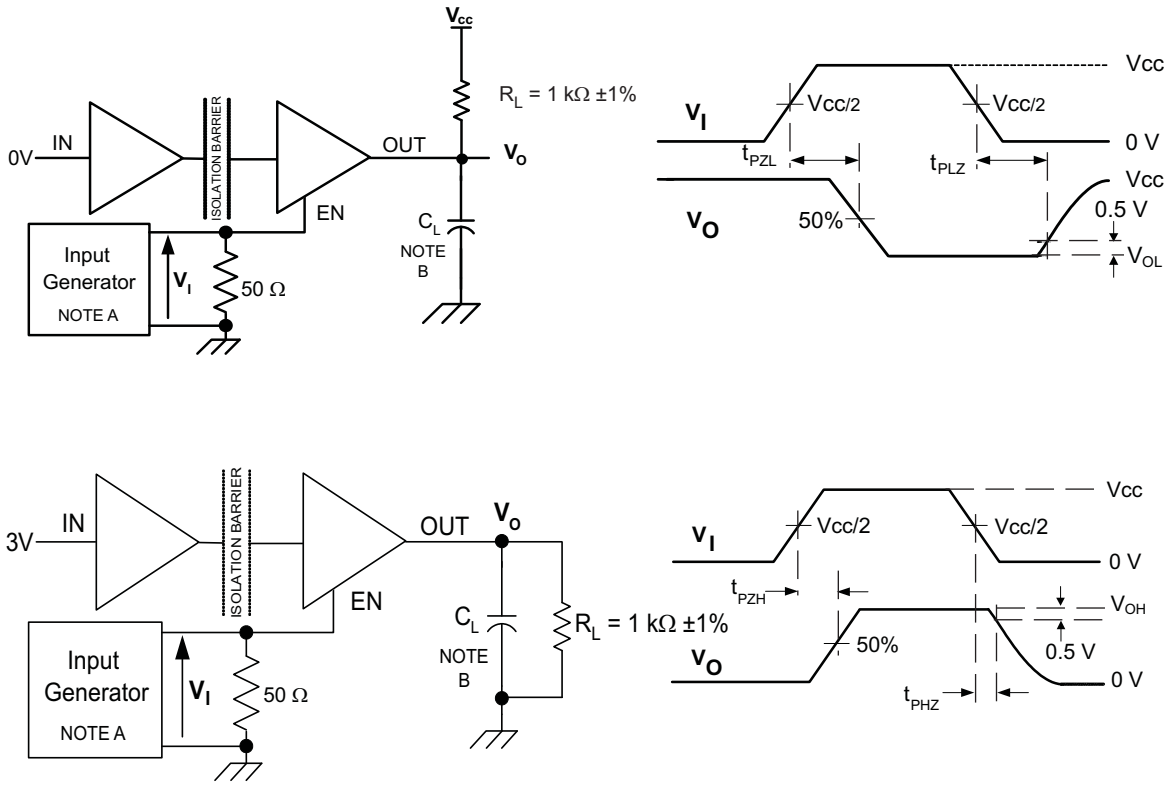
## PARAMETER MEASUREMENT INFORMATION




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms**

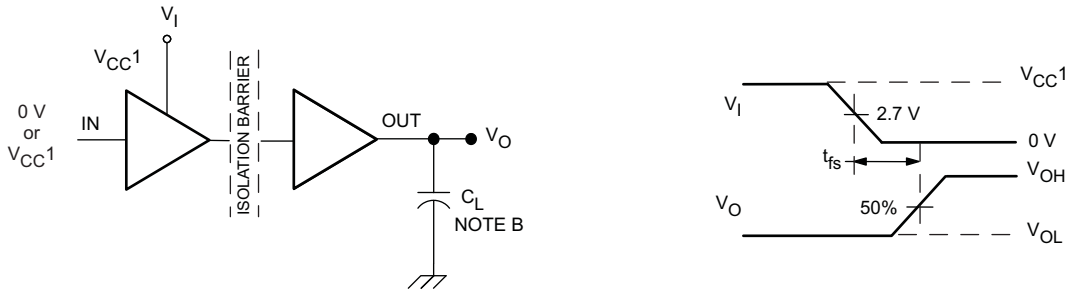



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform**

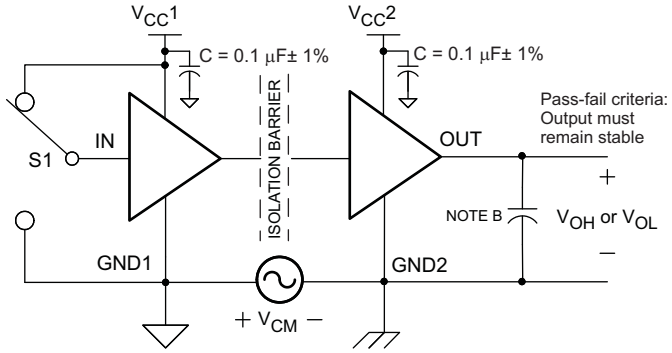
## PARAMETER MEASUREMENT INFORMATION (continued)




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

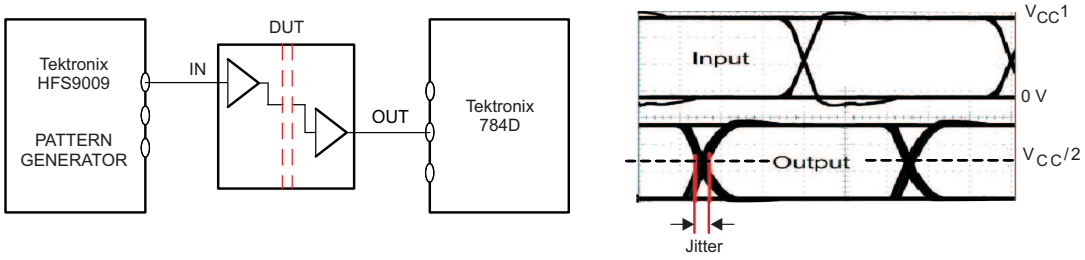
**Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

**Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform**




NOTE: PRBS bit pattern run length is $2^{16}$ – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

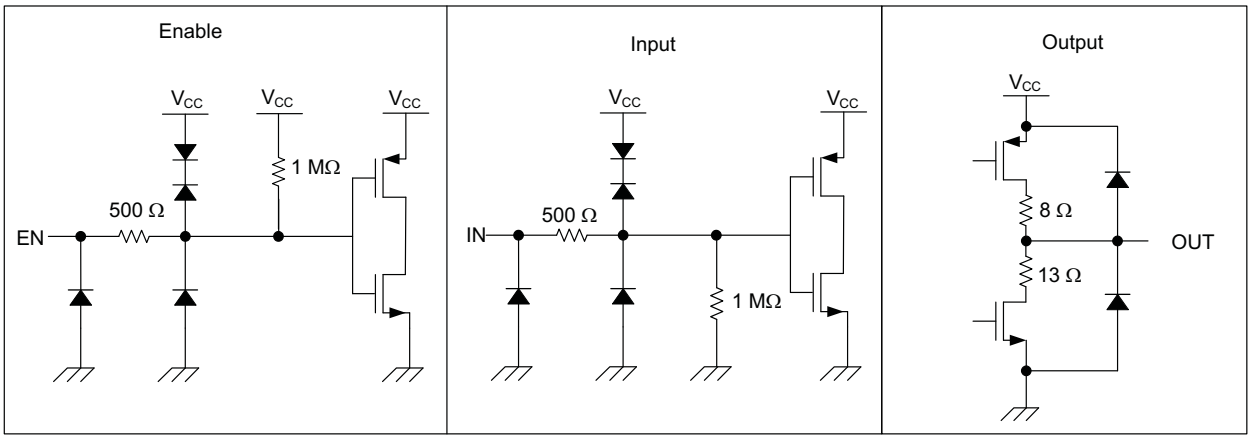
**Figure 5. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform**

# DEVICE INFORMATION

## PACKAGE CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| L(I01) | Minimum air gap (Clearance) | Shortest terminal-to-terminal distance through air | 7.7 | | | mm |
| L(I02) | Minimum external tracking (Creepage) | Shortest terminal-to-terminal distance across the package surface | 8.1 | | | mm |
| | Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.008 | | | mm |
| $R_{IO}$ | Isolation resistance | Input to output, $V_{IO}$ = 500 V, all pins on each side of the barrier tied together creating a two-terminal device | | $>10^{12}$ | | Ω |
| $C_{IO}$ | Barrier capacitance Input to output | $V_I$ = 0.4 sin (4E6πt) | | 1 | | pF |
| $C_I$ | Input capacitance to ground | $V_I$ = 0.4 sin (4E6πt) | | 1 | | pF |

## DEVICE I/O SCHEMATICS



## REGULATORY INFORMATION

| UL |
|---|
| Recognized under 1577 Component Recognition Program(1) |
| File Number: E181974 |

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

## THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-air | Low-K Thermal Resistance(1) | | 168 | | °C/W |
| | | High-K Thermal Resistance | | 96.1 | | |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | | | 61 | | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | | | 48 | | °C/W |
| $P_D$ | Device Power Dissipation | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 50% duty cycle square wave | | | 220 | mW |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

## TYPICAL CHARACTERISTIC CURVES

**3.3-V RMS SUPPLY CURRENT vs SIGNALING RATE**

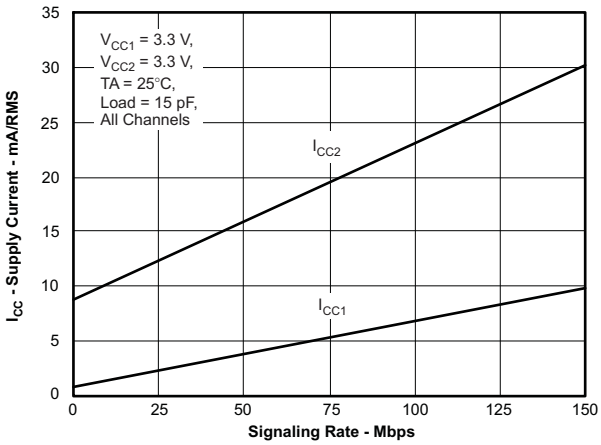



**Figure 6.**

**5-V RMS SUPPLY CURRENT vs SIGNALING RATE**

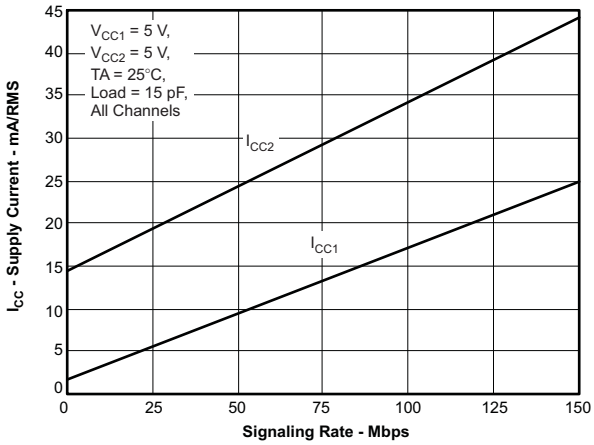



**Figure 7.**

## TYPICAL CHARACTERISTIC CURVES (continued)

**PROPAGATION DELAY VS FREE-AIR TEMPERATURE**

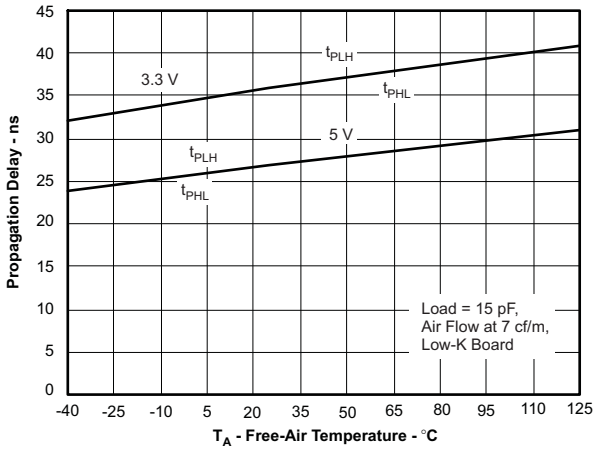



**Figure 8.**

**INPUT VOLTAGE THRESHOLD VS FREE-AIR TEMPERATURE**

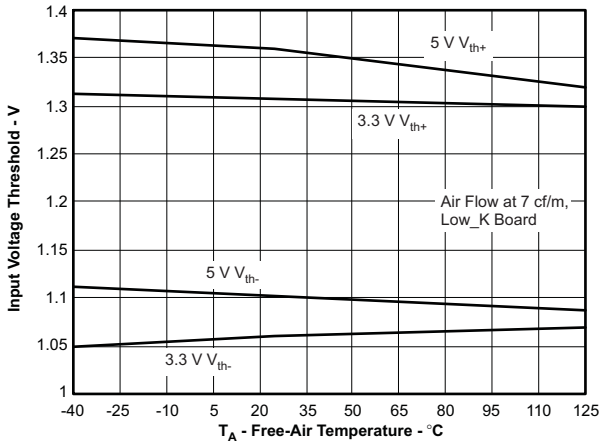



**Figure 9.**

**$V_{CC1}$ FAILSAFE THRESHOLD VS FREE-AIR TEMPERATURE**

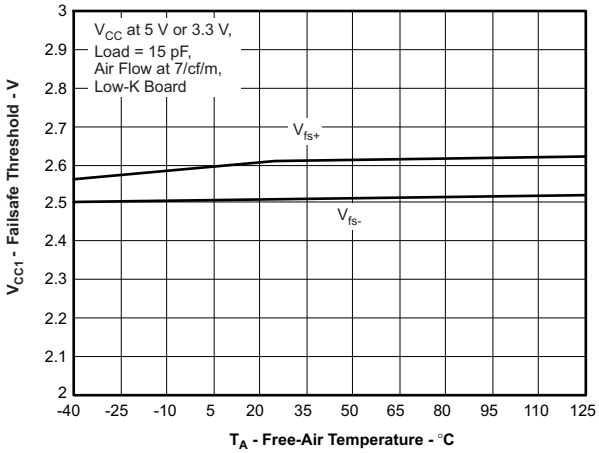



**Figure 10.**

**HIGH-LEVEL OUTPUT CURRENT VS HIGH-LEVEL OUTPUT VOLTAGE**

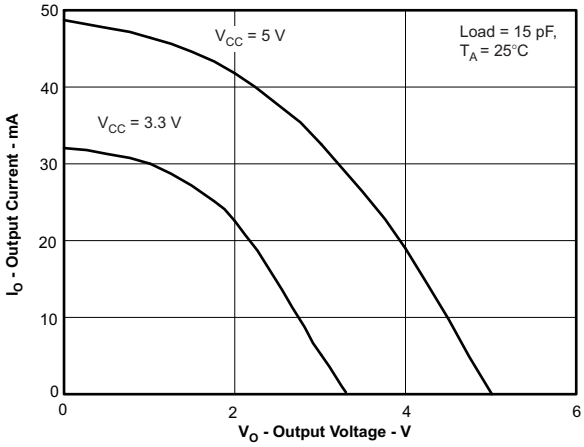



**Figure 11.**

## TYPICAL CHARACTERISTIC CURVES (continued)

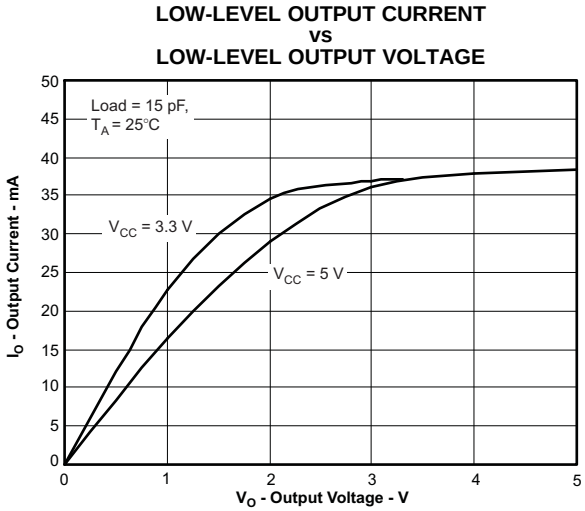



**Figure 12.**

## APPLICATION INFORMATION

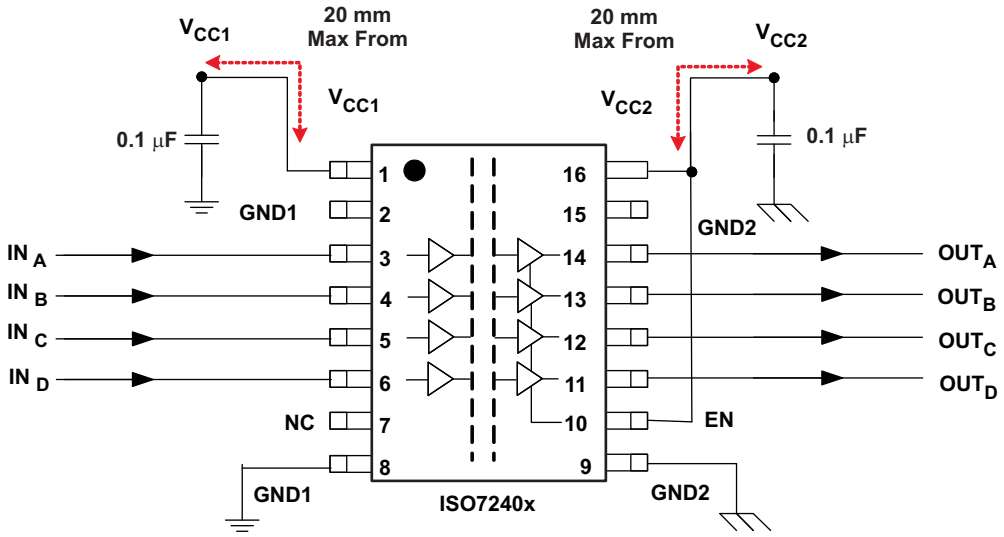



**Figure 13. Typical ISO724x Application Circuit**

## LIFE EXPECTANCY vs. WORKING VOLTAGE

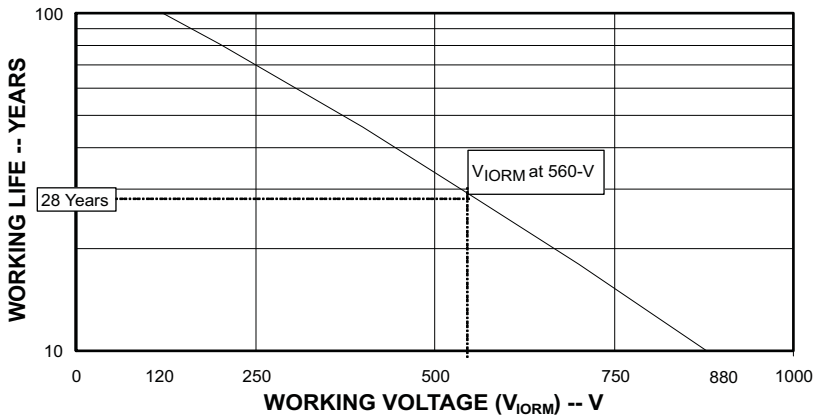
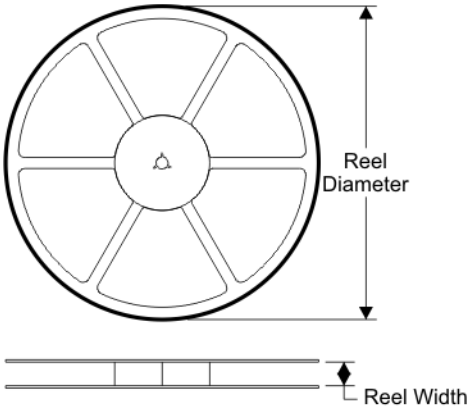


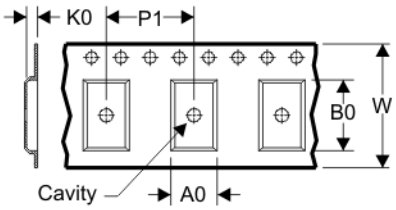

**Figure 14. Time-Dependant Dielectric Breakdown Testing Results**

## TAPE AND REEL BOX INFORMATION

**REEL DIMENSIONS**

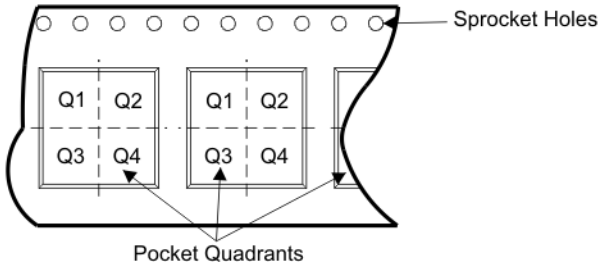



**TAPE DIMENSIONS**



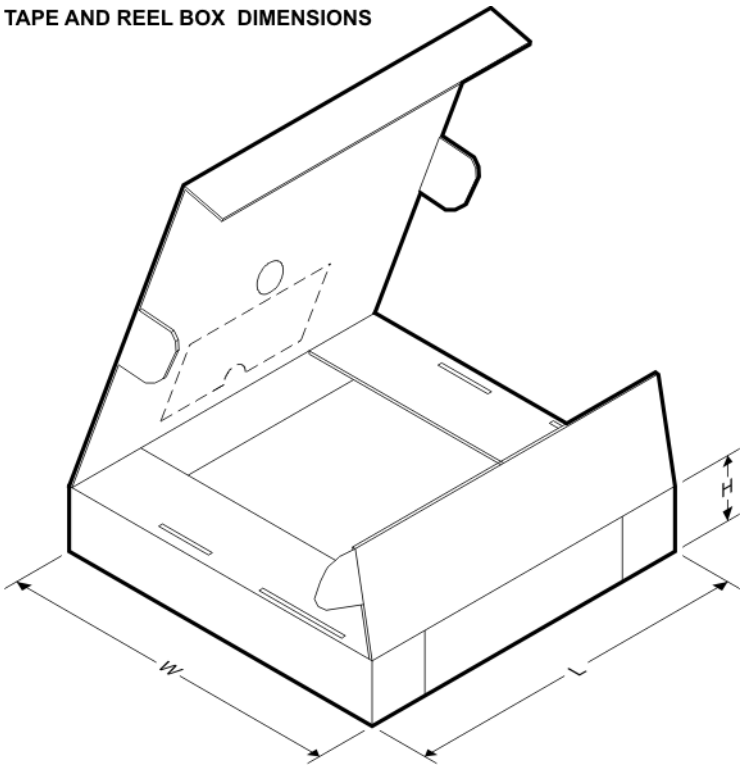

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



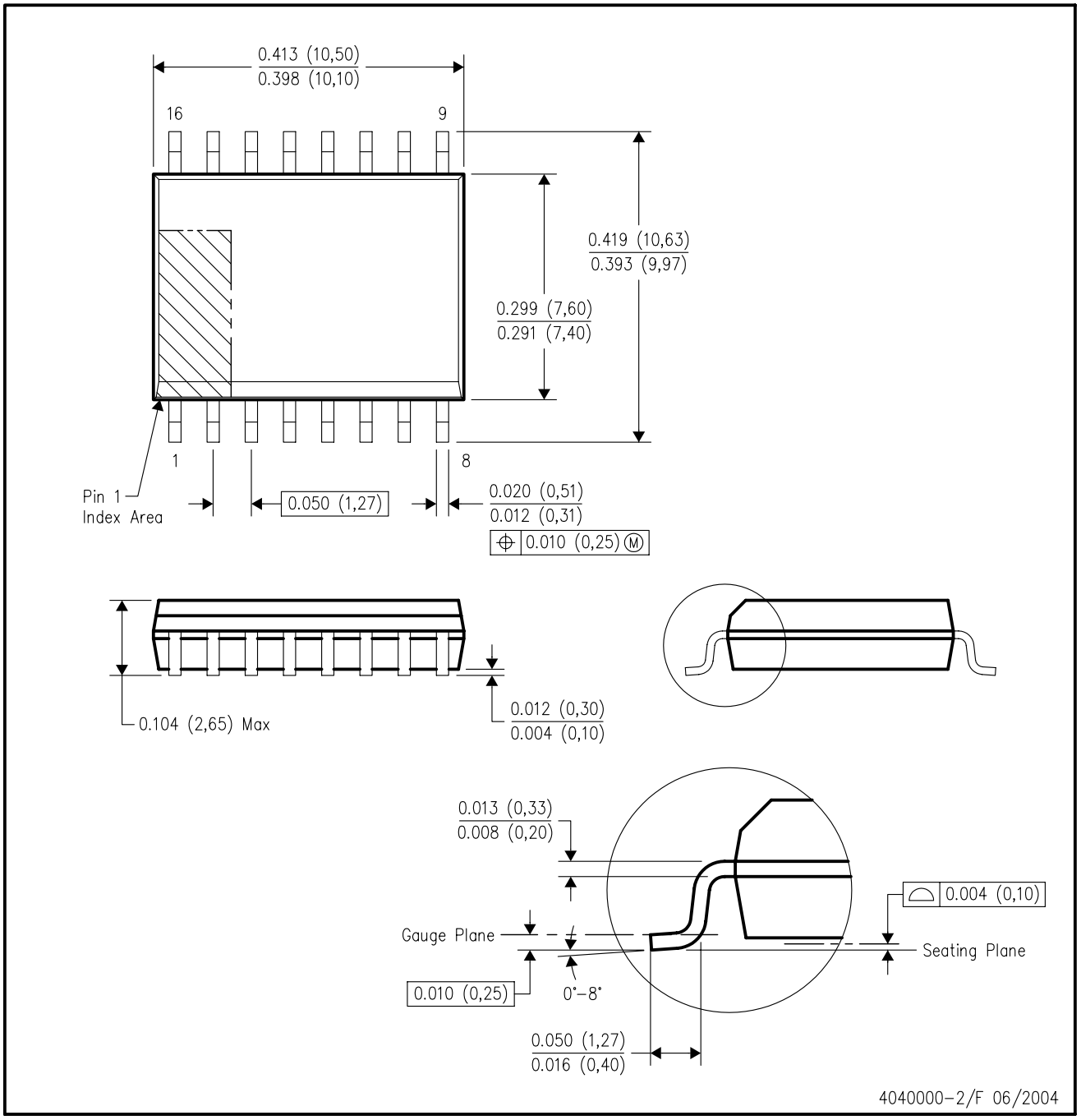

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7240ADWR | DW | 16 | SITE 35 | 330 | 16 | 10.9 | 10.78 | 3.0 | 12 | 16 | Q1 |
| ISO7240CDWR | DW | 16 | SITE 35 | 330 | 16 | 10.9 | 10.78 | 3.0 | 12 | 16 | Q1 |
| ISO7240MDWR | DW | 16 | SITE 35 | 330 | 16 | 10.9 | 10.78 | 3.0 | 12 | 16 | Q1 |

TAPE AND REEL BOX DIMENSIONS




| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| ISO7240ADWR | DW | 16 | SITE 35 | 406.0 | 348.0 | 63.0 |
| ISO7240CDWR | DW | 16 | SITE 35 | 406.0 | 348.0 | 63.0 |
| ISO7240MDWR | DW | 16 | SITE 35 | 406.0 | 348.0 | 63.0 |

## DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

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