

IR2101(S)/IR2102(S) & (PbF)

HIGH AND LOW SIDE DRIVER Product Summary

| | |
|----------------------------|-----------------|
| V_{OFFSET} | 600V max. |
| $I_{\text{O}+/-}$ | 130 mA / 270 mA |
| V_{OUT} | 10 - 20V |
| $t_{\text{on/off}}$ (typ.) | 160 & 150 ns |
| Delay Matching | 50 ns |

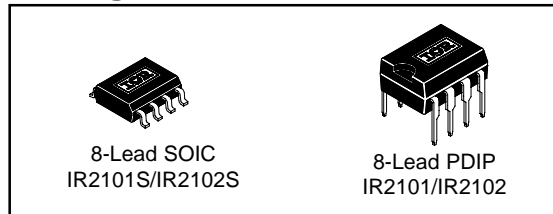
Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)
- Also available LEAD-FREE

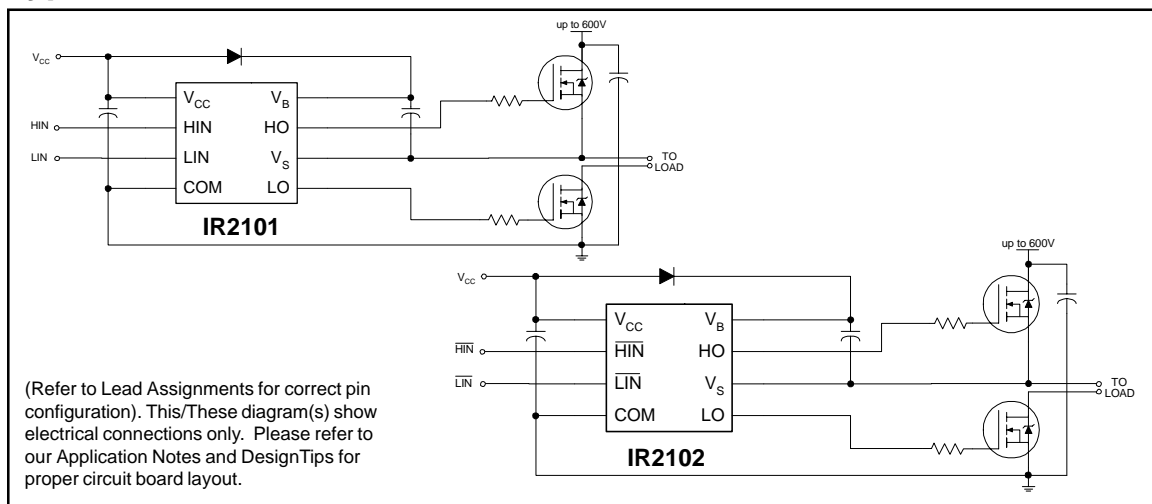
Description

The IR2101(S)/IR2102(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages



Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units | |
|---------------------|--|----------------------|-----------------------|-------|------|
| V _B | High side floating supply voltage | -0.3 | 625 | V | |
| V _S | High side floating supply offset voltage | V _B - 25 | V _B + 0.3 | | |
| V _{HO} | High side floating output voltage | V _S - 0.3 | V _B + 0.3 | | |
| V _{CC} | Low side and logic fixed supply voltage | -0.3 | 25 | | |
| V _{LO} | Low side output voltage | -0.3 | V _{CC} + 0.3 | | |
| V _{IN} | Logic input voltage (HIN & LIN) | -0.3 | V _{CC} + 0.3 | | |
| dV _S /dt | Allowable offset supply voltage transient | — | 50 | V/ns | |
| P _D | Package power dissipation @ T _A ≤ +25°C | (8 lead PDIP) | — | 1.0 | W |
| | | (8 lead SOIC) | — | 0.625 | |
| R _{thJA} | Thermal resistance, junction to ambient | (8 lead PDIP) | — | 125 | °C/W |
| | | (8 lead SOIC) | — | 200 | |
| T _J | Junction temperature | — | 150 | °C | |
| T _S | Storage temperature | -55 | 150 | | |
| T _L | Lead temperature (soldering, 10 seconds) | — | 300 | | |

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

| Symbol | Definition | Min. | Max. | Units |
|-----------------|---|---------------------|---------------------|-------|
| V _B | High side floating supply absolute voltage | V _S + 10 | V _S + 20 | V |
| V _S | High side floating supply offset voltage | Note 1 | 600 | |
| V _{HO} | High side floating output voltage | V _S | V _B | |
| V _{CC} | Low side and logic fixed supply voltage | 10 | 20 | |
| V _{LO} | Low side output voltage | 0 | V _{CC} | |
| V _{IN} | Logic input voltage (HIN & LIN) (IR2101) & ($\overline{\text{HIN}}$ & $\overline{\text{LIN}}$) (IR2102) | 0 | V _{CC} | |
| T _A | Ambient temperature | -40 | 125 | °C |

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $C_L = 1000 \text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|-------------------------------------|------|------|------|-------|-----------------|
| t_{on} | Turn-on propagation delay | — | 160 | 220 | ns | $V_S = 0V$ |
| t_{off} | Turn-off propagation delay | — | 150 | 220 | | $V_S = 600V$ |
| t_r | Turn-on rise time | — | 100 | 170 | | |
| t_f | Turn-off fall time | — | 50 | 90 | | |
| MT | Delay matching, HS & LS turn-on/off | — | — | 50 | | |

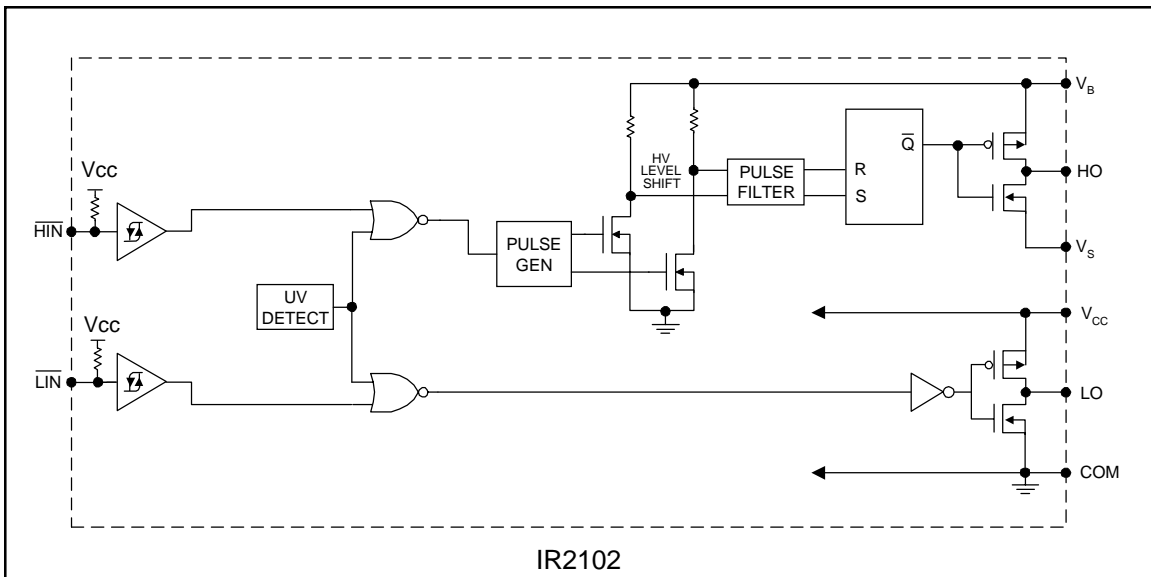
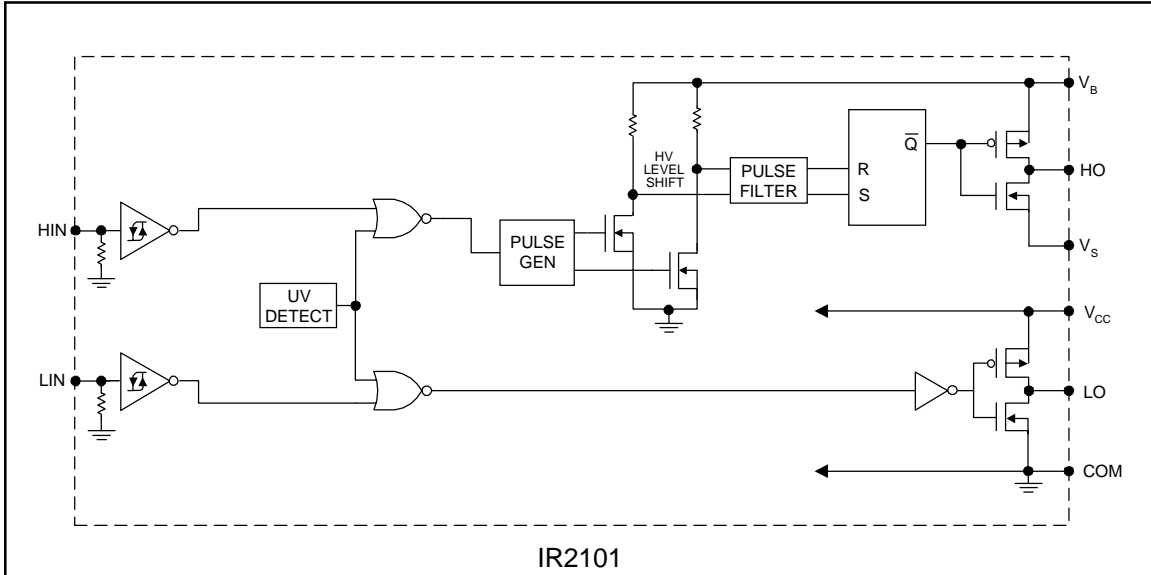
Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IH} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-------------|--|------|------|------|---------|--|
| V_{IH} | Logic "1" input voltage (IR2101) Logic "0" input voltage (IR2102) | 3 | — | — | V | $V_{CC} = 10V \text{ to } 20V$ |
| V_{IL} | Logic "0" input voltage (IR2101) Logic "1" input voltage (IR2102) | — | — | 0.8 | | $V_{CC} = 10V \text{ to } 20V$ |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | — | — | 100 | mV | $I_O = 0A$ |
| V_{OL} | Low level output voltage, V_O | — | — | 100 | | $I_O = 0A$ |
| I_{LK} | Offset supply leakage current | — | — | 50 | μA | $V_B = V_S = 600V$ |
| I_{QBS} | Quiescent V_{BS} supply current | — | 30 | 55 | | $V_{IN} = 0V \text{ or } 5V$ |
| I_{QCC} | Quiescent V_{CC} supply current | — | 150 | 270 | | $V_{IN} = 0V \text{ or } 5V$ |
| I_{IN+} | Logic "1" input bias current | — | 3 | 10 | | $V_{IN} = 5V$ (IR2101) $V_{IN} = 0V$ (IR2102) |
| I_{IN-} | Logic "0" input bias current | — | — | 1 | | $V_{IN} = 0V$ (IR2101) $V_{IN} = 5V$ (IR2102) |
| V_{CCUV+} | V_{CC} supply undervoltage positive going threshold | 8 | 8.9 | 9.8 | V | |
| V_{CCUV-} | V_{CC} supply undervoltage negative going threshold | 7.4 | 8.2 | 9 | | |
| I_{O+} | Output high short circuit pulsed current | 130 | 210 | — | mA | $V_O = 0V$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10 \mu s$ |
| I_{O-} | Output low short circuit pulsed current | 270 | 360 | — | | $V_O = 15V$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10 \mu s$ |

IR2101(S)/IR2102(S) & (PbF)

Functional Block Diagram



Lead Definitions

| Symbol | Description |
|-------------------------|--|
| HIN | Logic input for high side gate driver output (HO), in phase (IR2101) |
| $\overline{\text{HIN}}$ | Logic input for high side gate driver output (HO), out of phase (IR2102) |
| LIN | Logic input for low side gate driver output (LO), in phase (IR2101) |
| $\overline{\text{LIN}}$ | Logic input for low side gate driver output (LO), out of phase (IR2102) |
| V_B | High side floating supply |
| HO | High side gate drive output |
| V_S | High side floating supply return |
| V_{CC} | Low side and logic fixed supply |
| LO | Low side gate drive output |
| COM | Low side return |

Lead Assignments



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Figure 1. Input/Output Timing Diagram



Figure 2. Switching Time Waveform Definitions



Figure 3. Delay Matching Waveform Definitions

IR2101(S)/IR2102(S) & (PbF)



Figure 6A. Turn-On Time vs Temperature



Figure 6B. Turn-On Time vs Supply Voltage



Figure 6C. Turn-On Time vs Input Voltage

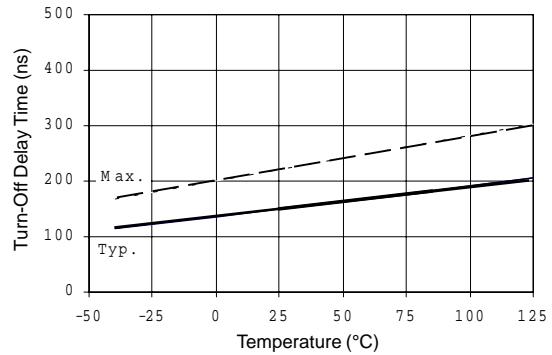


Figure 7A. Turn-Off Time vs Temperature



Figure 7B. Turn-Off Time vs Supply Voltage



Figure 7C. Turn-Off Time vs Input Voltage

IR2101(S)/IR2102(S) & (PbF)



Figure 9A. Turn-On Rise Time vs Temperature



Figure 9B. Turn-On Rise Time vs Voltage

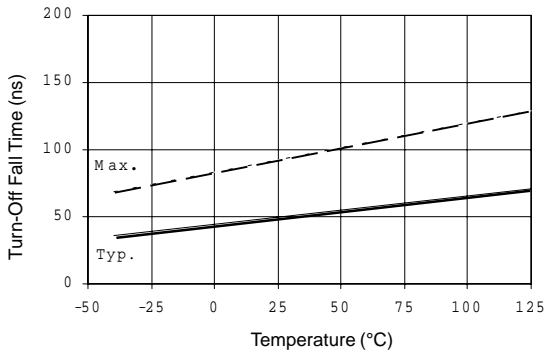


Figure 10A. Turn-Off Fall Time vs Temperature

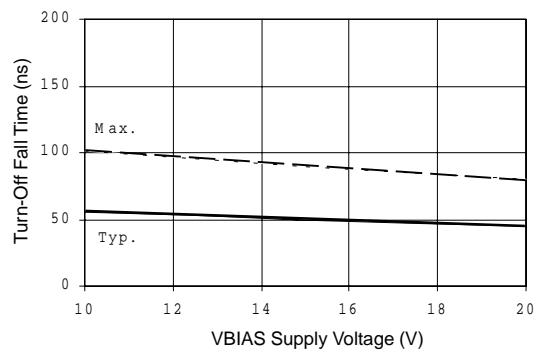
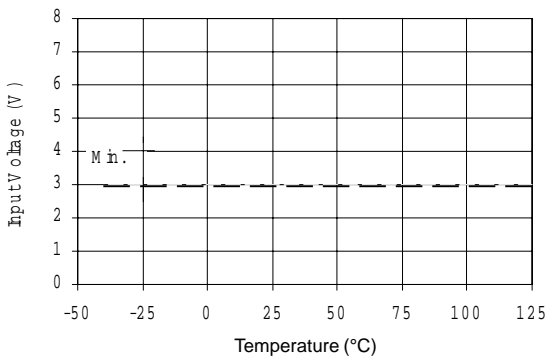
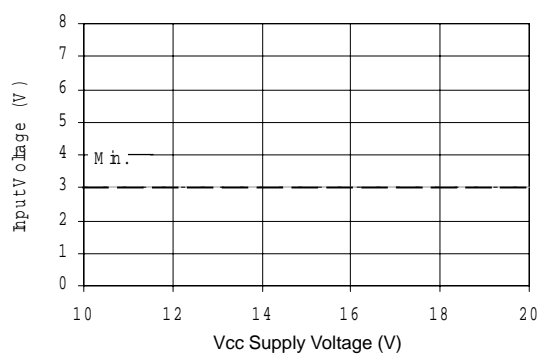


Figure 10B. Turn-Off Fall Time vs Voltage



**Figure 12A. Logic "1" Input Voltage (IR2101)
Logic "0" Input Voltage (IR2102)
vs Temperature**

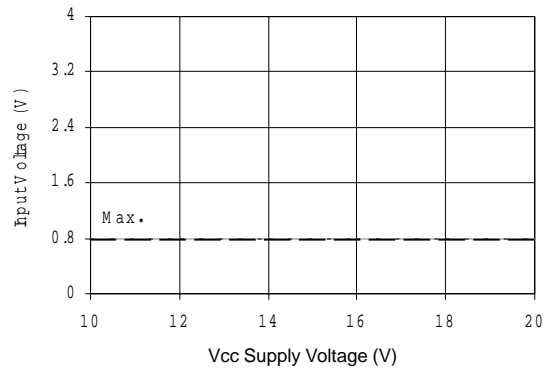


**Figure 12B. Logic "1" Input Voltage (IR2101)
Logic "0" Input Voltage (IR2102)
vs Voltage**

IR2101(S)/IR2102(S) & (PbF)



**Figure 13A. Logic "0" Input Voltage (IR2101)
 Logic "1" Input Voltage (IR2102)
 vs Temperature**



**Figure 13B. Logic "0" Input Voltage (IR2101)
 Logic "1" Input Voltage (IR2102)
 vs Voltage**



**Figure 14A. High Level Output
 vs Temperature**

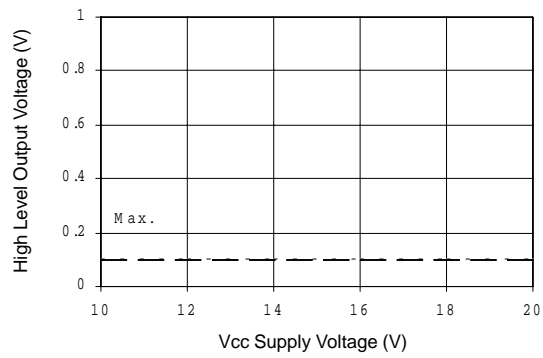


Figure 14B. High Level Output vs Voltage



**Figure 15A. Low Level Output
 vs Temperature**

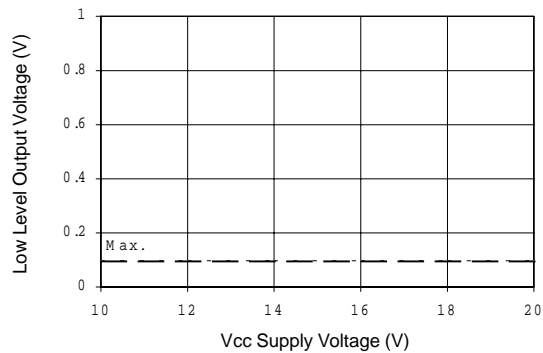


Figure 15B. Low level Output vs Voltage

IR2101(S)/IR2102(S) & (PbF)



Figure 16A. Offset Supply Current vs Temperature



Figure 16B. Offset Supply Current vs Voltage



Figure 17A. VBS Supply Current vs Temperature



Figure 17B. VBS Supply Current vs Voltage



Figure 18A. VCC Supply Current vs Temperature



Figure 18B. VCC Supply Current vs Voltage

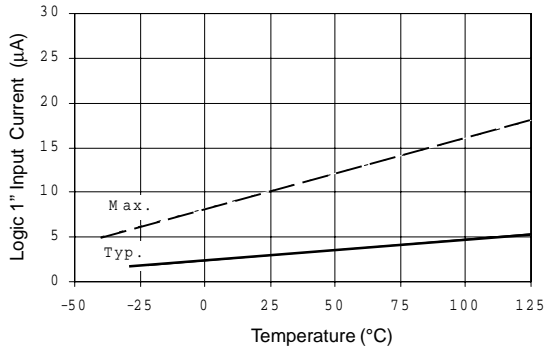


Figure 19A. Logic "1" Input Current vs Temperature



Figure 19B. Logic "1" Input Current vs Voltage



Figure 20A. Logic "0" Input Current vs Temperature

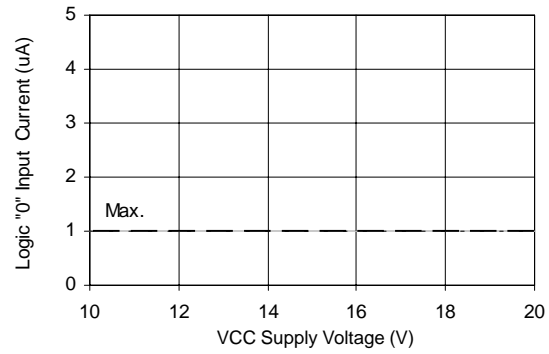


Figure 20B. Logic "0" Input Current vs Voltage

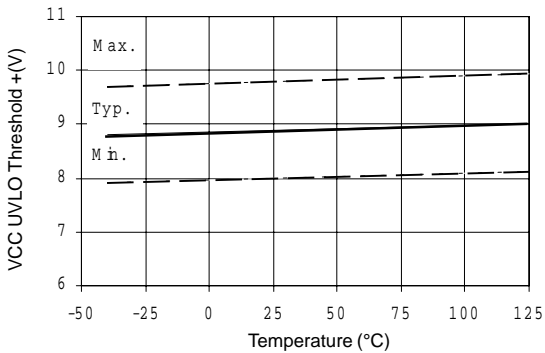


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

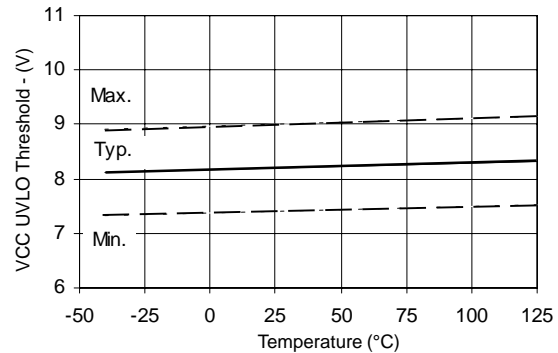


Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature

IR2101(S)/IR2102(S) & (PbF)



Figure 22A. Output Source Current vs Temperature

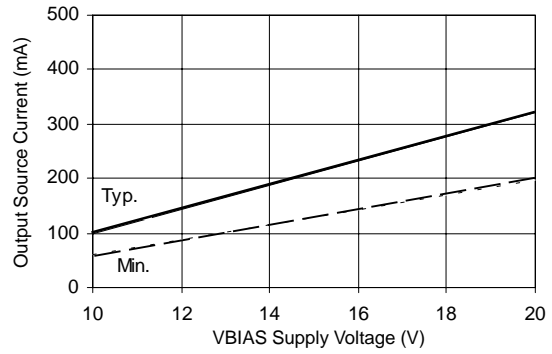


Figure 22B. Output Source Current vs Voltage

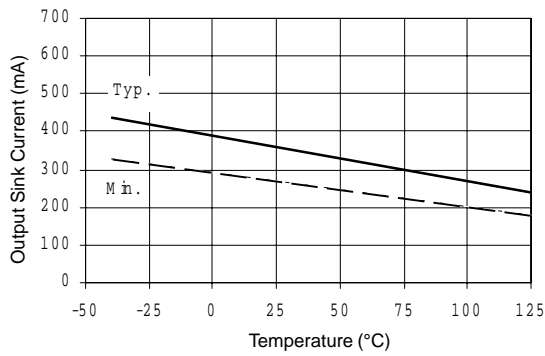


Figure 23A. Output Sink Current vs Temperature

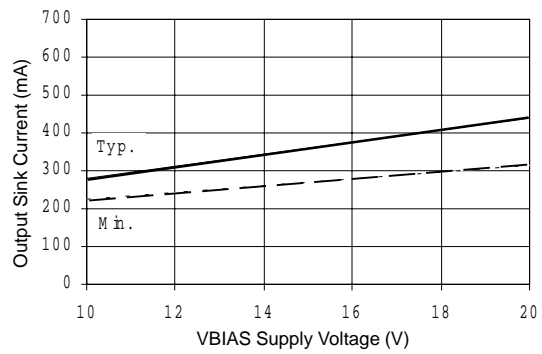


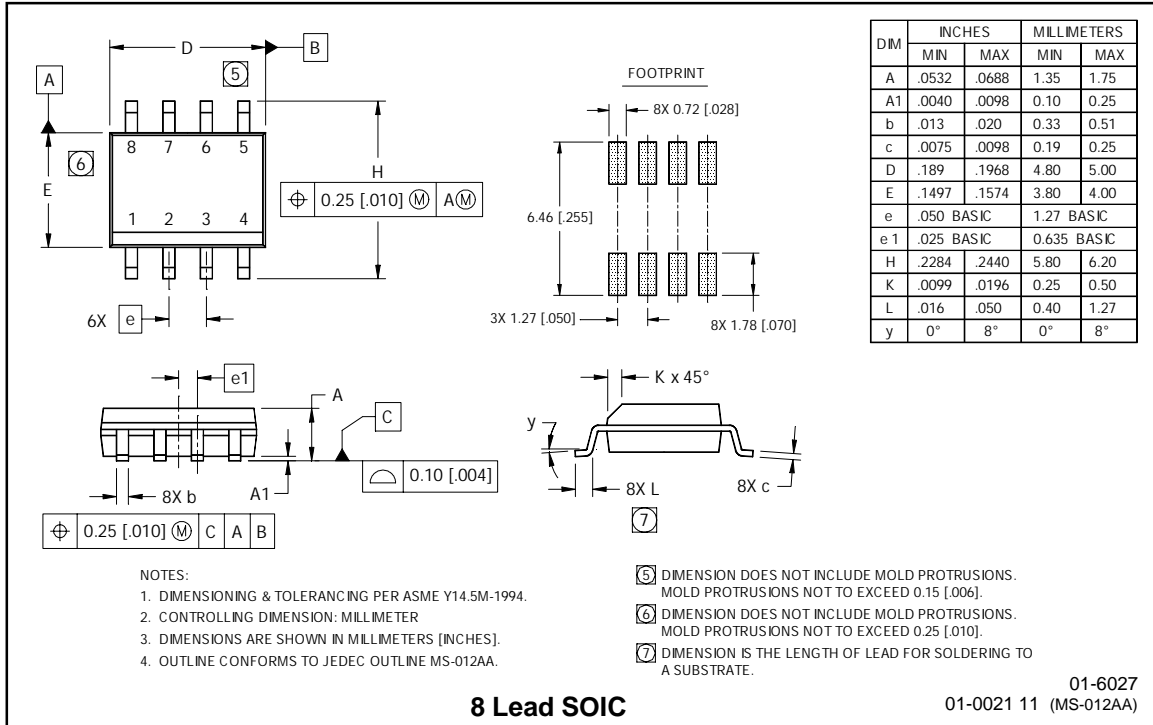
Figure 23B. Output Sink Current vs Voltage

IR2101(S)/IR2102(S) & (PbF)

Case outlines



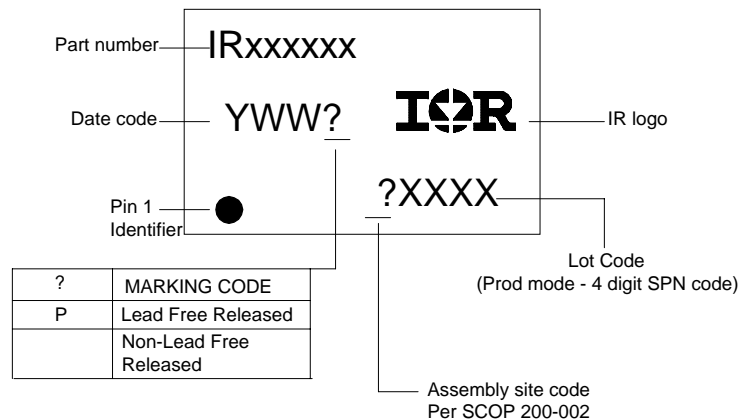
8 Lead PDIP



8 Lead SOIC

IR2101(S)/IR2102(S) & (PbF)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2101 order IR2101
 8-Lead SOIC IR2101S order IR2101S
 8-Lead PDIP IR2102 order IR2102
 8-Lead SOIC IR2102S order IR2102S

Leadfree Part

8-Lead PDIP IR2101 order IR2101PbF
 8-Lead SOIC IR2101S order IR2101SPbF
 8-Lead PDIP IR2102 order IR2102PbF
 8-Lead SOIC IR2102S order IR2102SPbF