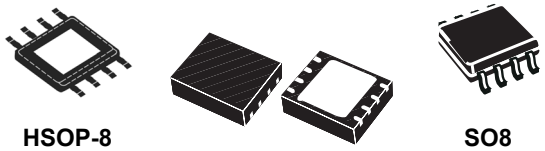
ST1S40

3 A DC step-down switching regulator

Datasheet - production data



HSOP-8 SO8

VFQFPN 4 x 4

Features

- 3 A DC output current
- 4.0 V to 18 V input voltage
- Output voltage adjustable from 0.8 V
- 850 kHz switching frequency
- Internal soft-start
- Integrated 95 mΩ and 69 mΩ Power MOSFETs
- All ceramic capacitor
- Enable
- Cycle-by-cycle current limiting
- Current fold back short-circuit protection
- Available in HSOP-8, VFQFPN4x4-8L, and SO8 packages

Applications

- µP/ASIC/DSP/FPGA core and I/O supplies
- Point of load for: STB, TVs, DVD
- Optical storage, hard disk drive, printers, audio/graphic cards

Description

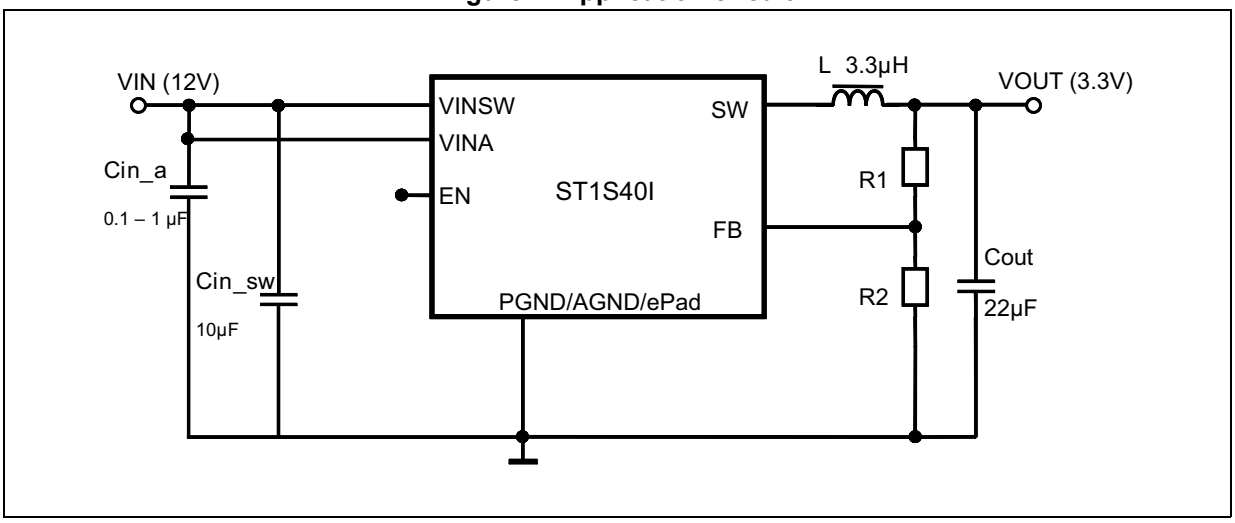
The ST1S40 device is an internally compensated 850 kHz fixed-frequency PWM synchronous step-down regulator. The ST1S40 operates from 4.0 V to 18 V input, while it regulates an output voltage as low as 0.8 V and up to V_{IN}.

The ST1S40 integrates a 95 mΩ high side switch and 69 mΩ synchronous rectifier allowing very high efficiency with very low output voltages.

The peak current mode control with internal compensation delivers a very compact solution with a minimum component count.

The ST1S40 is available in HSOP-8, VFQFPN 4 mm x 4 mm - 8 lead, and standard SO8 package.

Figure 1. Application circuit



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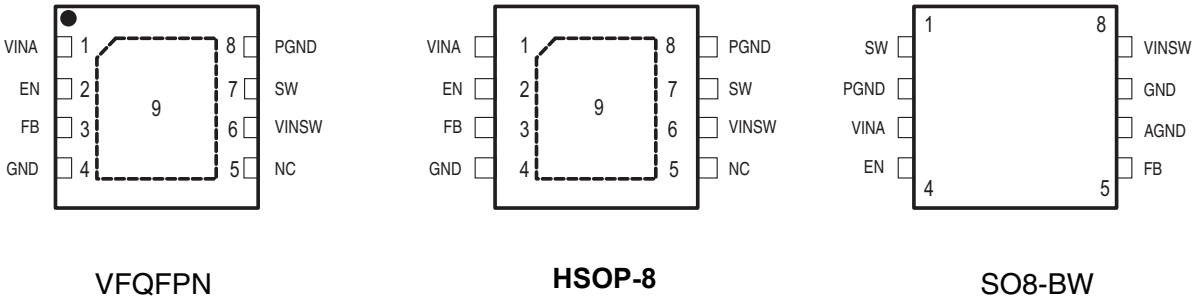
1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



VFQFPN **HSOP-8** SO8-BW

1.2 Pin description

Table 1. Pin description

No.		Type	Description
VFQFPN and HSOP-8	S08-BW		
1	3	V_{INA}	Unregulated DC input voltage
2	4	EN	Enable input. With EN higher than 1.2 V the device in ON and with EN lower than 0.4 V the device is OFF (ST1S40Ixx).
3	5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8 V. To have higher regulated voltages an external resistor divider is required from Vout to the FB pin.
4	6	AGND	Ground
5	-	NC	It can be connected to ground
6	8	VINSW	Power input voltage
7	1	SW	Regulator output switching pin
8	2	PGND	Power ground
-	7		Ground
9	-	ePad	Exposed pad mandatory connected to ground

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{INSW}	Power input voltage	-0.3 to 20	V
V_{INA}	Input voltage	-0.3 to 20	
V_{EN}	Enable voltage	-0.3 to V_{INA}	
V_{SW}	Output switching voltage	-1 to V_{IN}	
		-2 V to -1 V for 50 nsec	
V_{FB}	Feedback voltage	-0.3 to 2.5	
I_{FB}	FB current	-1 to +1	mA
P_{TOT}	Power dissipation at T_A < 60 °C	2.25 (HSOP-8/DFN4x4); 1.6 SO8-BW	W
T_{OP}	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient(1)	VFQFPN	40	°C/W
		HSOP-8	40	
		SO8-BW	55	

1. Package mounted on the demonstration board.

4 Electrical characteristics

T_J = 25 °C, V_{CC}= 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
V_{IN}	Operating input voltage range	(1)	4		18	V
V_{INON}	Turn-on V_{CC} threshold	(1)		2.9		
V_{INHYS}	Threshold hysteresis	(1)		0.250		
R_{DSON}-P	High side switch ON resistance	I_{SW} = 750 mA		95		mΩ
R_{DSON}-N	Low side switch ON resistance	I_{SW} = 750 mA		69		mΩ
I_{LIM}	Maximum limiting current	(2)	4.0		6.0	A
	Oscillator					
F_{SW}	Switching frequency		0.7	0.85	1	MHz
D_{MAX}	Maximum duty cycle	(2)	100			%
	Dynamic characteristics					
V_{FB}	Feedback voltage		0.784	0.8	0.816	V
		(1)	0.776	0.8	0.824	
$\%V_{OUT}/\Delta I_{OUT}$	Reference load regulation	Isw = 10 mA to I_{LIM}(2)		0.5		%
$\%V_{OUT}/\Delta V_{IN}$	Reference line regulation	V_{IN} = 4.0 V to 18 V(2)		0.4		%
	DC characteristics					
I_Q	Quiescent current	Duty cycle = 0, no load V_{FB} = 1.2 V		1.5	2.5	mA
I_{QST-BY}	Total standby quiescent current	OFF		2	15	µA
IFB	FB bias current			50		
	Enable					
V_{EN}	EN threshold voltage	Device ON level	1.2			V
		Device OFF level			0.4	
I_{EN}	EN current			2		µA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
	Soft start					
T_{SS}	Soft-start duration			1		ms
	Protection					
T_{SHDN}	Thermal shutdown			150		°C
	Hysteresis			15		

1. Specification referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

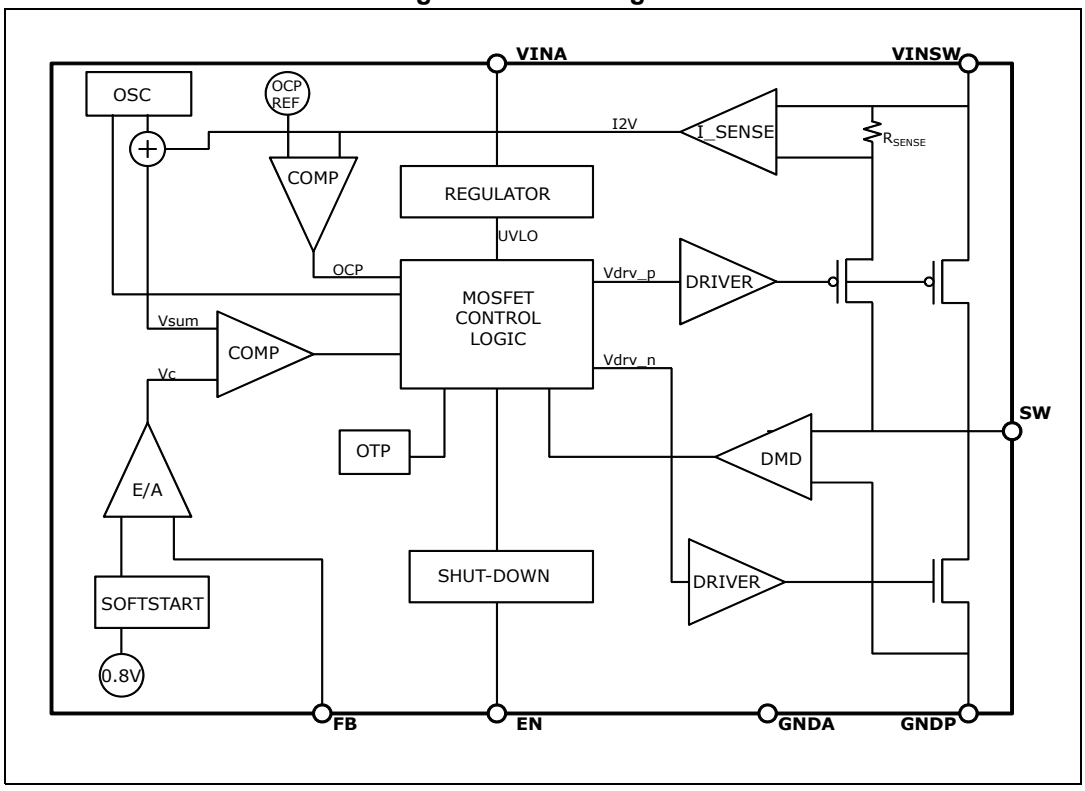
5 Functional description

The ST1S40 device is based on a “peak current mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.8 V) providing an error signal that, compared to the output of the current sense amplifier, controls the ON and OFF time of the power switch.

The main internal blocks are shown in the block diagram in *Figure 3*. They are:

- A fully integrated oscillator that provides the internal clock and the ramp for the slope compensation avoiding sub-harmonic instability
- The soft-start circuitry to limit inrush current during the startup phase
- The transconductance error amplifier with integrated compensation network
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switches
- The drivers for embedded P-channel and N-channel Power MOSFET switches
- The high side current sensing block
- The low side current sense to implement diode emulation
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages
- A thermal shutdown block, to prevent thermal run-away.

Figure 3. Block diagram



5.1 Internal soft-start

The soft-start is essential to assure correct and safe startup of the step-down converter. It avoids inrush current surge and causes the output voltage to increase monothonically.

The soft-start is performed by ramping the non-inverting input (V_{REF}) of the error amplifier from 0 V to 0.8 V in around 1 ms.

5.2 Error amplifier and control loop stability

The error amplifier compares the FB pin voltage with the internal 0.8 V reference and it provides the error signal to be compared with the output of the current sense circuitry, that is the high side Power MOSFET current. Comparing the output of the error amplifier and the peak inductor current implements the peak current mode control loop.

The error amplifier is a transconductance amplifier (OTA). The uncompensated characteristics are listed in *Table 5.*

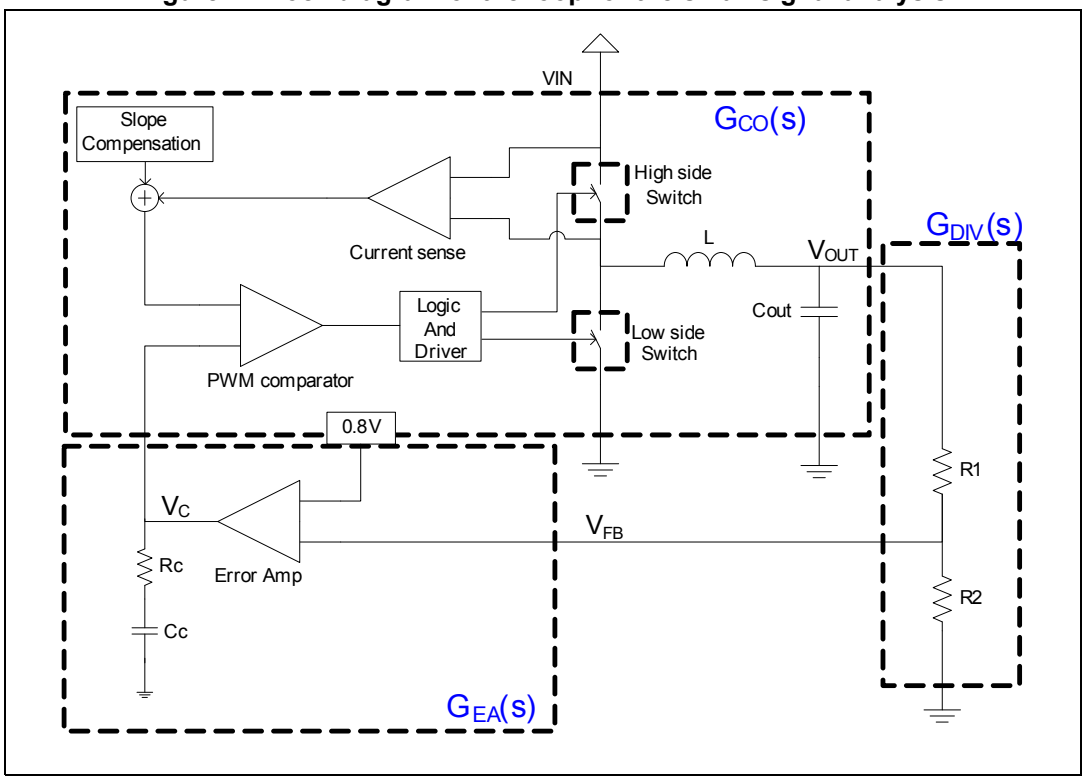
Table 5. Error amplifier characteristics

Parameter	Value
DC Gain	95 dB
Gm	251 µA/V
Ro	240 MΩ

The ST1S40 device embeds the compensation network that assures the stability of the loop in the whole operating range. All the tools needed to check the loop stability are shown below.

Figure 4 shows the simple small signal model for the peak current mode control loop.

Figure 4. Block diagram of the loop for the small signal analysis



Three main terms can be identified to obtain the loop transfer function:

1. from control (output of E/A) to output, $G_{CO}(s)$
2. from output (Vout) to the FB pin, $G_{DIV}(s)$
3. from the FB pin to control (output of E/A), $G_{EA}(s)$.

The transfer function from control to output $G_{CO}(s)$ results:

Equation 1

$$G_{CO}(s) = \frac{R_{LOAD}}{R_i} \cdot \frac{1}{1 + \frac{R_{out} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_{LOAD} represents the load resistance, R_i (0.3 Ω) the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts for the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 2

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 3

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 4

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the ON time slope of the sensed inductor current, S_e the slope of the external ramp (V_{PP} peak-to-peak amplitude 1.25 V) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

Equation 5

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

Equation 6

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

and

Equation 7

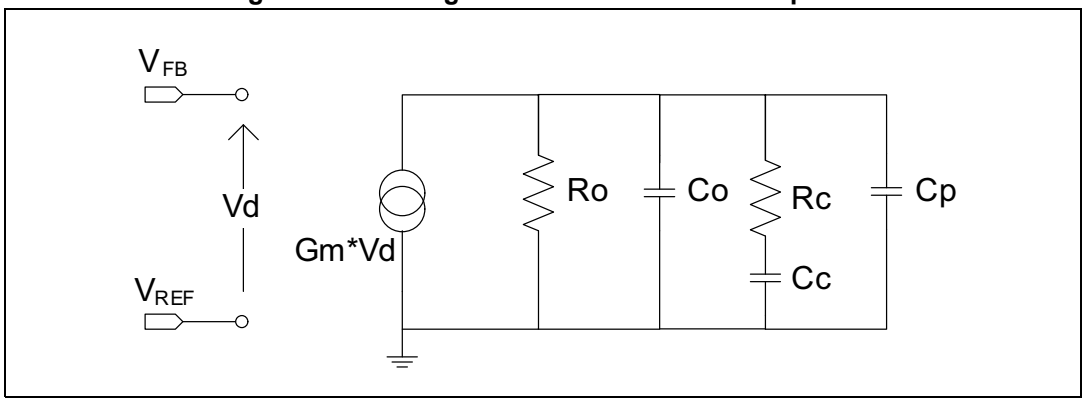
$$\omega_n = \pi \cdot f_{SW}$$

The resistor to adjust the output voltage gives the term from output voltage to the FB pin. $G_{DIV}(s)$ is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

The transfer function from FB to Vcc (output of E/A) introduces the singularities (poles and zeros) to stabilize the loop. *Figure 5* shows the small signal model of the error amplifier with the internal compensation network.

Figure 5. Small signal model for the error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability and can be neglected.

So $G_{EA}(s)$ results:

Equation 8

$$G_{EA}(s) = \frac{G_{EA0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

where $G_{EA} = G_m \cdot R_o$

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 9

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 10

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 11

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is R_C = 70 kΩ, C_C = 195 pF while C_P and C_O can be considered as negligible. The error amplifier output resistance is 240 MΩ so the relevant singularities are:

Equation 12

$$f_Z = 11,6\ \text{kHz} \qquad f_{P\,LF} = 3,4\ \text{Hz}$$

so by closing the loop, the loop gain $G_{LOOP}(s)$ is:

Equation 13

$$G_{LOOP}(s) = G_{CO}(s) \cdot G_{DIV}(s) \cdot G_{EA}(s)$$

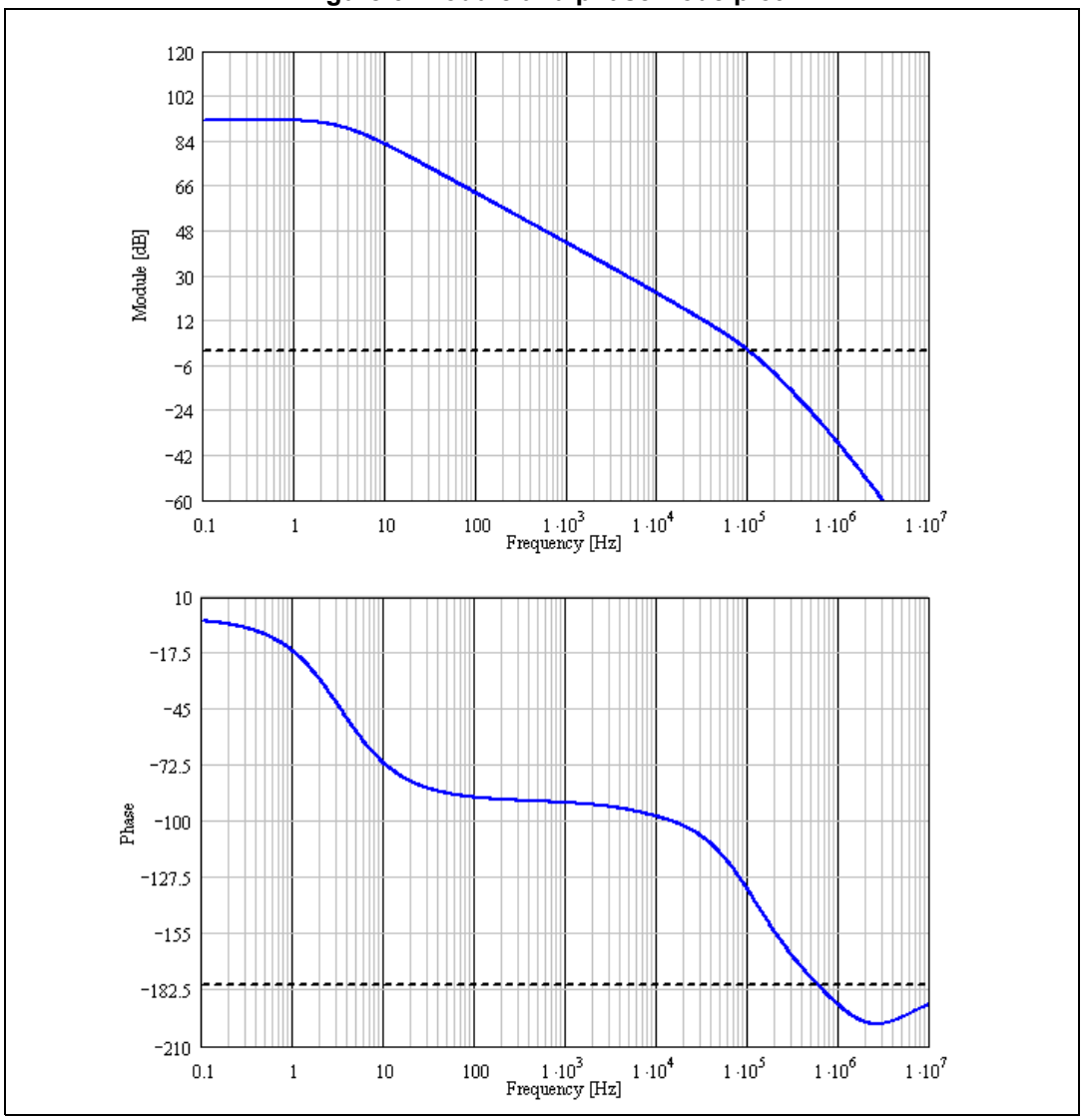
Example:

VIN = 12 V, VOUT = 1.2 V, Iomax = 3 A, L = 1.5 µH, Cout = 47 µF (MLCC), R1 = 10 kΩ, R2 = 20 kΩ (see Section 6.2 and Section 6.3 for inductor and output capacitor selection guidelines).

The module and phase Bode plot are reported in Figure 6.

The bandwidth is 100 kHz and the phase margin is 45 degrees.

Figure 6. Module and phase Bode plot



5.3 Overcurrent protection

The ST1S40 device implements the pulse-by-pulse overcurrent protection. The peak current is sensed through the high side Power MOSFET and when it exceeds the first overcurrent threshold (OCP1) the high side is immediately turned off and the low side conducts the inductor current for the rest of the clock period.

During overload condition, since the duty cycle is not set by the control loop but is limited by the overcurrent threshold, the output voltage drops out of regulation. If the feedback falls below 0.3 V the switching frequency is reduced to one fourth and the current limit threshold is folded back to around 2 A. Thanks to the current and frequency fold back the stress on the device and on the external power components is reduced in case of severe overload or dead-short to ground of the output.

The current fold back is disabled during the startup, in order to allow the Vout to rise up properly in case of the big output capacitor requiring high extra current to be charged.

An additional mechanism is protecting the device in case of short-circuit on the output and high input voltage. A further threshold (OCP2, 1A higher than OCP1) is compared to the inductor current. If the inductor current exceeds OCP2, the device stops switching and restarts with a soft-start cycle.

5.4 Enable function

The enable feature allows the device to be put into standby mode. With the EN pin lower than 0.4 V, the device is disabled and the power consumption is reduced to less than 15 μA. With the EN pin higher than 1.2 V, the device is enabled. If the EN pin is left floating, an internal pull-down ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{IN} compatible.

5.5 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 °C. Once the junction temperature goes back to about 130 °C, the device restarts in normal operation.

6 Application information

6.1 Input capacitor selection

The capacitor connected to the input must be capable of supporting the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have an RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 14

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where Io is the maximum DC output current, D is the duty cycle, η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and is equal to Io/2.

The peak-to-peak voltage across the input capacitor can be calculated as:

Equation 15

$$V_{PP} = \frac{I_O}{C_{IN} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

where ESR is the equivalent series resistance of the capacitor.

Given the physical dimension, ceramic capacitors can well meet the requirements of the input filter sustaining a higher input RMS current than electrolytic / tantalum types. In this case the equation of C_{IN} as a function of the target peak-to-peak voltage ripple (V_{PP}) can be written as follows:

Equation 16

$$C_{IN} = \frac{I_O}{V_{PP} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

neglecting the small ESR of ceramic capacitors.

Considering η = 1, this function has its maximum in D = 0.5, therefore, given the maximum peak-to-peak input voltage (V_{PP_MAX}), the minimum input capacitor (C_{IN_MIN}) value is:

Equation 17

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot F_{SW}}$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage ripple in the order of 1% of V_{INMAX}.

In *Table 6* some multi layer ceramic capacitors suitable for this device are reported.

Table 6. Input MLCC capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)
Murata	GRM31	10	25
	GRM55	10	25
TDK	C3225	10	25

A ceramic bypass capacitor, as close as possible to the V_{INA} pin, so that additional parasitic ESR and ESL are minimized, is suggested in order to prevent instability on the output voltage due to noise. The value of the bypass capacitor can go from 330 nF to 1 µF.

6.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value, to have the expected current ripple, must be selected. The rule to fix the current ripple value is to have a ripple at 20% to 40% of the output current.

In continuous current mode (CCM), the inductance value can be calculated by *Equation 18*

Equation 18

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

where T_{ON} is the conduction time of the high side switch and T_{OFF} is the conduction time of the low side switch (in CCM, $F_{SW} = 1/(T_{ON} + T_{OFF})$). The maximum current ripple, given the Vout, is obtained at maximum T_{OFF}, that is at minimum duty cycle. So by fixing ΔI_L = 20% to 30% of the maximum output current, the minimum inductance value can be calculated:

Equation 19

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SWMIN}}$$

where F_{SWMIN} is the minimum switching frequency, according to *Table 4*

The peak current through the inductor is given by:

Equation 20

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

so if the inductor value decreases, the peak current (that must be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

In *Table 7* below some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XPL7030	2.2 to 4.7	6.8 to 10.5
	MSS1048	2.2 to 6.8	4.14 to 6.62
	MSS1260	10	5.5
Wurth	WE-HC/HCA	3.3 to 4.7	7 to 11
	WE-TPC typ XLH	3.6 to 6.2	4.5 to 6.4
	WE-PD type L	10	5.6
TDK	RLF7030T	2.2 to 4.7	4 to 6

6.3 Output capacitor selection

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge or discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 21

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

For ceramic (MLCC) capacitors the capacitive component of the ripple dominates the resistive one. Whilst for electrolytic capacitors the opposite is true.

Since the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop.

The equations of *Section 5.2* help to check loop stability given the application conditions, the value of the inductor, and of the output capacitor.

In *Table 8* some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

6.4 Thermal dissipation

The thermal design is important in order to prevent thermal shutdown of the device if junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) conduction losses due to the ON resistance of high side switch (R_{HS}) and low side switch (R_{LS}); these are equal to:

Equation 22

$$P_{COND} = R_{HS} \cdot I_{OUT}^2 \cdot D + R_{LS} \cdot I_{OUT}^2 \cdot (1 - D)$$

where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but is actually slightly higher to compensate the losses of the regulator.

b) switching losses due to high side Power MOSFET turn ON and OFF; these can be calculated as:

Equation 23

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high side power switch (V_{DS}) and the current flowing into it during turn ON and turn OFF phases, as shown in *Figure 7*. T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

c) Quiescent current losses, calculated as:

Equation 24

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current (I_Q = 2.5 mA maximum).

The junction temperature T_J can be calculated as:

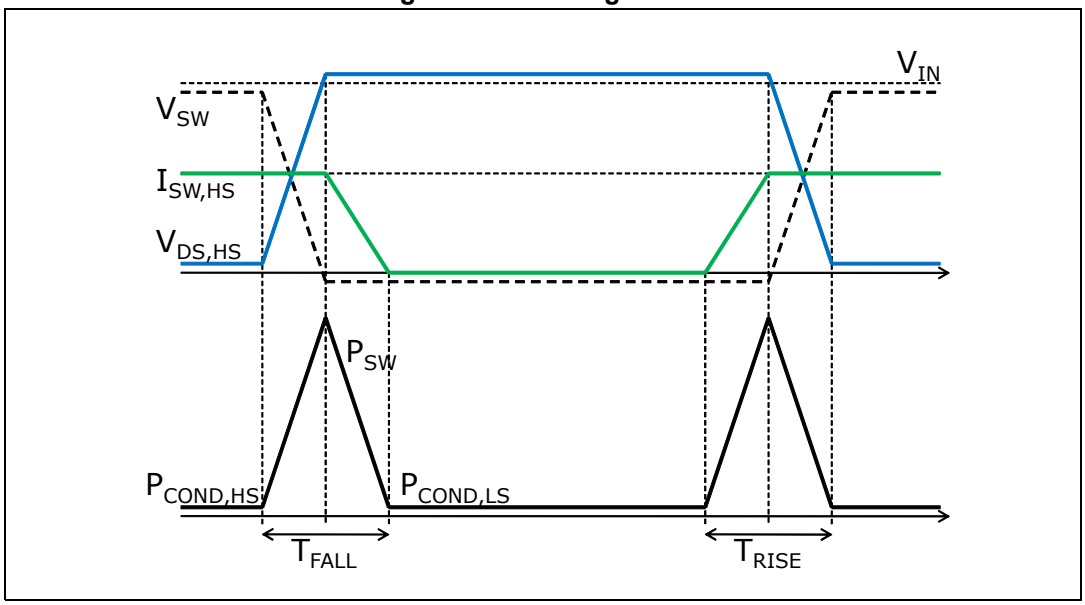
Equation 25

$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen.

Rth_{JA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The Rth_{JA} measured on the demonstration board described in the following paragraph is about 40 °C/W for the VFQFPN and HSOP packages and about 55 °C/W for the SO8-BW package.

Figure 7. Switching losses



6.5 Layout consideration

The PC board layout of switching DC-DC regulator is very important in order to minimize the noise injected in high impedance nodes, to reduce interferences generated by the high switching current loops, and to optimize the reliability of the device.

In order to avoid EMC problems, the high switching current loops must be as short as possible. In the buck converter there are two high switching current loops: during the ON time, the pulsed current flows through the input capacitor, the high side power switch, the inductor and the output capacitor; during the OFF time, through the low side power switch, the inductor and the output capacitor.

The input capacitor connected to VINSW must be placed as close as possible to the device, to avoid spikes on VINSW due to the stray inductance and the pulsed input current.

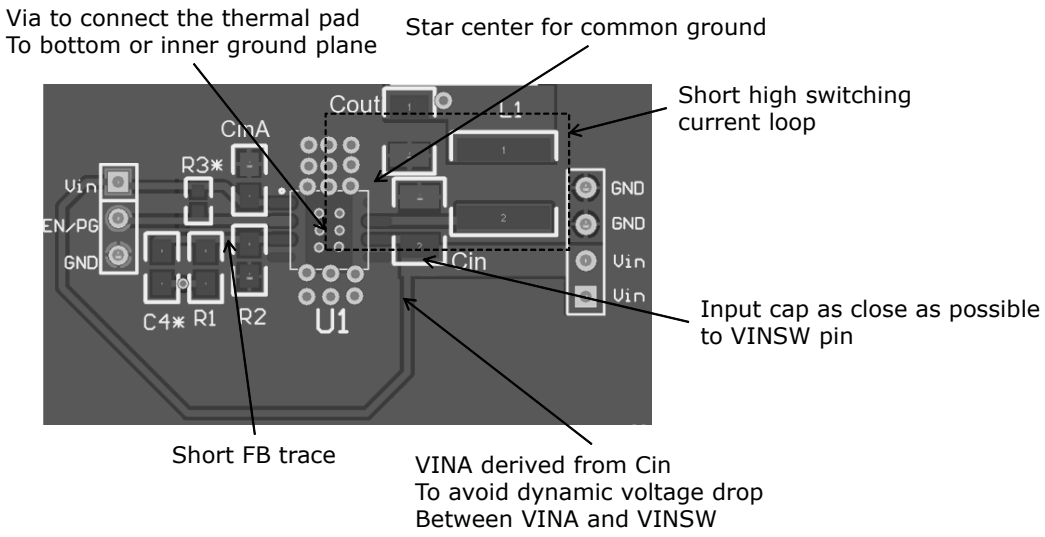
In order to prevent dynamic unbalance between VINSW and V_{INA}, the trace connecting the V_{INA} pin to the input must be derived from VINSW.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interferences can be minimized through the routing of the feedback node with a very short trace and as far as possible from the high current paths.

A single point connection from signal ground to power ground is suggested.

Thanks to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane, soldered to the exposed pad, enhances the thermal performance of the converter allowing high power conversion.

Figure 8. PCB layout guidelines



7 Demonstration board

Figure 9. Demonstration boards schematic

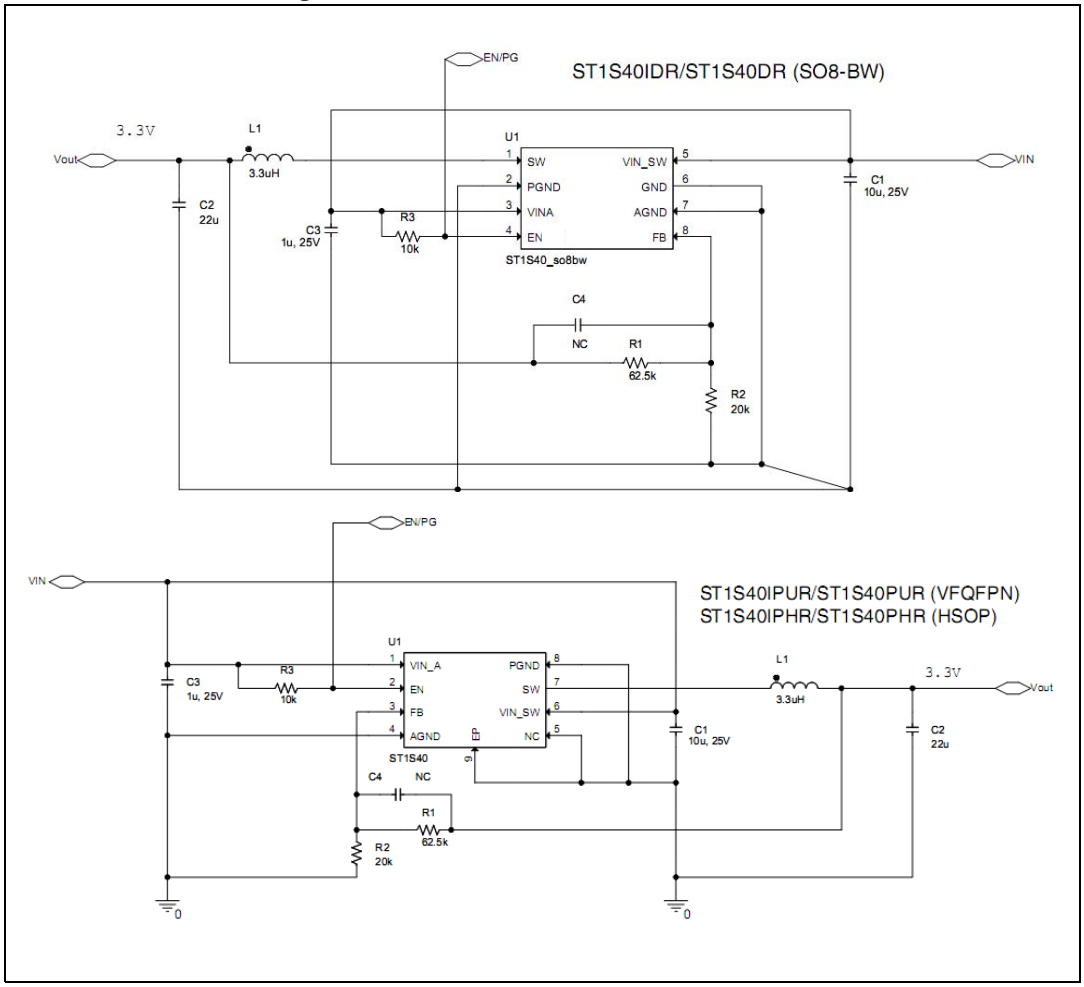


Table 9. Component list

Reference	Part number	Description	Manufacturer
U1	ST1S40		STMicroelectronics®
L1	DRA74 3R3	3.3 µH, Isat = 5.4 A	Coiltronics
C1	C3225X7RE106K	10 µF 25 V X7R	TDK
C2	C3225X7R1C226M	22 µF 16 V X7R	TDK
C3		1 µF 25 V X7R	
C4		NC	
R1		62.5 kΩ	
R2		20 kΩ	
R3		10 kΩ	

Figure 10. Demonstration board PCB top and bottom: HSOP-8 package

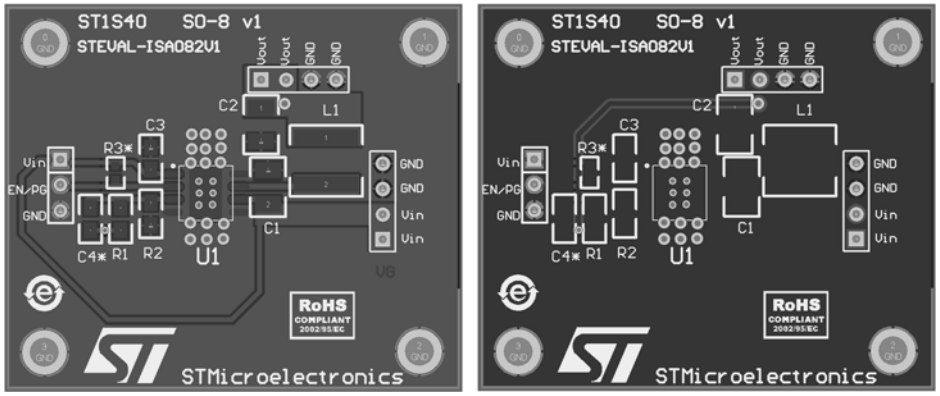


Figure 11. Demonstration board PCB top and bottom: VFQFPN package

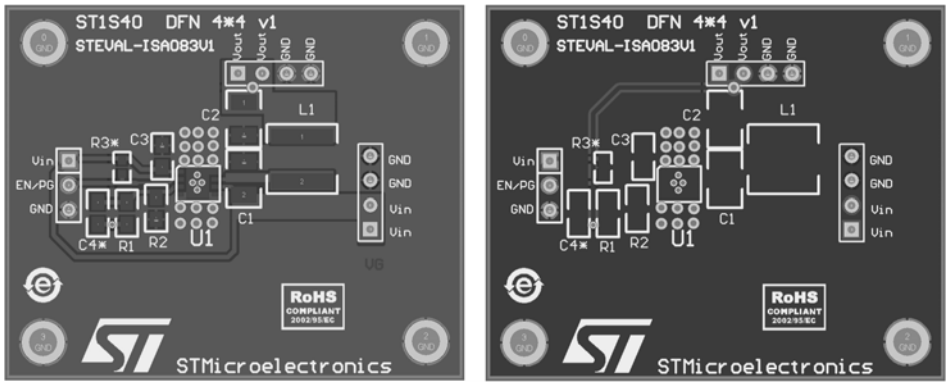
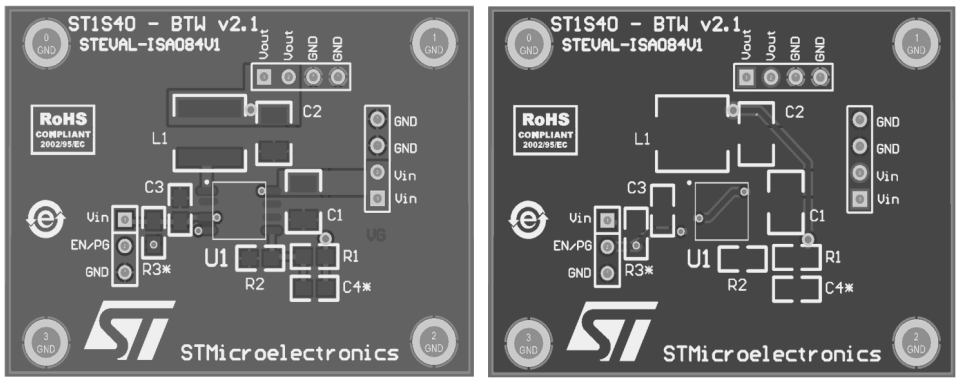


Figure 12. Demonstration board PCB top and bottom: SO8-BW package



8 Typical characteristics

Figure 13. Efficiency vs. I_{OUT}

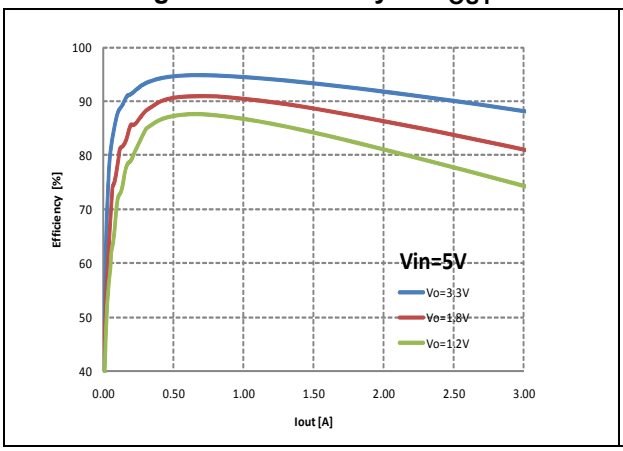


Figure 14. Efficiency vs. I_{OUT}

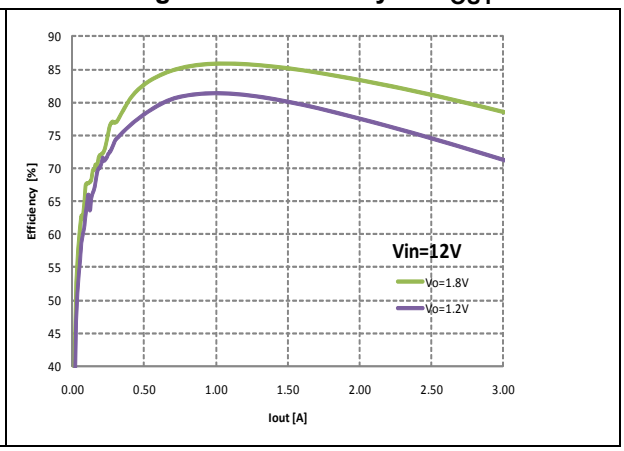


Figure 15. Efficiency vs. I_{OUT}

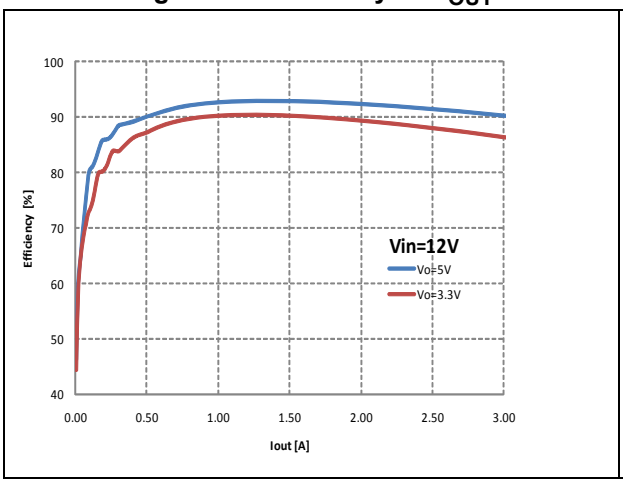


Figure 16. Overcurrent protection

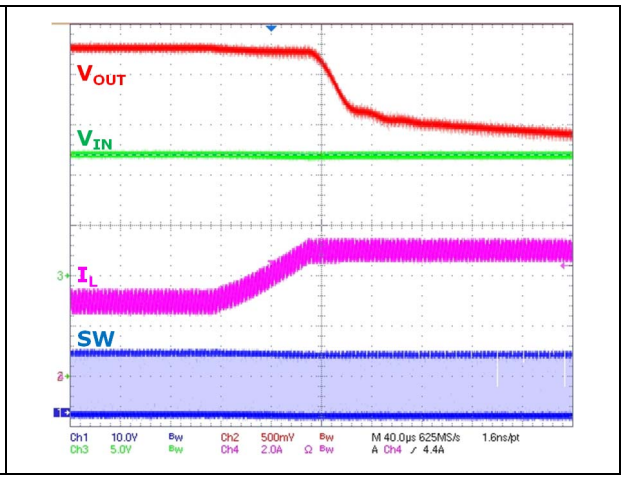


Figure 17. Short-circuit protection

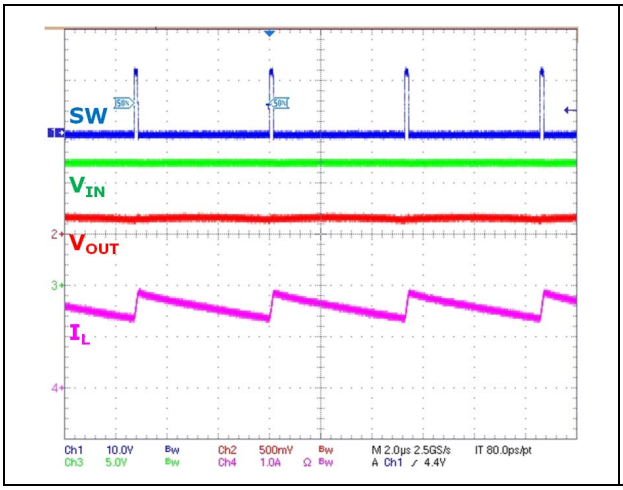
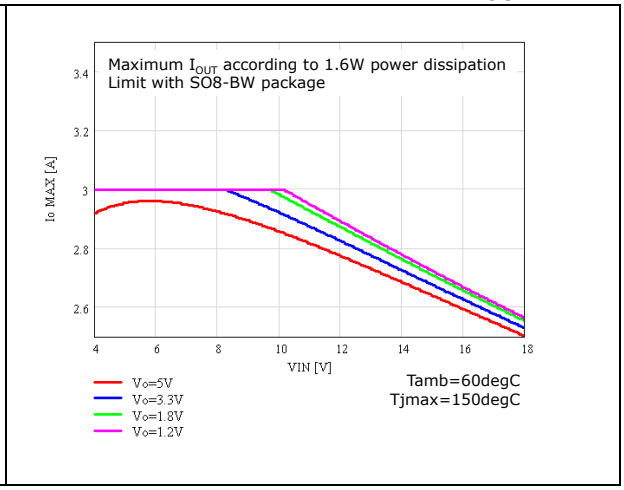


Figure 18. SO8-BW maximum I_{OUT}



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 19. VFQFPN8 (4 x 4 x 1.0 mm) package outline

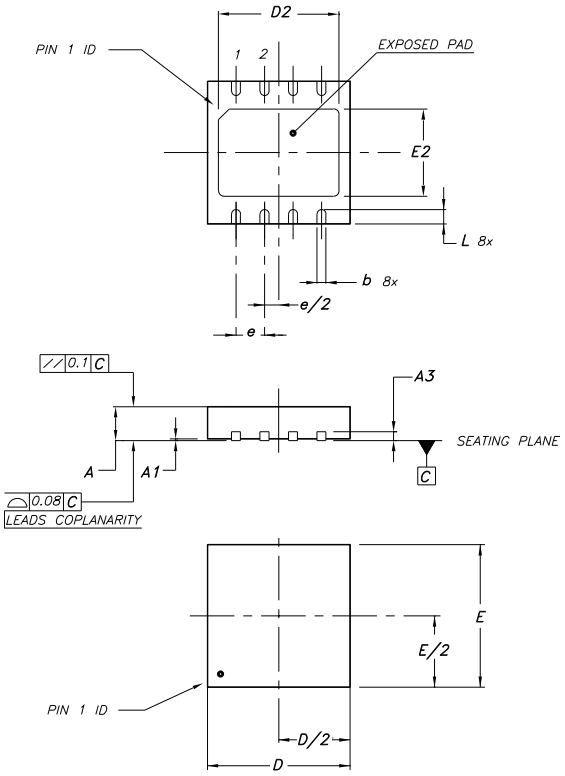


Table 10. VFQFPN8 (4 x 4 x 1.0 mm) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.23	0.30	0.38	0.009	0.0117	0.0149
D	3.90	4.00	4.10	0.153	0.157	0.161
D2	2.82	3.00	3.23	0.111	0.118	0.127
E	3.90	4.00	4.10	0.153	0.157	0.161
E2	2.05	2.20	2.30	0.081	0.087	0.091
e		0.80			0.031	
L	0.40	0.50	0.60	0.016	0.020	0.024

Figure 20. SO8-BW package outline

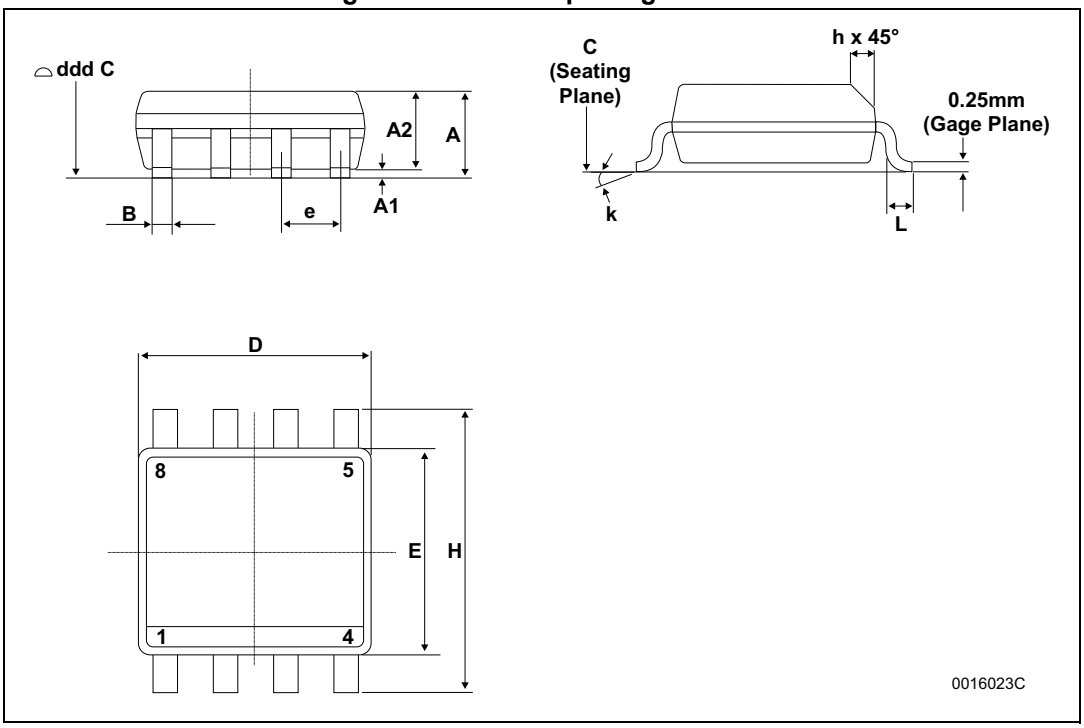


Table 11. SO8-BW package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	135		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.001
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D(1)	4.80		5.00	0.1890	0.1929	0.1969
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0°(min.), 8° (max.)					
ddd			0.10			0.0039

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs must not exceed 0.15 mm (.006 inch) in total (both sides).

Figure 21. HSOP-8 package outline

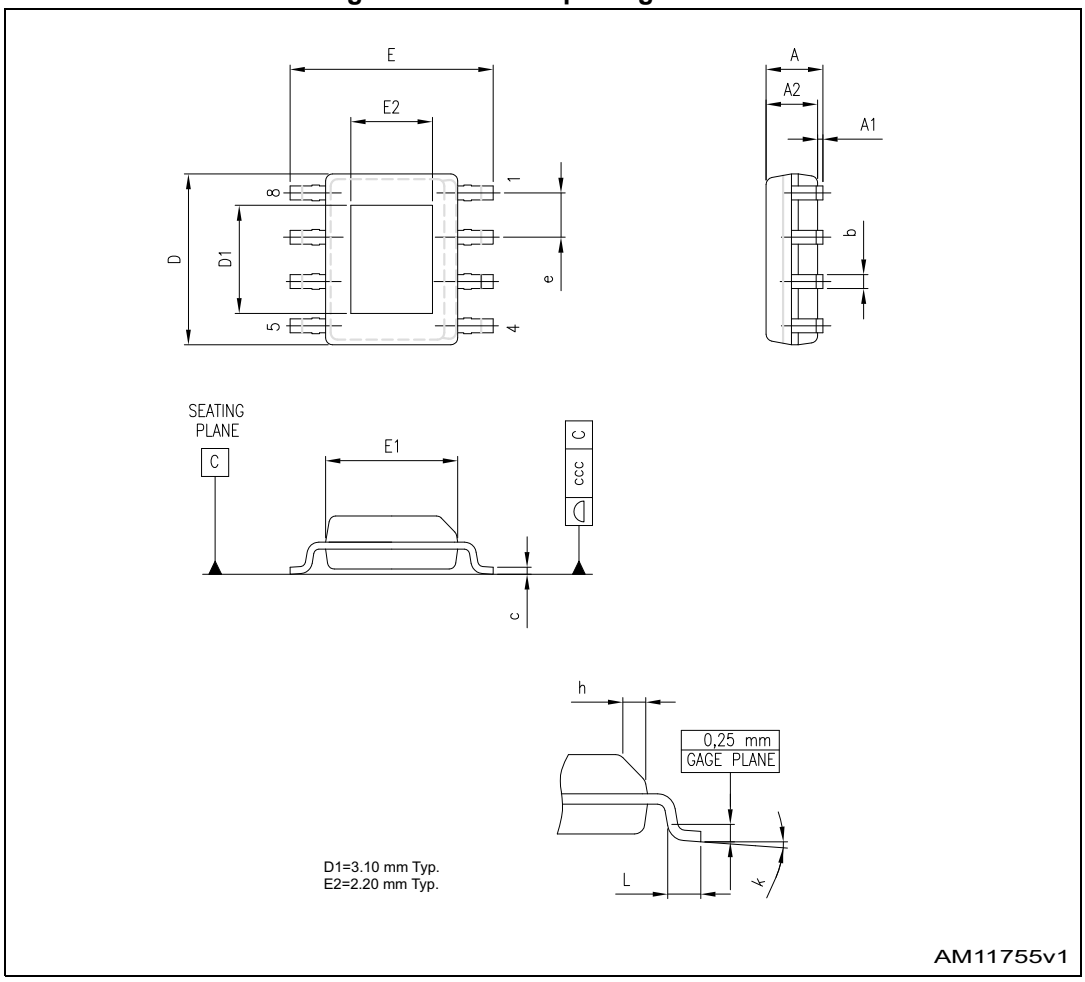


Table 12. HSOP-8 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.70			0.0669
A1	0.00		0.150		0.00	0.0059
A2	1.25			0.0492		
b	0.31		0.51	0.0122		0.0201
c	0.17		0.25	0.0067		0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
E	5.80	6.00	6.20	0.2283	0.2362	0.2441
E1	3.80	3.90	4.00	0.1496	0.1535	0.1575
e		1.27			0.0500	
h	0.25		0.50	0.0098		0.0197
L	0.40		1.27	0.0157		0.0500
k	0.00		8.00			0.3150
ccc			0.10			0.0039

10 Order codes

Table 13. Ordering information

Order codes	Package	Function
ST1S40IPUR	VFQFPN 4 x 4 8L	Enable
ST1S40IPHR	HSOP-8	
ST1S40IDR	SO8-BW	

11 Revision history

Table 14. Document revision history

Date	Revision	Changes
15-Dec-2010	1	First release
04-Mar-2011	2	Updated: *Table 1*, *Table 2*, *Table 3* and *Table 13*.
20-Dec-2011	3	Updated cover page: *Table 1*, *Table 2*, *Section 5* Added *Section 6*, *Section 7* and *Section 8*
01-Mar-2012	4	HSOP8 mechanical data and package dimensions have been updated.
10-Oct-2013	5	Updated *Table 2* - added value “-2 V to -1 V for 50 nsec” for parameter V_{SW}. Reformatted *Section 9: Package information* - reversed order of *Figure 19* and *Table 10*, *Figure 20* and *Table 11*, *Figure 21* and *Table 12*. Minor corrections throughout document.