Atmel

Atmel 8-bit AVR Microcontroller with 512/1024 Bytes In-System Programmable Flash

ATtiny4 / ATtiny5 / ATtiny9 / ATiny10

DATASHEET SUMMARY

Introduction

The Atmel® ATtiny4/5/9/10 is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny4/5/9/10 achieves throughputs close to 1 MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

Feature

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 54 Powerful Instructions
  - Most Single Clock Cycle Execution
  - 16 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 12 MIPS Throughput at 12 MHz
- Non-volatile Program and Data Memories
  - 512/1024 Bytes of In-System Programmable Flash Program Memory
  - 32 Bytes Internal SRAM
  - Flash Write/Erase Cycles: 10,000
  - Data Retention: 20 Years at 85°C / 100 Years at 25°C
- Peripheral Features
  - QTouch® Library Support for Capacitive Touch Sensing (1 Channel)
  - One 16-bit Timer/Counter with Prescaler and Two PWM Channels
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - 4-channel, 8-bit Analog to Digital Converter (ATtiny5/10, only)
  - On-chip Analog Comparator
- Special Microcontroller Features
  - In-System Programmable (at 5V, only)

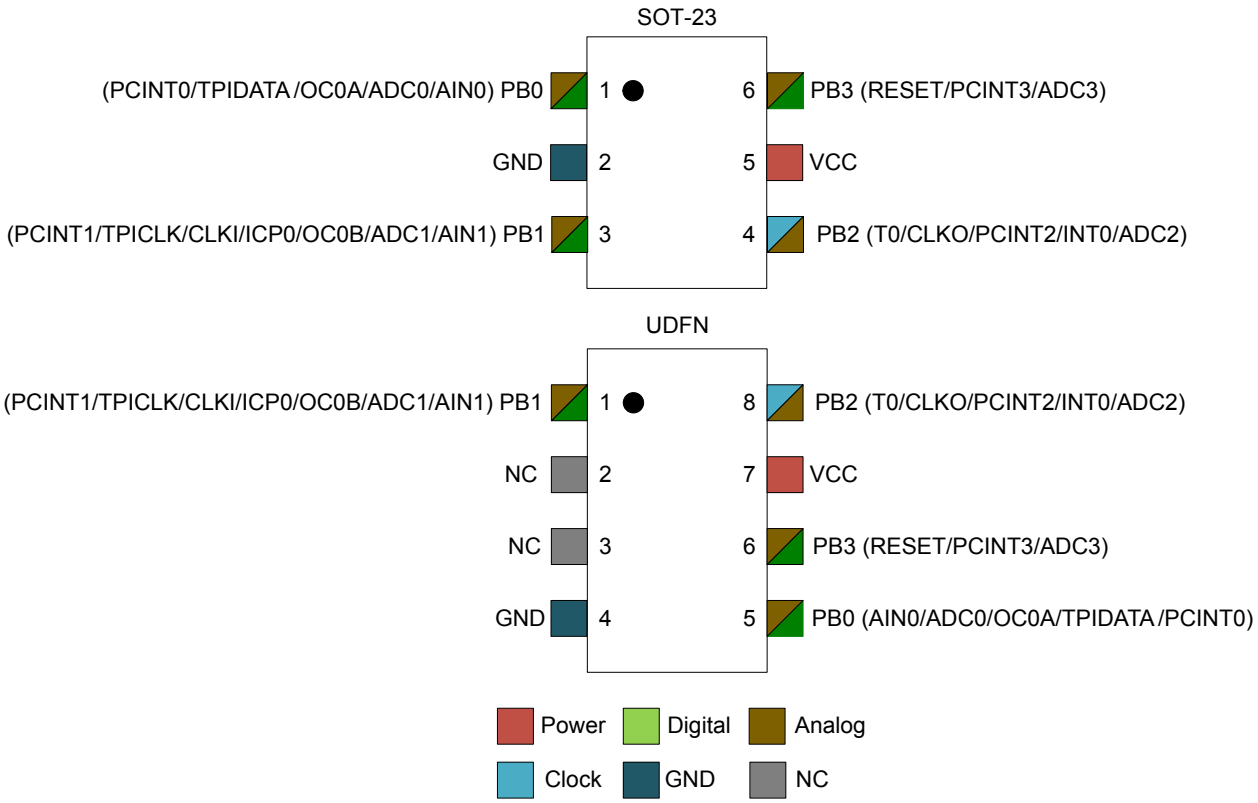
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Supply Voltage Level Monitor with Interrupt and Reset
  - Internal Calibrated Oscillator
- I/O and Packages
  - Four Programmable I/O Lines
  - 6-pin SOT and 8-pad UDFN
- Operating Voltage:
  - 1.8 - 5.5V
- Programming Voltage:
  - 5V
- Speed Grade:
  - 0 - 4 MHz @ 1.8 - 5.5V
  - 0 - 8 MHz @ 2.7 - 5.5V
  - 0 - 12 MHz @ 4.5 - 5.5V
- Industrial and Extended Temperature Ranges
- Low Power Consumption
  - Active Mode:
    - 200µA at 1MHz and 1.8V

    Idle Mode:
    - 25µA at 1MHz and 1.8V
  - Power-down Mode:
    - <0.1µA at 1.8V

Table of Contents

1. Pin Configurations

Figure 1-1. Pinout of ATtiny4/5/9/10



1.1. Pin Descriptions

1.1.1. VCC

Digital supply voltage.

1.1.2. GND

Ground.

1.1.3. Port B (PB[3:0])

This is a 4-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.4. $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in *System and Reset Characteristics of Electrical Characteristics*. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

2. Ordering Information

2.1. ATtiny4

Supply Voltage	Speed (1)	Temperature	Package (2)	Ordering Code (3)
1.8 – 5.5V	12MHz	Industrial (-40°C to 85°C) (4)	6ST1	ATTINY4-TSUR(5) ATTINY4-TSHR(6)(7)
			8MA4	ATTINY4-MAHR (7)
	10MHz	Extended (-40°C to 125°C) (8)	6ST1	ATTINY4-TSFR(5) ATTINY4-TS8R (6)(7)

Note:

1. For speed vs. supply voltage, see section *Speed*.
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS). NiPdAu finish.
3. Tape and reel.
4. Can also be supplied in wafer form. Contact your local sales office for ordering information and minimum quantities.
5. Marking details:
   - Top mark 1st line: ddddTY
   - Top mark 2nd line: wwxxx

   dddd= device, special code

   T= Type

   Y= Year last digit

   ww= calendar workweek

   xxx = trace code
6. Not recommended for new designs.TPUBSTINY-216
7. Top/bottom markings:
   - Top: T4**x**, where **x** = die revision
   - Bottom: z**H**zzz or z**8**zzz, where **H** = (-40°C to 85°C), and **8** = (-40°C to 125°C)
8. For typical and Electrical characteristics for this device please consult Appendix A, ATtiny4/5/9/10 Specification at 125°C.

Table 2-1. Package Type

6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)
8MA4	8-pad, 2 x 2 x 0.6 mm Plastic Ultra Thin Dual Flat No Lead (UDFN)

2.2. ATtiny5

Supply Voltage	Speed [1]	Temperature	Package [2]	Ordering Code [3]
1.8 – 5.5V	12MHz	Industrial (-40°C to 85°C) [4]	6ST1	ATTINY5-TSUR[5] ATTINY5-TSHR[6][7]
			8MA4	ATTINY5-MAHR [7]
	10MHz	Extended (-40°C to 125°C) [8]	6ST1	ATTINY5-TSFR[5] ATTINY5-TS8R [6][7]

Note:

1. For speed vs. supply voltage, see section *Speed*.
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS). NiPdAu finish.
3. Tape and reel.
4. Can also be supplied in wafer form. Contact your local sales office for ordering information and minimum quantities.
5. Marking details:
   - Top mark 1st line: ddddTY
   - Top mark 2nd line: wwxxx

   dddd= device, special code

   T= Type

   Y= Year last digit

   ww= calendar workweek

   xxx = trace code
6. Not recommended for new designs.TPUBSTINY-216
7. Top/bottomside markings:
   - Top: T5**x**, where **x** = die revision
   - Bottom: z**H**zzz or z**8**zzz, where **H** = (-40°C to 85°C), and **8** = (-40°C to 125°C)
8. For typical and Electrical characteristics for this device please consult Appendix A, ATtiny4/5/9/10 Specification at 125°C.

Table 2-2. Package Type

6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)
8MA4	8-pad, 2 x 2 x 0.6 mm Plastic Ultra Thin Dual Flat No Lead (UDFN)

2.3. ATtiny9

Supply Voltage	Speed [1]	Temperature	Package [2]	Ordering Code [3]
1.8 – 5.5V	12MHz	Industrial (-40°C to 85°C) [4]	6ST1	ATTINY9-TSUR[5] ATTINY9-TSHR[6][7]
			8MA4	ATTINY9-MAHR [7]
	10MHz	Extended (-40°C to 125°C) [8]	6ST1	ATTINY9-TSFR[5] ATTINY9-TS8R [6][7]

Note:

1. For speed vs. supply voltage, see section *Speed*.
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS). NiPdAu finish.
3. Tape and reel.
4. Can also be supplied in wafer form. Contact your local sales office for ordering information and minimum quantities.
5. Marking details:
   - Top mark 1st line: ddddTY
   - Top mark 2nd line: wwxxx

   dddd= device, special code

   T= Type

   Y= Year last digit

   ww= calendar workweek

   xxx = trace code
6. Not recommended for new designs.TPUBSTINY-216
7. Top/bottomside markings:
   - Top: T9**x**, where **x** = die revision
   - Bottom: z**H**zzz or z**8**zzz, where **H** = (-40°C to 85°C), and **8** = (-40°C to 125°C)
8. For typical and Electrical characteristics for this device please consult Appendix A, ATtiny4/5/9/10 Specification at 125°C.

Table 2-3. Package Type

6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)
8MA4	8-pad, 2 x 2 x 0.6 mm Plastic Ultra Thin Dual Flat No Lead (UDFN)

2.4. ATtiny10

Supply Voltage	Speed [1]	Temperature	Package [2]	Ordering Code [3]
1.8 – 5.5V	12MHz	Industrial (-40°C to 85°C) [4]	6ST1	ATTINY10-TSUR[5] ATTINY10-TSHR[6][7]
			8MA4	ATTINY10-MAHR [7]
	10MHz	Extended (-40°C to 125°C) [8]	6ST1	ATTINY10-TSFR[5] ATTINY10-TS8R [6][7]

Note:

1. For speed vs. supply voltage, see section *Speed*.
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS). NiPdAu finish.
3. Tape and reel.
4. Can also be supplied in wafer form. Contact your local sales office for ordering information and minimum quantities.
5. Marking details:
   - Top mark 1st line: ddddTY
   - Top mark 2nd line: wwxxx

   dddd= device, special code

   T= Type

   Y= Year last digit

   ww= calendar workweek

   xxx = trace code
6. Not recommended for new designs.TPUBSTINY-216
7. Top/bottomside markings:
   - Top: T10**x**, where **x** = die revision
   - Bottom: z**H**zzz or z**8**zzz, where **H** = (-40°C to 85°C), and **8** = (-40°C to 125°C)
8. For typical and Electrical characteristics for this device please consult Appendix A, ATtiny4/5/9/10 Specification at 125°C.

Table 2-4. Package Type

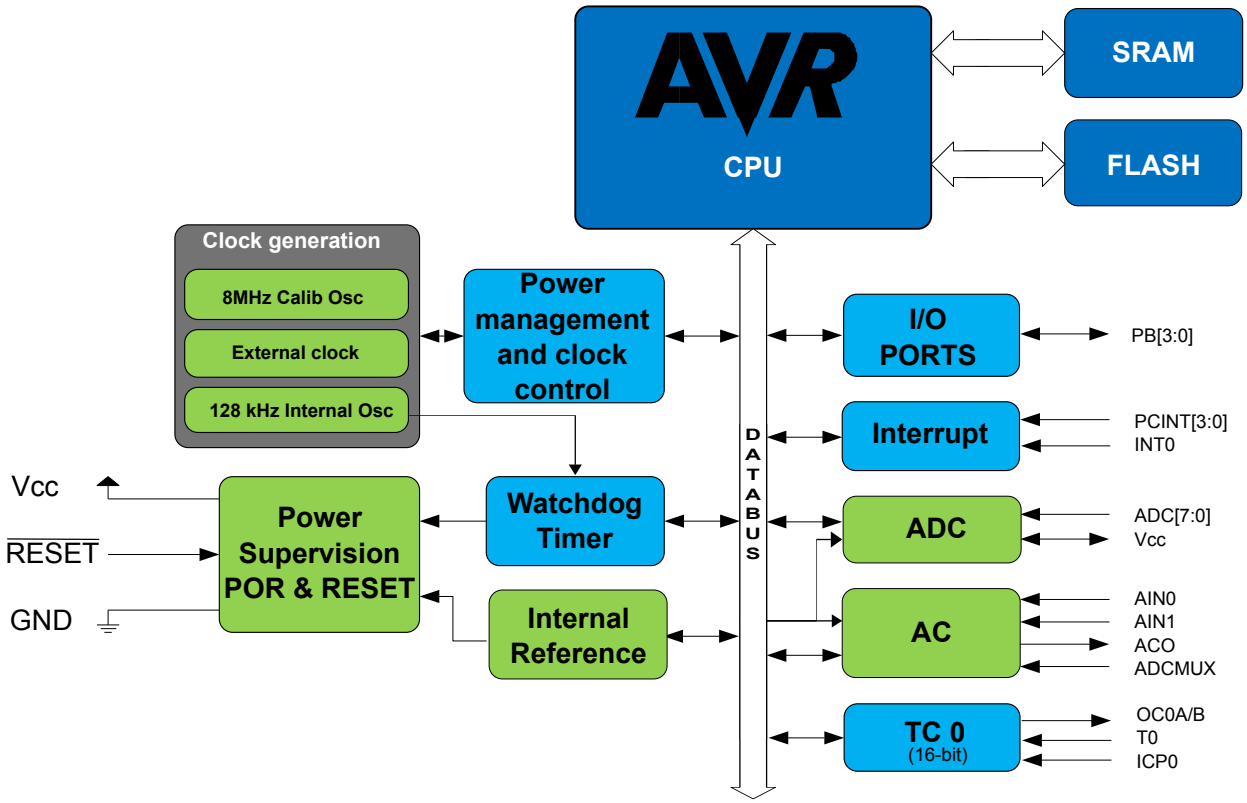
6ST1	6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)
8MA4	8-pad, 2 x 2 x 0.6 mm Plastic Ultra Thin Dual Flat No Lead (UDFN)

3. Overview

This device is low-power CMOS 8-bit microcontrollers based on the compact AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the device achieve throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

3.1. Block Diagram

Figure 3-1. Block Diagram



3.1.1. Description

The AVR core combines a rich instruction set with 16 general purpose working registers and system registers. All registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is compact and code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

This device provides the following features: 512/1024 byte of In-System Programmable Flash, 32 bytes of SRAM, four general purpose I/O lines, 16 general purpose working registers, a 16-bit timer/counter with two PWM channels, internal and external interrupts, a programmable watchdog timer with internal oscillator, an internal calibrated oscillator, and four software selectable power saving modes. ATtiny5/10 are also equipped with a four-channel and 8-bit Analog to Digital Converter (ADC).

Idle mode stops the CPU while allowing the SRAM, timer/counter, ADC (ATtiny5/10, only), analog comparator, and interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disabled until the next interrupt

or hardware reset. In Standby mode, the oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density Non-Volatile Memory (NVM) technology. The on-chip, in-system programmable Flash allows program memory to be re-programmed in-system by a conventional, non-volatile memory programmer.

The ATtiny4/5/9/10AVR are supported by a suite of program and system development tools, including macro assemblers and evaluation kits.

3.2. Comparison of ATtiny4, ATtiny5, ATtiny9 and ATtiny10

A comparison of the devices is shown in the table below.

Table 3-1. Differences between ATtiny4, ATtiny5, ATtiny9 and ATtiny10

Device	Flash	ADC	Signature
ATtiny4	512 bytes	No	0x1E 0x8F 0x0A
ATtiny5	512 bytes	Yes	0x1E 0x8F 0x09
ATtiny9	1024 bytes	No	0x1E 0x90 0x08
ATtiny10	1024 bytes	Yes	0x1E 0x90 0x03

4. General Information

4.1. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com/avr.

4.2. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

4.3. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

4.4. Capacitive Touch Sensing

4.4.1. QTouch Library

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the Atmel QTouch and Atmel QMatrix® acquisition methods.

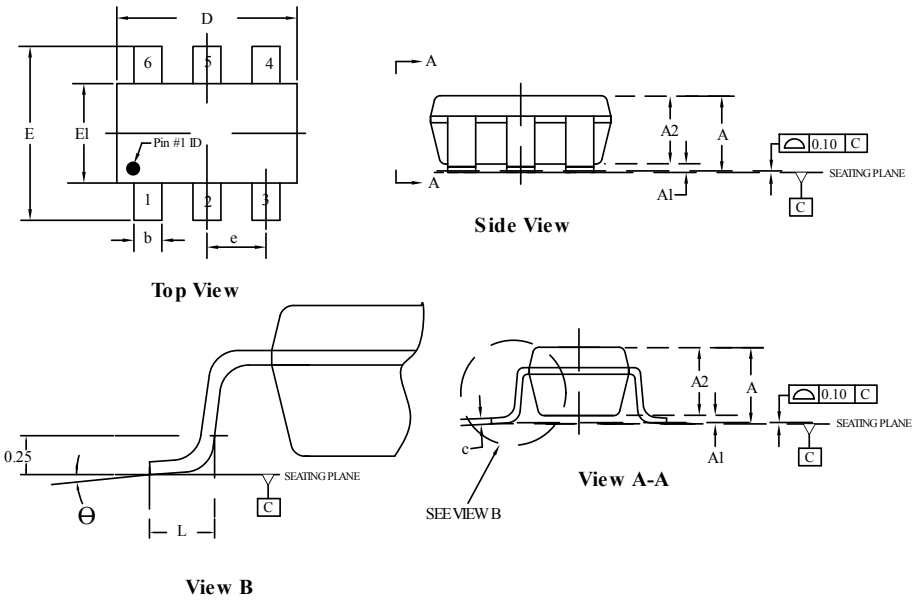
Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API’s to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/technologies/touch/. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

5. Packaging Information

5.1. 6ST1

Figure 5-1. 6ST1



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.45	
A1	0	–	0.15	
A2	0.90	–	1.30	
D	2.80	2.90	3.00	2
E	2.60	2.80	3.00	
E1	1.50	1.60	1.75	
L	0.30	0.45	0.55	
e	0.95 BSC			
b	0.30	–	0.50	3
c	0.09	–	0.20	
θ	0°	–	8°	

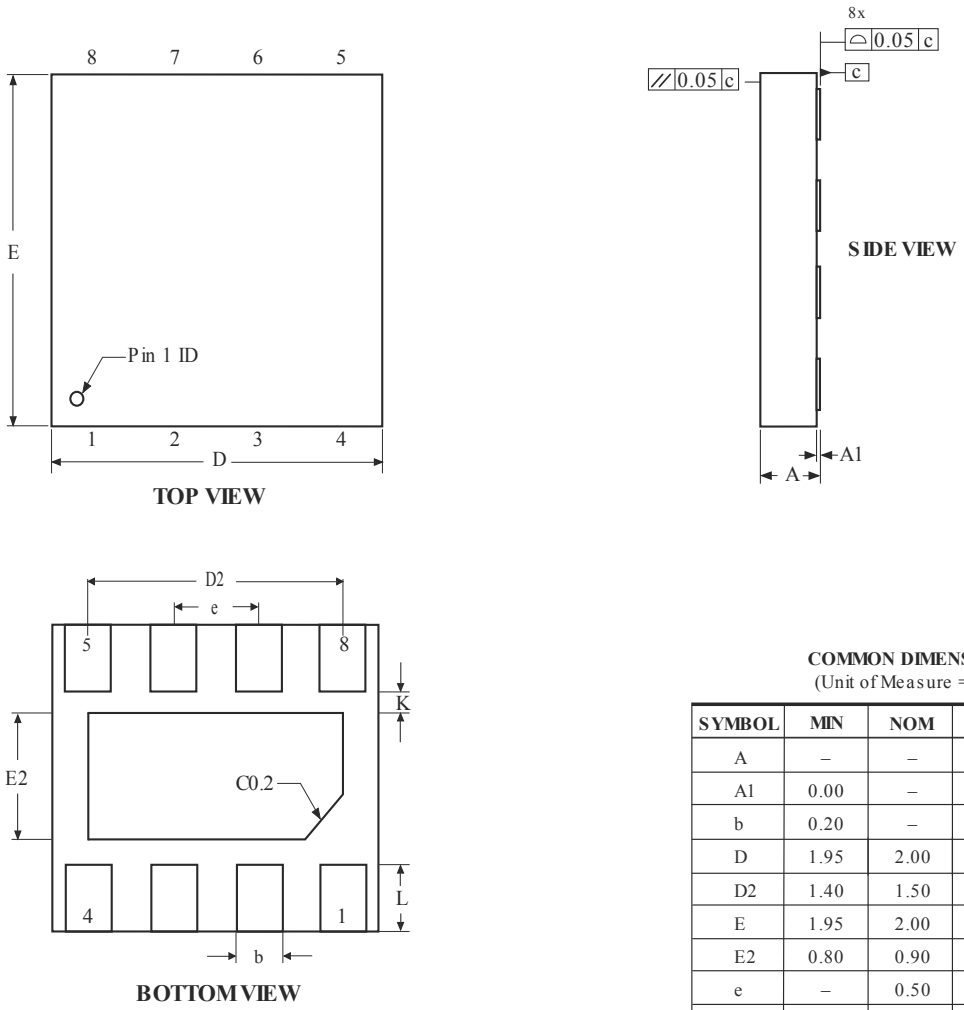
Notes:
1. This package is compliant with JEDEC specification MO-178 Variation AB
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrustion or gate burrs shall not exceed 0.25 mm per end.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm
4. Die is facing down after trim/form.

6/30/08

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE **6ST1,** 6-lead, 2.90 x 1.60 mm Plastic Small Outline Package (SOT23)	GPC TAQ	DRAWING NO. 6ST1	REV. A

5.2. 8MA4

Figure 5-2. 8MA4



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.60	
A1	0.00	–	0.05	
b	0.20	–	0.30	
D	1.95	2.00	2.05	
D2	1.40	1.50	1.60	
E	1.95	2.00	2.05	
E2	0.80	0.90	1.00	
e	–	0.50	–	
L	0.20	0.30	0.40	
K	0.20	–	–	

Note:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. REFER JEDEC MO-236/MO-252

12/17/09

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	8PAD, 2x2x0.6 mm body, 0.5 mm pitch, 0.9x1.5 mm exposed pad, Saw singulated Thermally enhanced plastic ultra thin dual flat no lead package (UDFN/USON)	YAG	8MA4	A

6. Errata

6.1. ATtiny4

6.1.1. Rev. E

• Programming Lock Bits

1. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.1.2. Rev. D

• ESD HBM (ESD STM 5.1) level ±1000V

• Programming Lock Bits

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.1.3. Rev. A – C

Not sampled.

6.2. ATtiny5

6.2.1. Rev. E

• Programming Lock Bits

1. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.2.2. Rev. D

• ESD HBM (ESD STM 5.1) level ±1000V

• Programming Lock Bits

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.2.3. Rev. A – C

Not sampled.

6.3. ATtiny9

6.3.1. Rev. E

• Programming Lock Bits

1. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.3.2. Rev. D

• ESD HBM (ESD STM 5.1) level ±1000V

• Programming Lock Bits

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.3.3. Rev. A – C

Not sampled.

6.4. ATtiny10

6.4.1. Rev. E

• Programming Lock Bits

1. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.4.2. Rev. C – D

• ESD HBM (ESD STM 5.1) level ±1000V

• Programming Lock Bits

1. ESD HBM (ESD STM 5.1) level ±1000V

The device meets ESD HBM (ESD STM 5.1) level ±1000V.

Problem Fix / Workaround

Always use proper ESD protection measures (Class 1C) when handling integrated circuits before and during assembly.

2. Programming Lock Bits

Programming Lock Bits to a lock mode equal or lower than the current causes one word of Flash to be corrupted. The location of the corruption is random.

Problem Fix / Workaround

When programming Lock Bits, make sure lock mode is not set to present, or lower levels.

6.4.3. Rev. A – B

Not sampled.

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