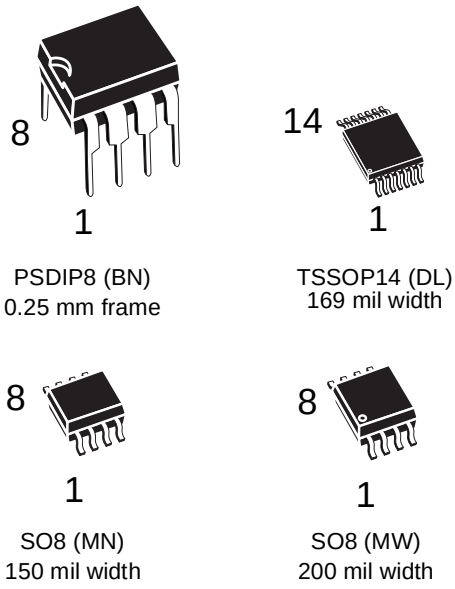
M95256
M95128

256/128 Kbit Serial SPI Bus EEPROM With High Speed Clock

PRELIMINARY DATA

- SPI Bus Compatible Serial Interface
- Supports Positive Clock SPI Modes
- 5 MHz Clock Rate (maximum)
- Single Supply Voltage:
  - 4.5V to 5.5V for M95xxx
  - 2.7V to 3.6V for M95xxx-V
  - 2.5V to 5.5V for M95xxx-W
  - 1.8V to 3.6V for M95xxx-R
- Status Register
- Hardware and Software Protection of the Status Register
- BYTE and PAGE WRITE (up to 64 Bytes)
- Self-Timed Programming Cycle
- Resizeable Read-Only EEPROM Area
- Enhanced ESD Protection
- 100,000 Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



DESCRIPTION

These SPI-compatible electrically erasable programmable memory (EEPROM) devices are organized as 32K x 8 bits (M95256) and 16K x 8 bits (M95128), and operate down to 2.7 V (for the

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

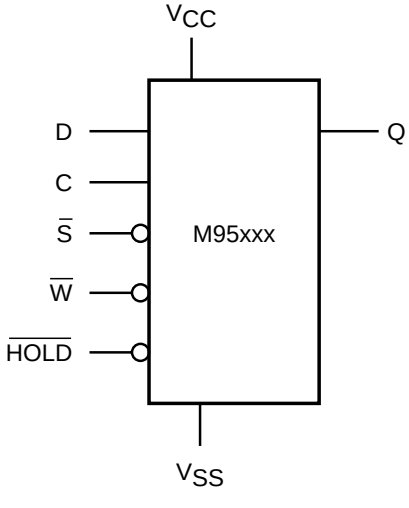


Figure 2A. DIP Connections

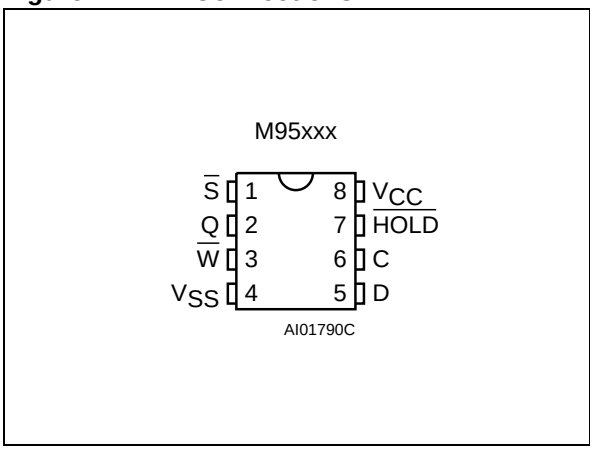
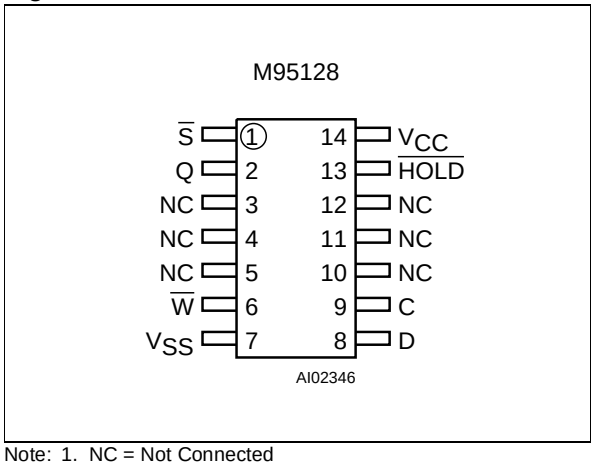
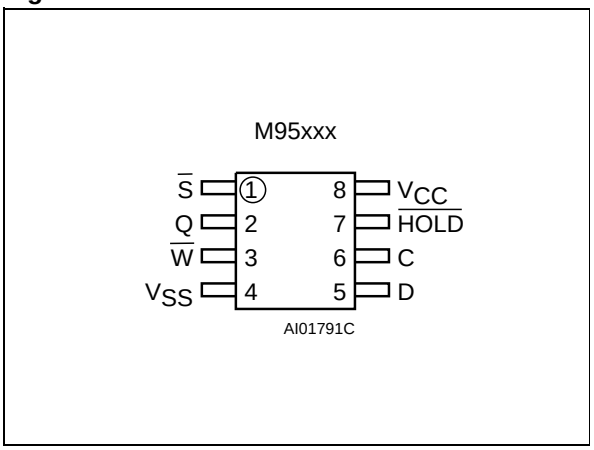


Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2B. SO Connections



-V version), 2.5 V (for the -W version), and down to 1.8 V (for the -R version of each device).

The M95256 and M95128 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Each memory device is accessed by a simple serial interface that is SPI bus compatible. The bus signals are C, D and Q, as shown in Table 1 and Figure 3.

The device is selected when the chip select input ($\overline{S}$) is held low. Communications with the chip can be interrupted using the hold input ($\overline{HOLD}$).

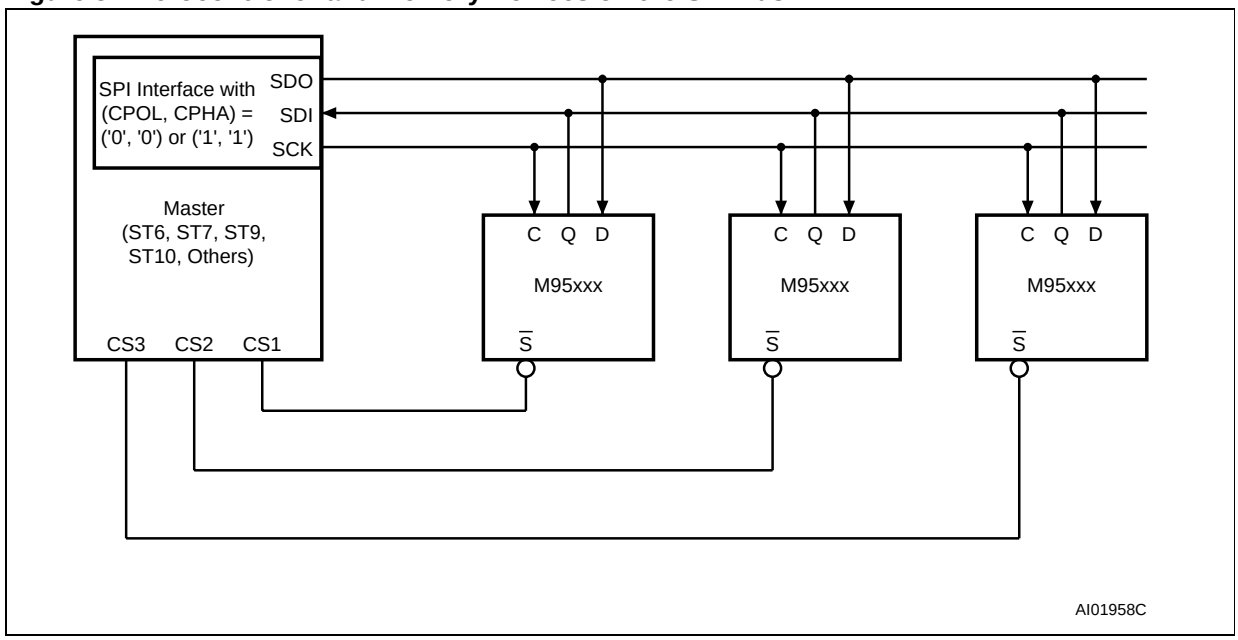
Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c.	°C
V_O	Output Voltage Range		-0.3 to V_{CC}+0.6	V
V_I	Input Voltage Range		-0.3 to 6.5	V
V_{CC}	Supply Voltage Range		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.

2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

Figure 3. Microcontroller and Memory Devices on the SPI Bus



SIGNAL DESCRIPTION

Serial Output (Q)

The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D)

The input pin is used to transfer data serially into the device. Instructions, addresses, and the data to be written, are each received this way. Input is latched on the rising edge of the serial clock.

Serial Clock (C)

The serial clock provides the timing for the serial interface (as shown in Figure 4). Instructions, addresses, or data are latched, from the input pin, on the rising edge of the clock input. The output data on the Q pin changes state after the falling edge of the clock input.

Chip Select ($\overline{S}$)

When $\overline{S}$ is high, the memory device is deselected, and the Q output pin is held in its high impedance state. Unless an internal write operation is underway, the memory device is placed in its stand-by power mode.

After power-on, a high-to-low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$)

The protection features of the memory device are summarized in Table 3.

The hardware write protection, controlled by the $\overline{W}$ pin, restricts write access to the Status Register (though not to the WIP and WEL bits, which are set or reset by the device internal logic).

Bit 7 of the status register (as shown in Table 5) is the Status Register Write Disable bit (SRWD). When this is set to 0 (its initial delivery state) it is possible to write to the status register if the WEL bit (Write Enable Latch) has been set by the WREN instruction (irrespective of the level being applied to the $\overline{W}$ input).

When bit 7 (SRWD) of the status register is set to 1, the ability to write to the status register depends on the logic level being presented at pin $\overline{W}$:

– If $\overline{W}$ pin is high, it is possible to write to the status register, after having set the WEL bit using the WREN instruction (Write Enable Latch).

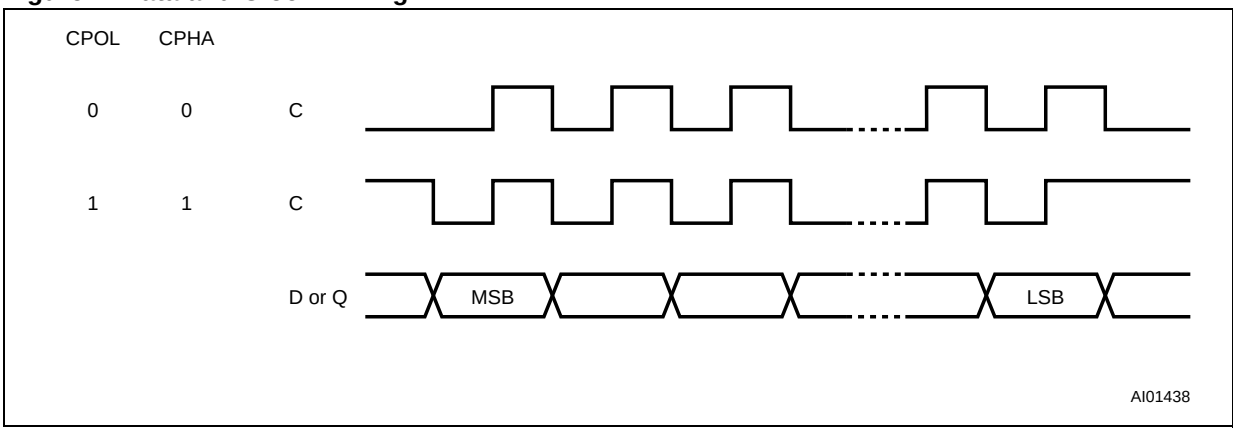
– If $\overline{W}$ pin is low, any attempt to modify the status register is ignored by the device, even if the WEL bit has been set. As a consequence, all the data bytes in the EEPROM area, protected by the BPn bits of the status register, are also hardware protected against data corruption, and appear as a Read Only EEPROM area for the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) either by setting the SRWD bit after pulling low the $\overline{W}$ pin, or by pulling low the $\overline{W}$ pin after setting the SRWD bit.

The only way to abort the Hardware Protected Mode, once entered, is to pull high the $\overline{W}$ pin.

If $\overline{W}$ pin is permanently tied to the high level, the Hardware Protected Mode is never activated, and

Figure 4. Data and Clock Timing



the memory device only allows the user to protect a part of the memory, using the BPn bits of the status register, in the Software Protected Mode (SPM).

Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used to pause the serial communications between the SPI memory and controller, without losing bits that have already been decoded in the serial sequence. For a hold condition to occur, the memory device must already have been selected ($\overline{S}$ = 0). The hold condition starts when the $\overline{\text{HOLD}}$ pin is held low while the clock pin (C) is also low (as shown in Figure 5).

During the hold condition, the Q output pin is held in its high impedance state, and the levels on the input pins (D and C) are ignored by the memory device.

It is possible to deselect the device when it is still in the hold state, thereby resetting whatever transfer had been in progress. The memory remains in the hold state as long as the $\overline{\text{HOLD}}$ pin is low. To restart communication with the device, it is necessary both to remove the hold condition (by taking $\overline{\text{HOLD}}$ high) and to select the memory (by taking $\overline{S}$ low).

OPERATIONS

All instructions, addresses and data are shifted serially in and out of the chip. The most significant bit is presented first, with the data input (D) sampled on the first rising edge of the clock (C) after the chip select ($\overline{S}$) goes low.

Every instruction starts with a single-byte code, as summarized in Table 4. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ held low). If an invalid instruction is sent (one not contained in Table 4), the chip automatically deselects itself.

Write Enable (WREN) and Write Disable (WRDI)

The write enable latch, inside the memory device, must be set prior to each WRITE and WRSR operation. The WREN instruction (write enable) sets this latch, and the WRDI instruction (write disable) resets it.

The latch becomes reset by any of the following events:

– Power on
– WRDI instruction completion
– WRSR instruction completion
– WRITE instruction completion.

Table 3. Write Protection Control on the M95256 and M95128

$\overline{\text{W}}$	SRWD Bit	Mode	Status Register	Data Bytes	
				Protected Area	Unprotected Area
0 or 1	0	Software Protected (SPM)	Writeable (if the WREN instruction has set the WEL bit)	Software write protected by the BPn of the status register	Writeable (if the WREN instruction has set the WEL bit)
1	1				
0	1	Hardware Protected (HPM)	Hardware write protected	Hardware write protected by the BPn bits of the status register	Writeable (if the WREN instruction has set the WEL bit)

Figure 5. Hold Condition Activation

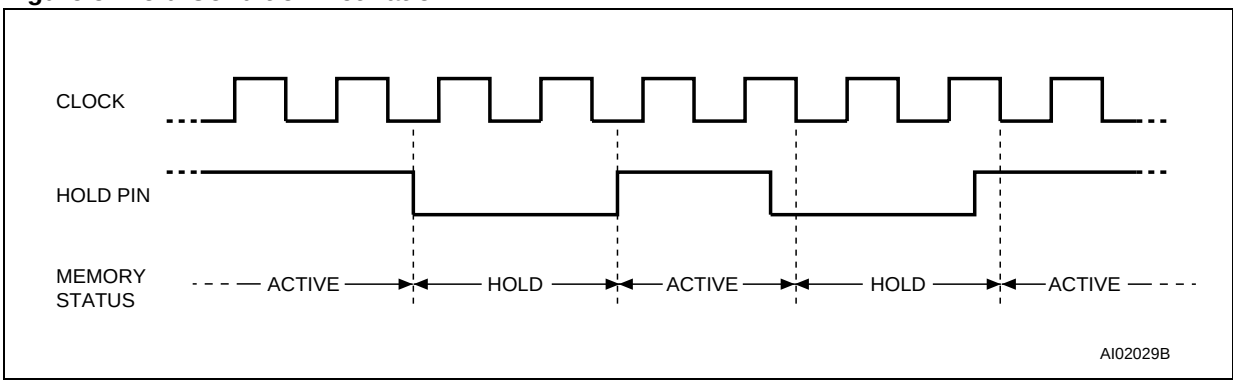
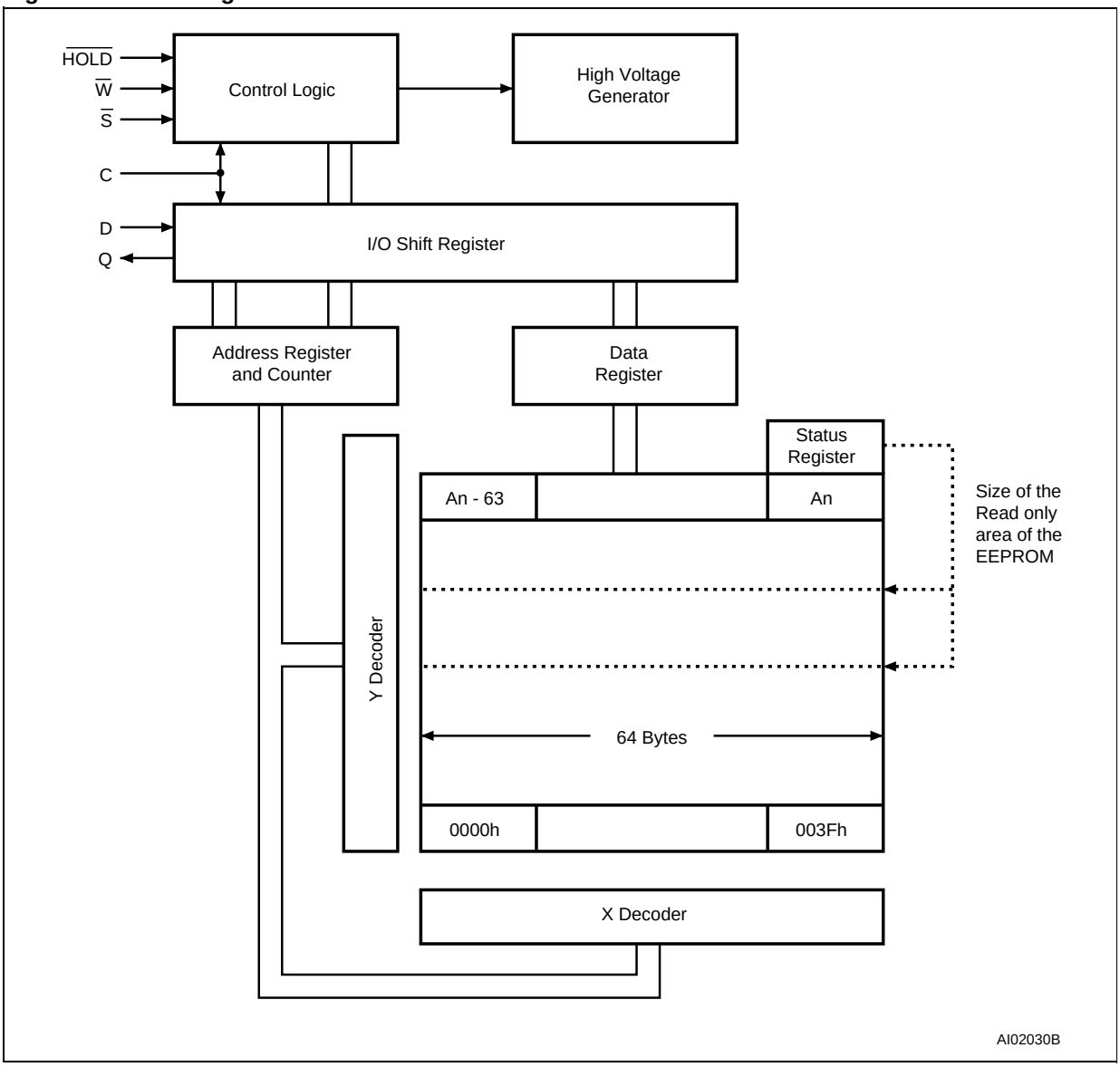


Figure 6. Block Diagram



Note: 1. The cell *An* represents the byte at the highest address in the memory

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Table 5. Status Register Format

b7							b0
SRWD	X	X	X	BP1	BP0	WEL	WIP

Note: 1. SRWD, BP0 and BP1 are Read and write bits.
2. WEL and WIP are Read only bits.

As soon as the WREN or WRDI instruction is received, the memory device first executes the instruction, then enters a wait mode until the device is deselected.

Read Status Register (RDSR)

The RDSR instruction allows the status register to be read, and can be sent at any time, even during a Write operation. Indeed, when a Write is in progress, it is recommended that the value of the Write-In-Progress (WIP) bit be checked. The value in the WIP bit (whose position in the status register is shown in Table 5) can be continuously polled, before sending a new WRITE instruction, using the timing shown in Figure 7. The Write-In-Process (WIP) bit is read-only, and indicates whether the memory is busy with a Write operation. A '1' indicates that a write is in progress, and a '0' that no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. It, too, is read-only. Its value can only be changed by one of the events listed in the previous paragraph, or as a result of executing WREN or WRDI instruction. It cannot be changed using a WRSR instruction. A '1' indicates that the latch is set (the forthcoming Write instruction will be executed), and a '0' that it is reset (and any forthcoming Write instructions will be ignored).

The Block Protect (BP0 and BP1) bits indicate the amount of the memory that is to be write-protected. These two bits are non-volatile. They are set using a WRSR instruction.

During a Write operation (whether it be to the memory area or to the status register), all bits of the status register remain valid, and can be read using the RDSR instruction. However, during a Write operation, the values of the non-volatile bits (SRWD, BP0, BP1) become frozen at a constant value. The updated value of these bits becomes available when a new RDSR instruction is executed, after completion of the write cycle. On the other hand, the two read-only bits (WEL, WIP) are dynamically updated during internal write cycles. Using this facility, it is possible to poll the WIP bit to detect the end of the internal write cycle.

Write Status Register (WRSR)

The format of the WRSR instruction is shown in Figure 8. After the instruction and the eight bits of the status register have been latched-in, the internal Write cycle is triggered by the rising edge of the $\overline{S}$ line. This must occur before the rising edge of the 17th clock pulse (as indicated in Figure 14), otherwise the internal write sequence is not performed.

The WRSR instruction is used for the following:

- to select the size of memory area that is to be write-protected
- to select between SPM (Software Protected Mode) and HPM (Hardware Protected Mode).

Figure 7. RDSR: Read Status Register Sequence

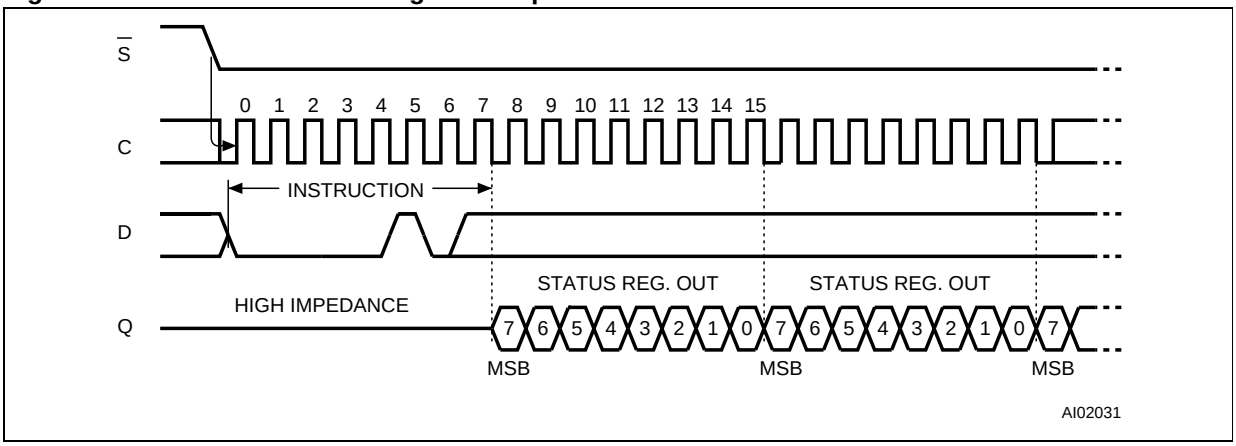


Table 6. Write Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected	
BP1	BP0		M95256	M95128
0	0	none	none	none
0	1	Upper quarter	6000h - 7FFFh	3000h - 3FFFh
1	0	Upper half	4000h - 7FFFh	2000h - 3FFFh
1	1	Whole memory	0000h - 7FFFh	0000h - 3FFFh

The size of the write-protection area applies equally in SPM and HPM. The BP1 and BP0 bits of the status register have the appropriate value (see Table 6) written into them after the contents of the protected area of the EEPROM have been written.

The initial delivery state of the BP1 and BP0 bits is 00, indicating a write-protection size of 0.

Software Protected Mode (SPM)

The act of writing a non-zero value to the BP1 and BP0 bits causes the Software Protected Mode (SPM) to be started. All attempts to write a byte or page in the protected area are ignored, even if the Write Enable Latch is set. However, writing is still allowed in the unprotected area of the memory array and to the SRWD, BP1 and BP0 bits of the status register, provided that the WEL bit is first set.

Hardware Protected Mode (HPM)

The Hardware Protected Mode (HPM) offers a higher level of protection, and can be selected by setting the SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting the SRWD bit. The SRWD is set by the WSR instruction, provided that the WEL bit is first set. The setting of the SRWD bit can be made independently of, or at the same time as, writing a new value to the BP1 and BP0 bits.

Once the device is in the Hardware Protected Mode, the data bytes in the protected area of the memory array, *and* the content of the status register, are write-protected. The only way to re-enable writing new values to the status register is to pull the $\overline{W}$ pin high. This cause the device to leave the Hardware Protected Mode, and to revert to being in the Software Protected Mode. (The value in the BP1 and BP0 bits will not have been changed).

Further details of the operation of the Write Protect pin ($\overline{W}$) is given earlier, on page 3.

Typical Use of HPM and SPM

The $\overline{W}$ pin can be dynamically driven by an output port of a microcontroller. It is also possible, though, to connect it permanently to V_{SS} (by a solder connection, or through a pull-down resistor). The manufacturer of such a printed circuit board can take the memory device, still in its initial delivery state, and can solder it directly on to the board. After power on, the microcontroller can be instructed to write the protected data into the

Figure 8. WRSR: Write Status Register Sequence

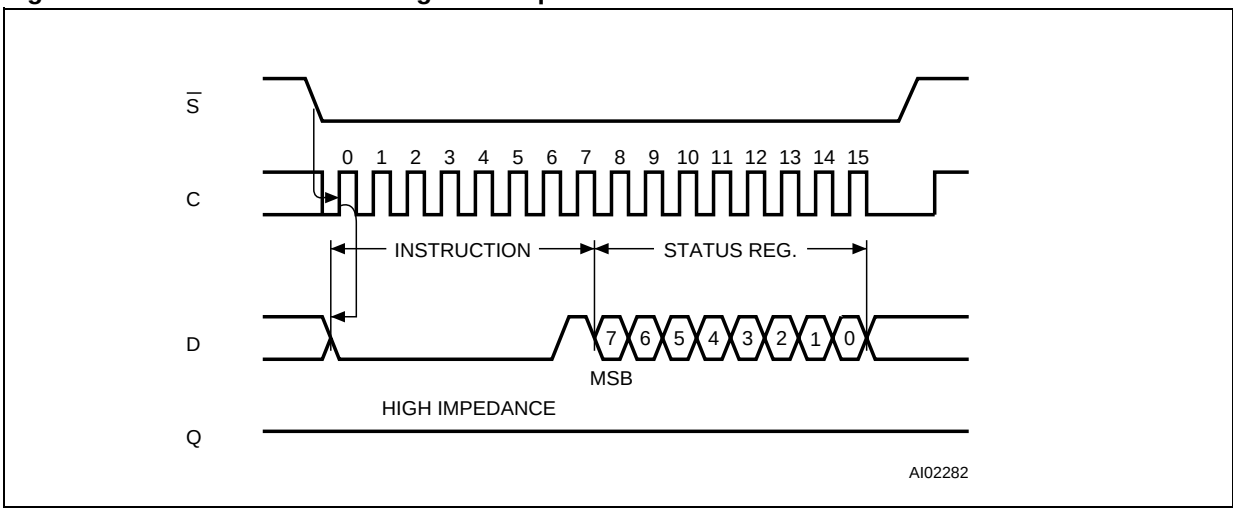
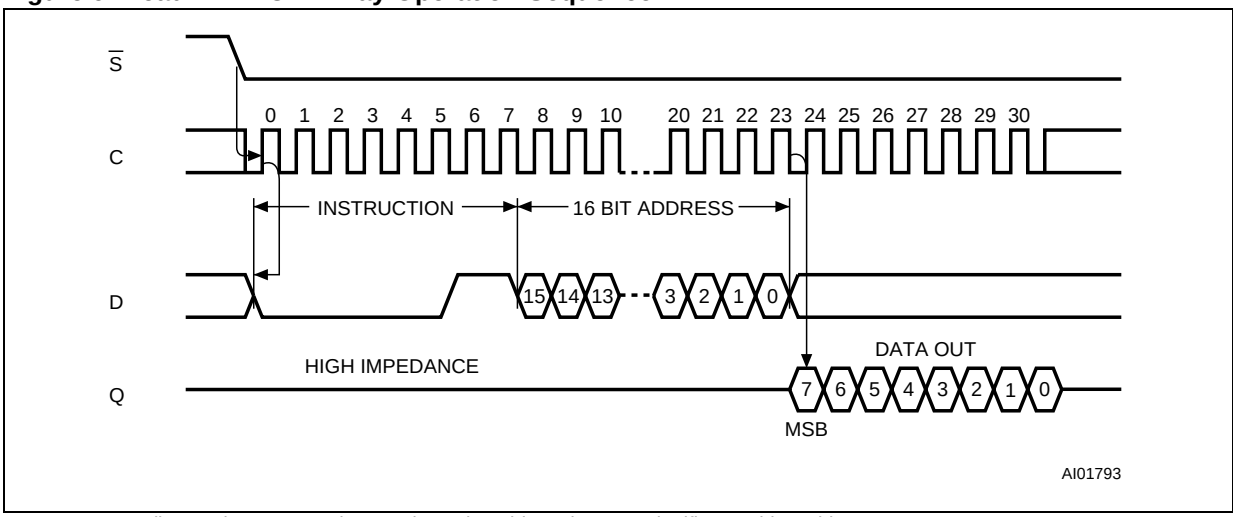


Figure 9. Read EEPROM Array Operation Sequence



Note: 1. Depending on the memory size, as shown in Table 7, the most significant address bits are Don't Care.

Table 7. Address Range Bits

Device	M95256	M95128
Address Bits	A14-A0	A13-A0

Note: 1. b15 is Don't Care on the M95256 series.
b15 and b14 are Don't Care on the M95128 series.

appropriate area of the memory. When it has finished, the appropriate values are written to the BP1, BP0 and SRWD bits, thereby putting the device in the hardware protected mode.

An alternative method is to write the protected data, and to set the BP1, BP0 and SRWD bits, before soldering the memory device to the board. Again, this results in the memory device being placed in its hardware protected mode.

If the $\overline{W}$ pin has been connected to V_{SS} by a pull-down resistor, the memory device can be taken out of the hardware protected mode by driving the $\overline{W}$ pin high, to override the pull-down resistor.

If the $\overline{W}$ pin has been directly soldered to V_{SS}, there is only one way of taking the memory device out of the hardware protected mode: the memory device must be de-soldered from the board, and connected to external equipment in which the $\overline{W}$ pin is allowed to be taken high.

Read Operation

The chip is first selected by holding $\overline{S}$ low. The serial one byte read instruction is followed by a two byte address (A15-A0), each bit being latched-in during the rising edge of the clock (C).

The data stored in the memory, at the selected address, is shifted out on the Q output pin. Each bit is shifted out during the falling edge of the clock (C) as shown in Figure 9. The internal address counter is automatically incremented to the next higher address after each byte of data has been shifted out. The data stored in the memory, at the

Figure 10. Write Enable Latch Sequence

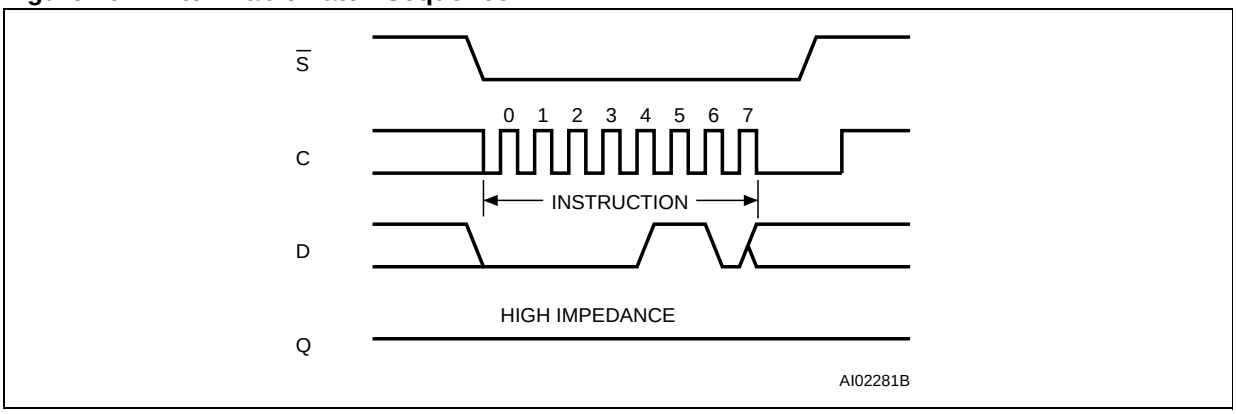
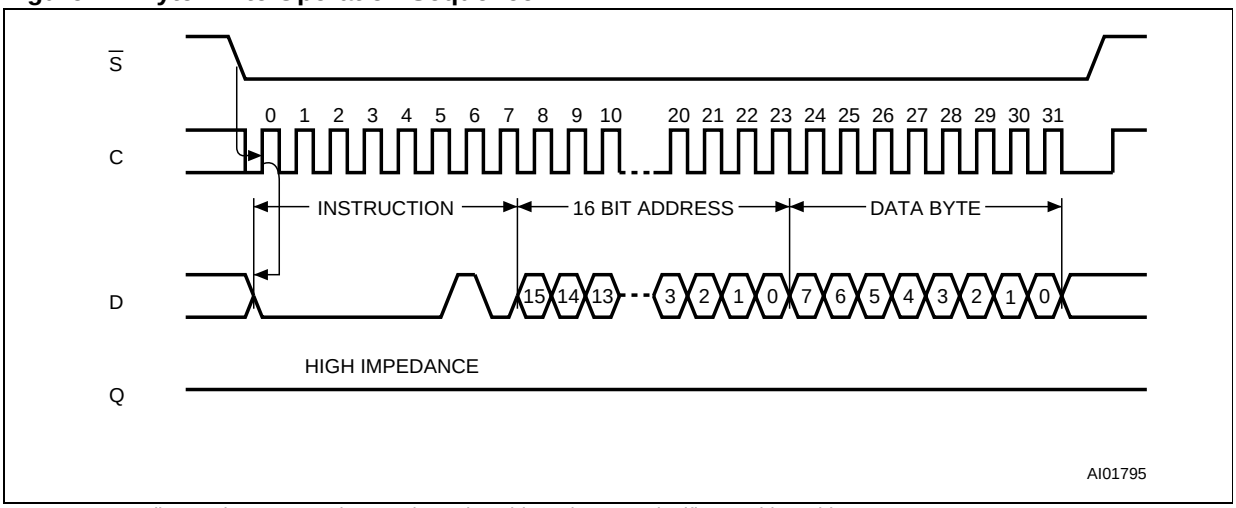


Figure 11. Byte Write Operation Sequence



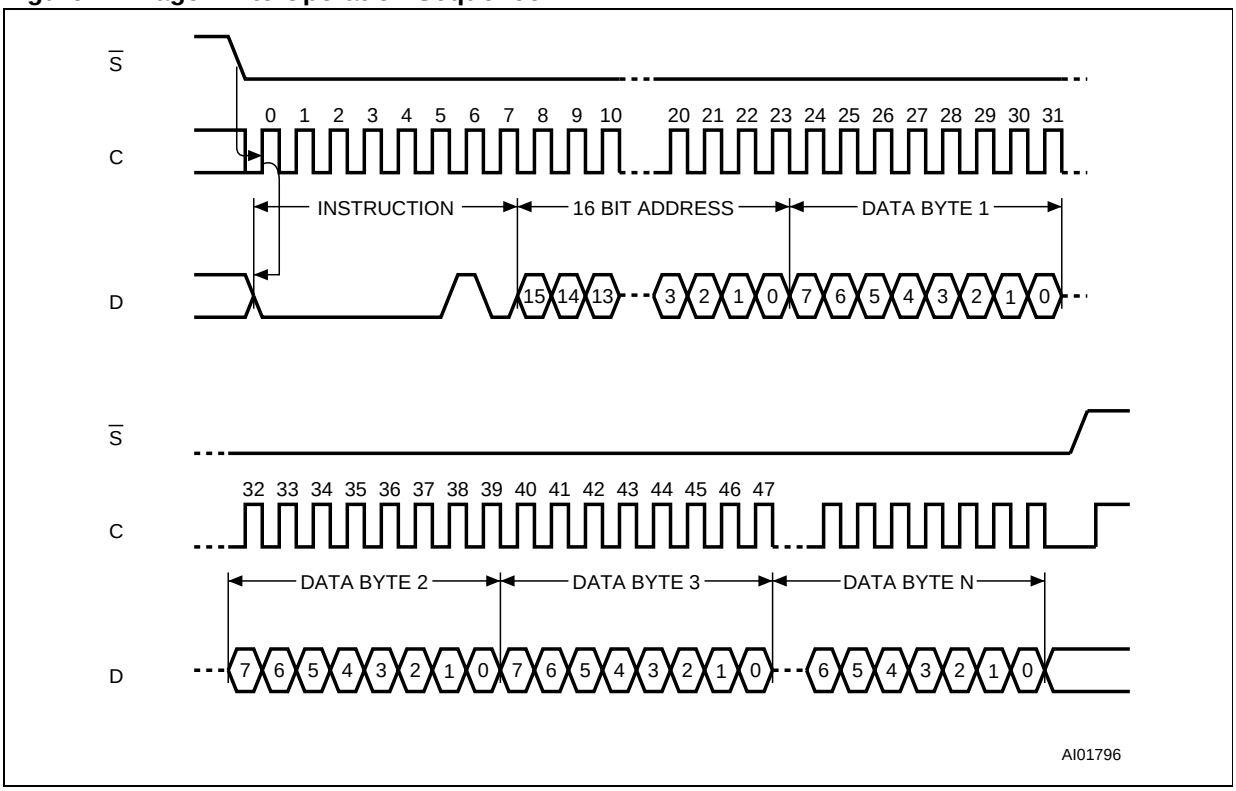
Note: 1. Depending on the memory size, as shown in Table 7, the most significant address bits are Don't Care.

next address, can be read by successive clock pulses. When the highest address is reached, the address counter rolls over to "0000h", allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. If a read instruction is received during a write cycle, it is rejected, and the memory device deselects itself.

Byte Write Operation

Before any write can take place, the WEL bit must be set, using the WREN instruction. The write state is entered by selecting the chip, issuing three

Figure 12. Page Write Operation Sequence



Note: 1. Depending on the memory size, as shown in Table 7, the most significant address bits are Don't Care.

bytes of instruction and address, and one byte of data. Chip Select ($\overline{S}$) must remain low throughout the operation, as shown in Figure 11. The product must be deselected just after the eighth bit of the data byte has been latched in, otherwise the write process is cancelled. As soon as the memory device is deselected, the self-timed internal write cycle is initiated. While the write is in progress, the status register may be read to check the status of the SRWD, BP1, BP0, WEL and WIP bits. In particular, WIP contains a '1' during the self-timed write cycle, and a '0' when the cycle is complete, (at which point the write enable latch is also reset).

Page Write Operation

A maximum of 64 bytes of data can be written during one Write time, t_W, provided that they are all to the same page (see Figure 6). The Page Write operation is the same as the Byte Write operation, except that instead of deselecting the device after the first byte of data, up to 63 additional bytes can be shifted in (and then the device is deselected after the last byte).

Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (an address of the form xxxx xx11 1111) and the clock continues, the counter rolls over to the first address of the same page (xxxx xx00 0000) and over-writes any previously written data.

As before, the Write cycle only starts if the $\overline{S}$ transition occurs just after the eighth bit of the last data byte has been received, as shown in Figure 12.

Table 8. Initial Status Register Format

b7							b0
0	0	0	0	0	0	0	0

Table 9. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100 pF

Note: 1. Output Hi-Z is defined as the point where data is no longer driven.

DATA PROTECTION AND PROTOCOL SAFETY

To protect the data in the memory from inadvertent corruption, the memory device only responds to correctly formulated commands. The main security measures can be summarized as follows:

– The WEL bit is reset at power-up.
– $\overline{S}$ must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile write cycle (in the memory array or in the status register).
– Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
– After execution of a WREN, WRDI, or RDSR instruction, the chip enters a wait state, and waits to be deselected.
– Invalid $\overline{S}$ and $\overline{HOLD}$ transitions are ignored.

POWER ON STATE

After power-on, the memory device is in the following state:

– low power stand-by state
– deselected (after power-on, a high-to-low transition is required on the $\overline{S}$ input before any operations can be started).
– not in the hold condition
– the WEL bit is reset
– the SRWD, BP1 and BP0 bits of the status register are un-changed from the previous power-down (they are non-volatile bits).

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The status register bits are initialized to 00h, as shown in Table 8.

Figure 13. AC Testing Input Output Waveforms

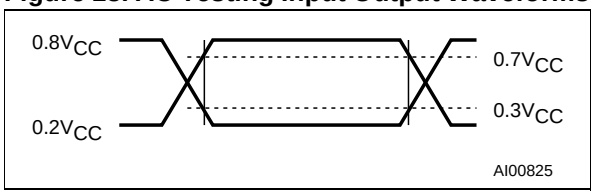


Table 10. Input Parameters[1] (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF

Note: 1. Sampled only, not 100% tested.

Table 11. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 4.5 to 5.5 V)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 2.7 to 3.6 V)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 2.5 to 5.5 V)
(T_A = 0 to 70 °C or –20 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Parameter	Voltage Range	Temp. Range	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	all	all			± 2	µA
I_{LO}	Output Leakage Current	all	all			± 2	µA
I_{CC}	Supply Current	4.5-5.5	6	C = 0.1 V_{CC}/0.9. V_{CC} at 5 MHz, V_{CC} = 5 V, Q = open		4	mA
		4.5-5.5	3	C = 0.1 V_{CC}/0.9. V_{CC} at 2 MHz, V_{CC} = 5 V, Q = open		4	mA
		2.7-3.6	6	C = 0.1 V_{CC}/0.9. V_{CC} at 5 MHz, V_{CC} = 2.7 V, Q = open		3	mA
		2.5-5.5	6	C = 0.1 V_{CC}/0.9. V_{CC} at 2 MHz, V_{CC} = 2.5 V, Q = open		2	mA
		1.8-3.6	5	C = 0.1 V_{CC}/0.9. V_{CC} at 1 MHz, V_{CC} = 1.8 V, Q = open		2	mA
I_{CC1}	Supply Current (Stand-by)	4.5-5.5	6	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5 V		10	µA
		4.5-5.5	3	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5 V		20	µA
		2.7-3.6	6	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 2.7 V		2	µA
		2.5-5.5	6	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 2.5 V		2	µA
		1.8-3.6	5	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} , V_{CC} = 1.8 V		1	µA
V_{IL}	Input Low Voltage	all	all		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage	all	all		0.7 V_{CC}	V_{CC}+1	V
V_{OL}[1]	Output Low Voltage	4.5-5.5	6	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
		4.5-5.5	3	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
		2.7-3.6	6	I_{OL} = 1.5 mA, V_{CC} = 2.7 V		0.4	V
		2.5-5.5	6	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
		1.8-3.6	5	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
V_{OH}[1]	Output High Voltage	4.5-5.5	6	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
		4.5-5.5	3	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
		2.7-3.6	6	I_{OH} = –0.4 mA, V_{CC} = 2.7 V	0.8 V_{CC}		V
		2.5-5.5	6	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8 V_{CC}		V
		1.8-3.6	5	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V

Note: 1. For all 5V range devices, the device meets the output requirements for both TTL and CMOS standards.

Table 12A. AC Characteristics

Symbol	Alt.	Parameter	M95256 / M95128				Unit
			V_{CC}=4.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=4.5 to 5.5 V T_A=-40 to 125°C		
			Min	Max	Min	Max	
f_C	f_{SCK}	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		200		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} [1]	t_{CLH}	Clock High Time	90		200		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} [2]	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} [2]	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		140		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		90		ns
t_{CHHL}		Clock High Set-up Time before $\overline{HOLD}$ Active	60		120		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ not Active	60		120		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WC}	Write Time		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 12B. AC Characteristics

Symbol	Alt.	Parameter	M95256-V / M95128-V		M95256-W / M95128-W		M95256-R / M95128-R		Unit
			V_{CC}= 2.7 to 3.6 V T_A=0 to 70°C or –40 to 85°C		V_{CC}= 2.5 to 5.5 V T_A=0 to 70°C or –40 to 85°C		V_{CC}= 1.8 to 3.6 V T_A=0 to 70°C or –20 to 85°C		
			Min	Max	Min	Max	Min	Max	
f_C	f_{SCK}	Clock Frequency	D.C.	5	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ Active Setup Time	90		200		400		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ Not Active Setup Time	90		200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		300		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		400		ns
t_{CH} [1]	t_{CLH}	Clock High Time	90		200		400		ns
t_{CL} [1]	t_{CLL}	Clock Low Time	90		200		400		ns
t_{CLCH} [2]	t_{RC}	Clock Rise Time		0.05		1		1	µs
t_{CHCL} [2]	t_{FC}	Clock Fall Time		0.05		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		100		ns
t_{DLDH} [2]	t_{RI}	Data In Rise Time		0.05		1		1	µs
t_{DHDL} [2]	t_{FI}	Data In Fall Time		0.05		1		1	µs
t_{HHCH}		Clock Low Hold Time after $\overline{HOLD}$ not Active	70		140		350		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active	40		90		200		ns
t_{CHHL}		Clock High Set-up Time before $\overline{HOLD}$ Active	60		120		250		ns
t_{CHHH}		Clock High Set-up Time before $\overline{HOLD}$ not Active	60		120		250		ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		100		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		0		ns
t_{QLQH} [2]	t_{RO}	Output Rise Time		50		100		200	ns
t_{QHQL} [2]	t_{FO}	Output Fall Time		50		100		200	ns
t_{HHQX} [2]	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100		250	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250		500	ns
t_W	t_{WC}	Write Time		10		10		10	ms

Note: 1. $t_{CH} + t_{CL} \geq 1 / f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Figure 14. Serial Input Timing

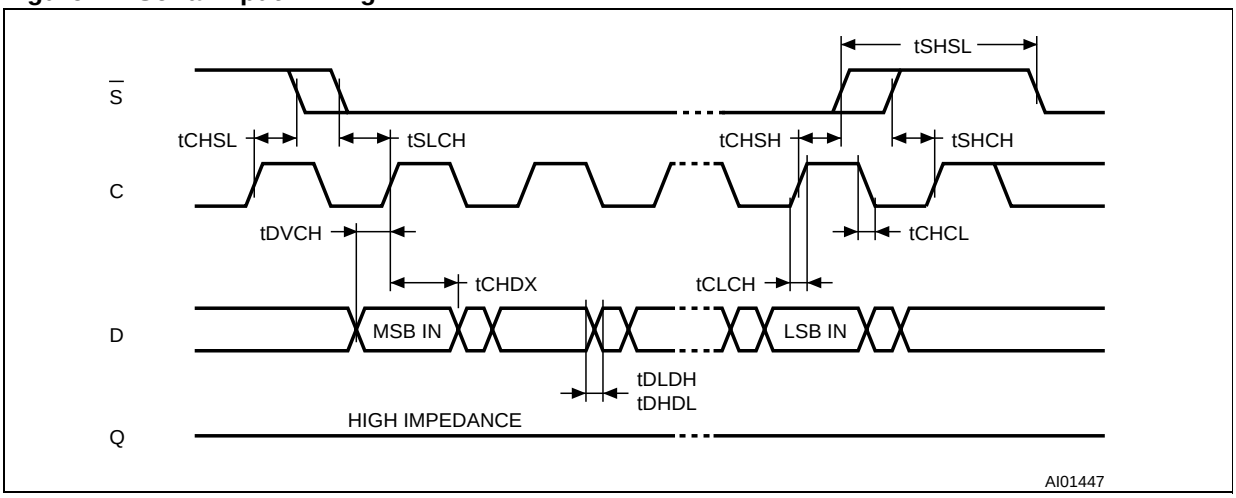


Figure 15. Hold Timing

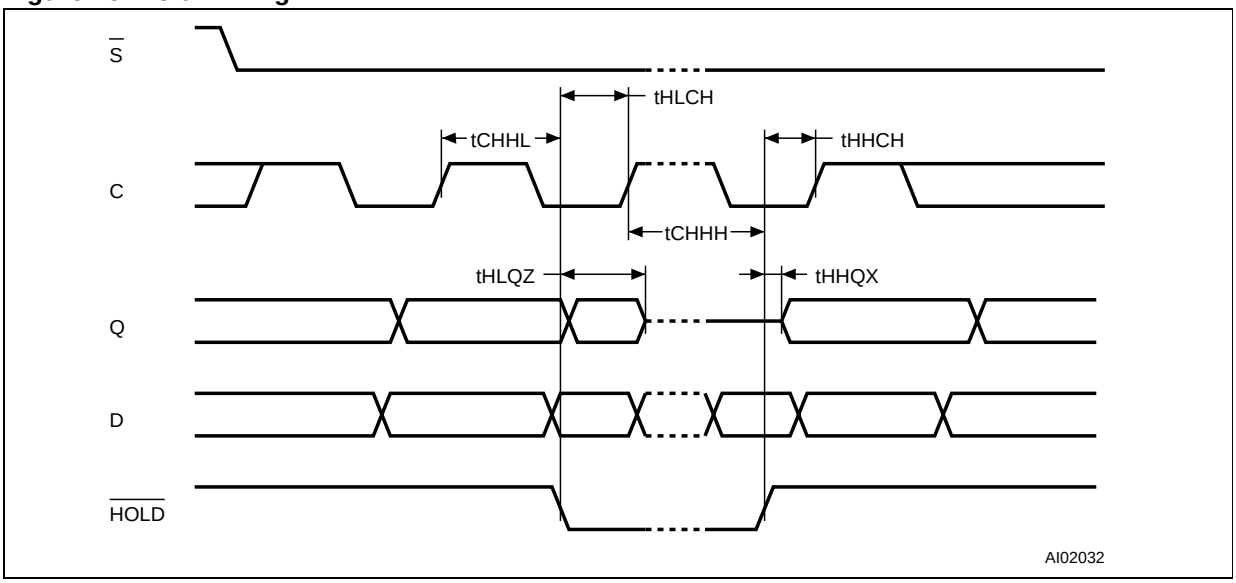


Figure 16. Output Timing

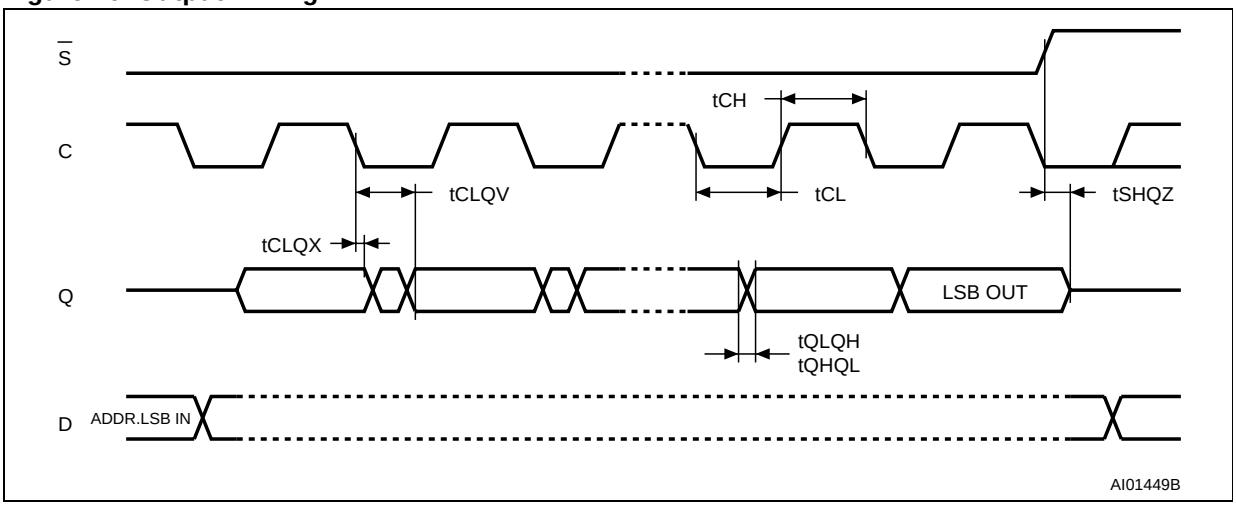


Table 13. Ordering Information Scheme

Example: M95256 – R MW 6 T

Memory Capacity

256	256 Kbit (32K x 8)
128	128 Kbit (16K x 8)

Operating Voltage

blank	4.5 V to 5.5 V
V	2.7 V to 3.6 V
W	2.5 V to 5.5 V
R[3]	1.8 V to 3.6 V

Temperature Range

1[1]	0 °C to 70 °C
5	–20 °C to 85 °C
6	–40 °C to 85 °C
3[2]	–40 °C to 125 °C

Package

BN	PSDIP8 (0.25 mm frame)
MW	SO8 (200 mil width)
MN[4]	SO8 (150 mil width)
DL[5]	TSSOP14 (169 mil width)

Option

T	Tape and Reel Packing

Note: 1. Temperature range available only on request.
2. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5 V to 5.5 V only.
3. The -R version (V_{CC} range 1.8 V to 3.6 V) only available in temperature ranges 5 or 1.
4. SO8, 150 mil width, package is available for the M95128 series only.
5. TSSOP14, 169 mil width, package is available for the M95128 series only.

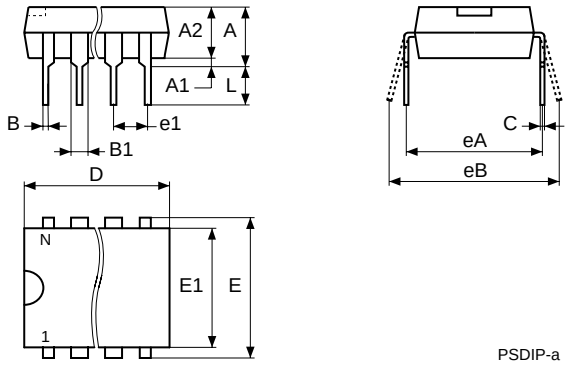
ORDERING INFORMATION

The notation used for the device number is as shown in Table 13. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 14. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 17. PSDIP8 (BN)

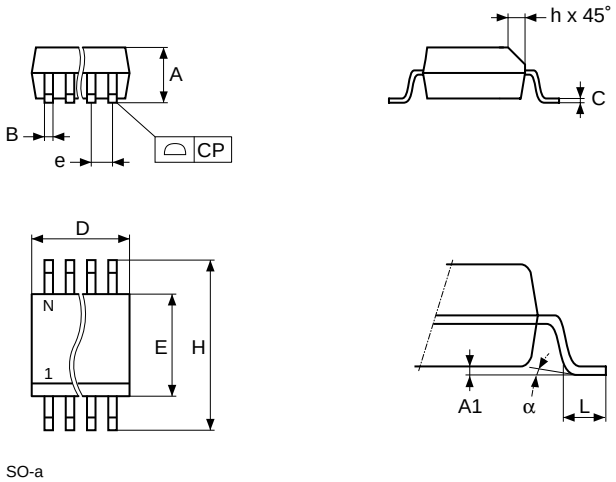


Note: 1. Drawing is not to scale.

Table 15. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 18. SO8 narrow (MN)



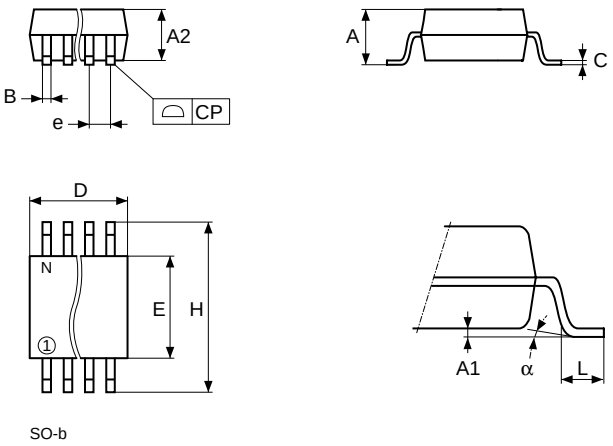
SO-a

Note: 1. Drawing is not to scale.

Table 16. SO8 - 8 lead Plastic Small Outline, 200 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

Figure 19. SO8 wide (MW)

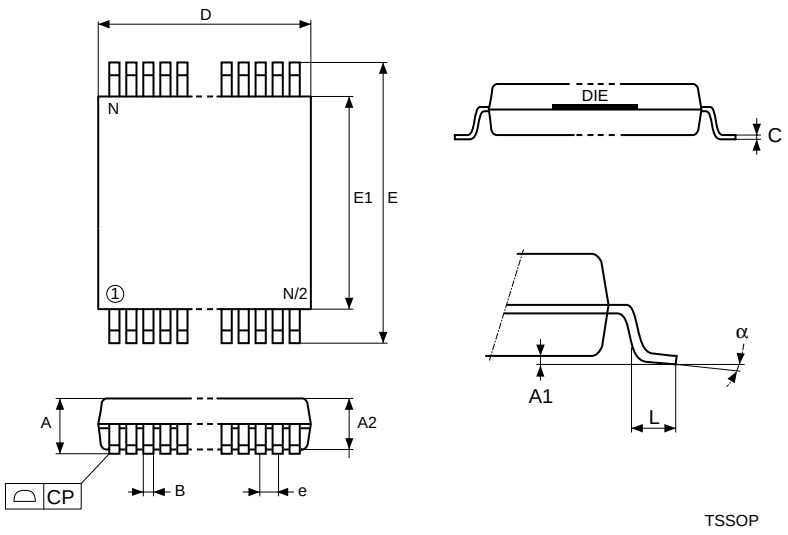


Note: 1. Drawing is not to scale.

Table 17. TSSOP14 - 14 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	14			14		
CP			0.08			0.003

Figure 20. TSSOP14 (DL)



Note: 1. Drawing is not to scale.

Table 18. Revision History

Date	Description of Revision
17-Nov-1999	New -V voltage range added (including the tables for DC characteristics, AC characteristics, and ordering information).
07-Feb-2000	New -V voltage range extended to M95256 (including AC characteristics, and ordering information).
22-Feb-2000	tCLCH and tCHCL, for the M95xxx-V, changed from 1us to 100ns
15-Mar-2000	-V voltage range changed to 2.7-3.6V