

Features

- High Performance, Low Power AVR[®] 8-Bit Microcontroller
- Advanced RISC Architecture
 - 120 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 20 MIPS Throughput at 20 MHz
- High Endurance Non-volatile Memory segments
 - 1K Bytes of In-System Self-programmable Flash program memory
 - 64 Bytes EEPROM
 - 64 Bytes Internal SRAM
 - Write/Erase cycles: 10,000 Flash/100,000 EEPROM
 - Data retention: 20 years at 85°C/100 years at 25°C (see [page 6](#))
 - Programming Lock for Self-Programming Flash & EEPROM Data Security
- Peripheral Features
 - One 8-bit Timer/Counter with Prescaler and Two PWM Channels
 - 4-channel, 10-bit ADC with Internal Voltage Reference
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - On-chip Analog Comparator
- Special Microcontroller Features
 - debugWIRE On-chip Debug System
 - In-System Programmable via SPI Port
 - External and Internal Interrupt Sources
 - Low Power Idle, ADC Noise Reduction, and Power-down Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-out Detection Circuit
 - Internal Calibrated Oscillator
- I/O and Packages
 - 8-pin PDIP/SOIC: Six Programmable I/O Lines
 - 20-pad MLF: Six Programmable I/O Lines
- Operating Voltage:
 - 1.8 - 5.5V for ATtiny13V
 - 2.7 - 5.5V for ATtiny13
- Speed Grade
 - ATtiny13V: 0 - 4 MHz @ 1.8 - 5.5V, 0 - 10 MHz @ 2.7 - 5.5V
 - ATtiny13: 0 - 10 MHz @ 2.7 - 5.5V, 0 - 20 MHz @ 4.5 - 5.5V
- Industrial Temperature Range
- Low Power Consumption
 - Active Mode:
 - 1 MHz, 1.8V: 240 µA
 - Power-down Mode:
 - < 0.1 µA at 1.8V



8-bit AVR[®] Microcontroller with 1K Bytes In-System Programmable Flash

ATtiny13
ATtiny13V

Summary



1. Pin Configurations

Figure 1-1. Pinout ATtiny13/ATtiny13V



NOTE: Bottom pad should be soldered to ground.
 DNC: Do Not Connect



NOTE: Bottom pad should be soldered to ground.
 DNC: Do Not Connect

1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB5:PB0)

Port B is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATTiny13 as listed on [page 54](#).

1.1.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [Table 18-1 on page 115](#). Shorter pulses are not guaranteed to generate a reset.

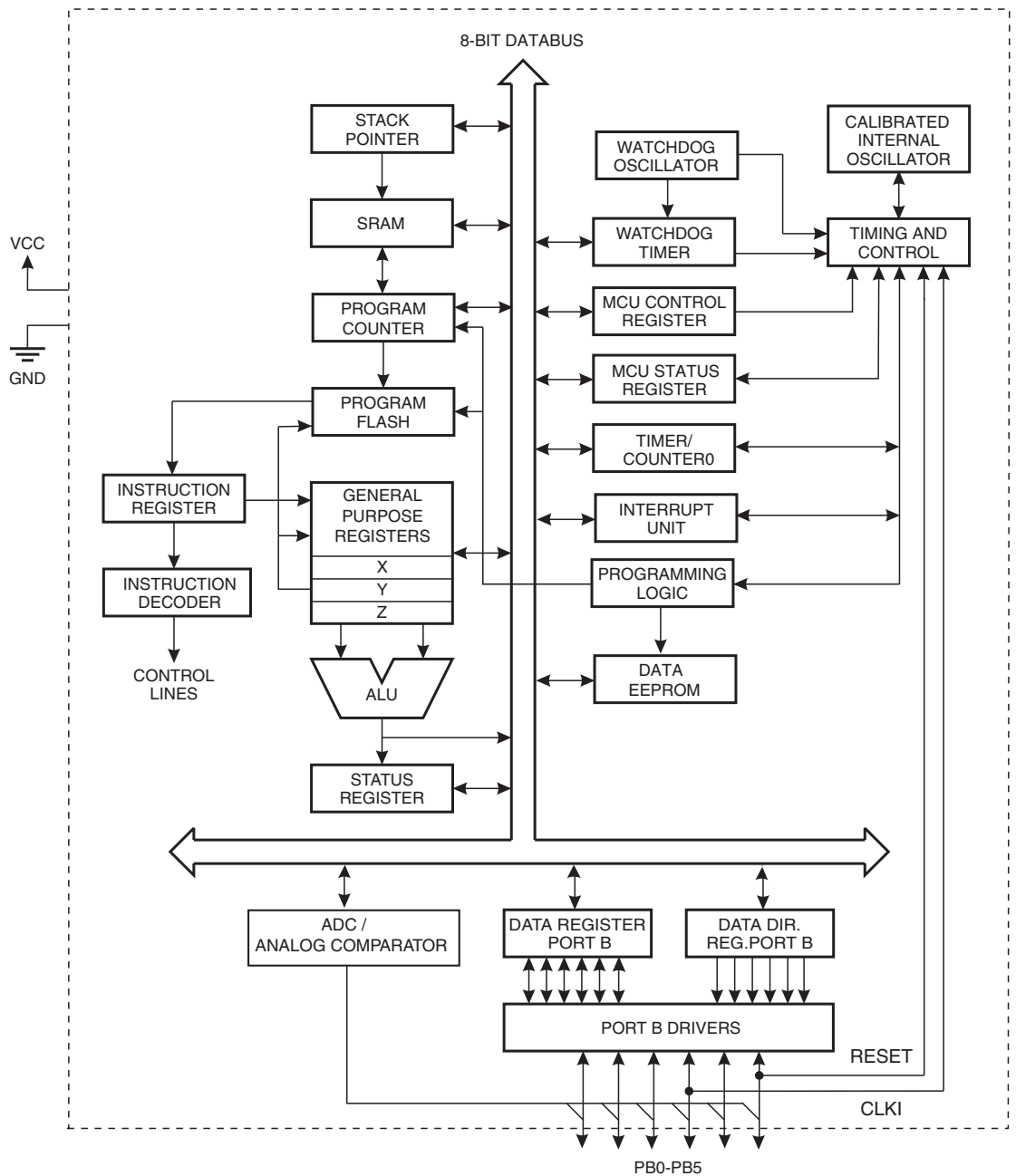
The reset pin can also be used as a (weak) I/O pin.

2. Overview

The ATtiny13 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny13 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATTiny13 provides the following features: 1K byte of In-System Programmable Flash, 64 bytes EEPROM, 64 bytes SRAM, 6 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. The Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATTiny13 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and Evaluation kits.

3. General Information

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|----------|---|--------|-------------------------|--------|--------|--------|--------|---------|------------------|
| 0x3F | SREG | I | T | H | S | V | N | Z | C | page 9 |
| 0x3E | Reserved | – | – | – | – | – | – | – | – | |
| 0x3D | SPL | SPI[7:0] | | | | | | | | page 11 |
| 0x3C | Reserved | – | | | | | | | | |
| 0x3B | GIMSK | – | INT0 | PCIE | – | – | – | – | – | page 46 |
| 0x3A | GIFR | – | INTF0 | PCIF | – | – | – | – | – | page 47 |
| 0x39 | TIMSK0 | – | – | – | – | OCIE0B | OCIE0A | TOIE0 | – | page 74 |
| 0x38 | TIFR0 | – | – | – | – | OCF0B | OCF0A | TOV0 | – | page 75 |
| 0x37 | SPMCSR | – | – | – | CTPB | RFLB | PGWRT | PGERS | SELFPR- | page 97 |
| 0x36 | OCR0A | Timer/Counter – Output Compare Register A | | | | | | | | page 74 |
| 0x35 | MCUCR | – | PUD | SE | SM1 | SM0 | – | ISC01 | ISC00 | page 32 |
| 0x34 | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | page 41 |
| 0x33 | TCCR0B | FOC0A | FOC0B | – | – | WGM02 | CS02 | CS01 | CS00 | page 72 |
| 0x32 | TCNT0 | Timer/Counter (8-bit) | | | | | | | | page 73 |
| 0x31 | OSCCAL | Oscillator Calibration Register | | | | | | | | page 27 |
| 0x30 | Reserved | – | | | | | | | | |
| 0x2F | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | – | – | WGM01 | WGM00 | page 69 |
| 0x2E | DWDR | DWDR[7:0] | | | | | | | | page 96 |
| 0x2D | Reserved | – | | | | | | | | |
| 0x2C | Reserved | – | | | | | | | | |
| 0x2B | Reserved | – | | | | | | | | |
| 0x2A | Reserved | – | | | | | | | | |
| 0x29 | OCR0B | Timer/Counter – Output Compare Register B | | | | | | | | page 74 |
| 0x28 | GTCCR | TSM | – | – | – | – | – | – | PSR10 | page 77 |
| 0x27 | Reserved | – | | | | | | | | |
| 0x26 | CLKPR | CLKPCE | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | page 28 |
| 0x25 | Reserved | – | | | | | | | | |
| 0x24 | Reserved | – | | | | | | | | |
| 0x23 | Reserved | – | | | | | | | | |
| 0x22 | Reserved | – | | | | | | | | |
| 0x21 | WDTCR | WDTIF | WDTIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | page 41 |
| 0x20 | Reserved | – | | | | | | | | |
| 0x1F | Reserved | – | | | | | | | | |
| 0x1E | EEARL | – | – | EEPROM Address Register | | | | | | page 20 |
| 0x1D | EEDR | EEPROM Data Register | | | | | | | | page 20 |
| 0x1C | EECR | – | – | EEP01 | EEP00 | EERIE | EEMPE | EEPE | EERE | page 21 |
| 0x1B | Reserved | – | | | | | | | | |
| 0x1A | Reserved | – | | | | | | | | |
| 0x19 | Reserved | – | | | | | | | | |
| 0x18 | PORTB | – | – | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 56 |
| 0x17 | DDRB | – | – | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | page 56 |
| 0x16 | PINB | – | – | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | page 57 |
| 0x15 | PCMSK | – | – | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | page 47 |
| 0x14 | DIDR0 | – | – | ADC0D | ADC2D | ADC3D | ADC1D | AIN1D | AIN0D | page 80, page 94 |
| 0x13 | Reserved | – | | | | | | | | |
| 0x12 | Reserved | – | | | | | | | | |
| 0x11 | Reserved | – | | | | | | | | |
| 0x10 | Reserved | – | | | | | | | | |
| 0x0F | Reserved | – | | | | | | | | |
| 0x0E | Reserved | – | | | | | | | | |
| 0x0D | Reserved | – | | | | | | | | |
| 0x0C | Reserved | – | | | | | | | | |
| 0x0B | Reserved | – | | | | | | | | |
| 0x0A | Reserved | – | | | | | | | | |
| 0x09 | Reserved | – | | | | | | | | |
| 0x08 | ACSR | ACD | ACBG | ACO | ACI | ACIE | – | ACIS1 | ACIS0 | page 79 |
| 0x07 | ADMUX | – | REFS0 | ADLAR | – | – | – | MUX1 | MUX0 | page 91 |
| 0x06 | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | page 92 |
| 0x05 | ADCH | ADC Data Register High Byte | | | | | | | | page 93 |
| 0x04 | ADCL | ADC Data Register Low Byte | | | | | | | | page 93 |
| 0x03 | ADCSRB | – | ACME | – | – | – | ADTS2 | ADTS1 | ADTS0 | page 94 |
| 0x02 | Reserved | – | | | | | | | | |
| 0x01 | Reserved | – | | | | | | | | |
| 0x00 | Reserved | – | | | | | | | | |



- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|-----------------------------------|----------|--|--|---------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | RdI,K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | RdI,K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \cdot Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \cdot K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | $Rd \leftarrow Rd \cdot (\sim K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \cdot Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | $Rd - Rr$ | Z, N, V, C, H | 1 |
| CPC | Rd,Rr | Compare with Carry | $Rd - Rr - C$ | Z, N, V, C, H | 1 |
| CPI | Rd,K | Compare Register with Immediate | $Rd - K$ | Z, N, V, C, H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRREQ | k | Branch if Equal | if (Z = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if (I = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if (I = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P,b | Set Bit in I/O Register | $I/O(P,b) \leftarrow 1$ | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | $I/O(P,b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|----------------------------|----------|----------------------------------|--|---------|---------|
| ROR | Rd | Rotate Right Through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n=0..6$ | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Twos Complement Overflow | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Twos Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half Carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | $Rd \leftarrow Rr$ | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | $Rd+1:Rd \leftarrow Rr+1:Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-Dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-Dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-Dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-Dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z | Load Program Memory | $Rd \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 3 |
| SPM | | Store Program Memory | $(z) \leftarrow R1:R0$ | None | |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/Timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

6. Ordering Information

| Speed (MHz) ⁽³⁾ | Power Supply (V) | Ordering Code ⁽⁴⁾ | Package ⁽²⁾ | Operation Range |
|----------------------------|------------------|--|---|---|
| 10 | 1.8 - 5.5 | ATtiny13V-10PU ATtiny13V-10SU ATtiny13V-10SUR ATtiny13V-10SSU ATtiny13V-10SSUR ATtiny13V-10MU ATtiny13V-10MUR ATtiny13V-10MMU ATtiny13V-10MMUR | 8P3 8S2 8S2 S8S1 S8S1 20M1 20M1 10M1 10M1 | Industrial (-40°C to +85°C) ⁽¹⁾ |
| 20 | 2.7 - 5.5 | ATtiny13-20PU ATtiny13-20SU ATtiny13-20SUR ATtiny13-20SSU ATtiny13-20SSUR ATtiny13-20MU ATtiny13-20MUR ATtiny13-20MMU ATtiny13-20MMUR | 8P3 8S2 8S2 S8S1 S8S1 20M1 20M1 10M1 10M1 | Industrial (-40°C to +85°C) ⁽¹⁾ |

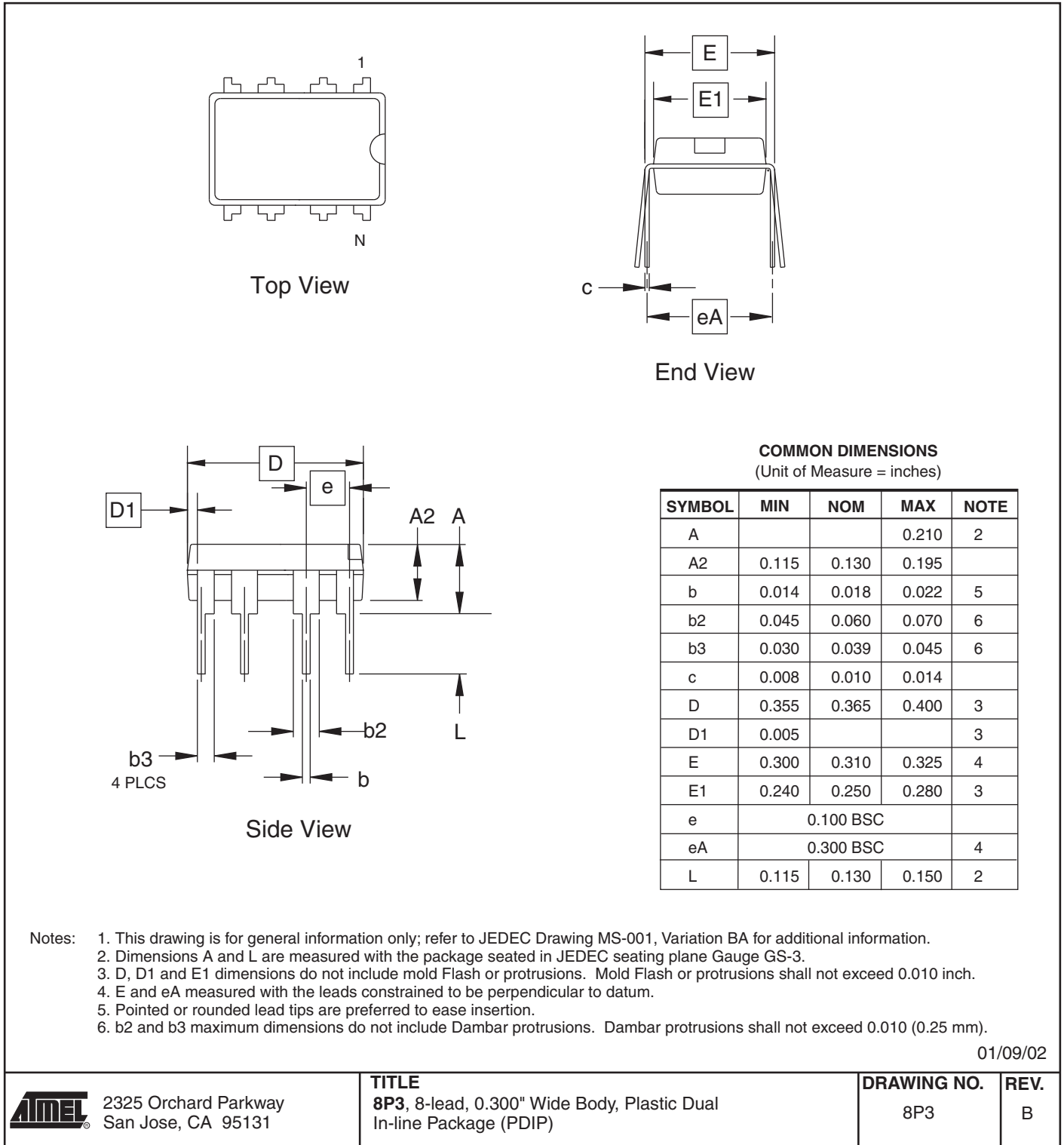
- Notes:
1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
 3. For Speed vs. V_{CC} , see [“Speed Grades” on page 117](#).
 4. Code indicators:
 - U: matte tin
 - R: tape & reel

| Package Type | |
|--------------|---|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S2 | 8-lead, 0.209" Wide, Plastic Small Outline Package (EIAJ SOIC) |
| S8S1 | 8-lead, 0.150" Wide, Plastic Gull-Wing Small Outline (JEDEC SOIC) |
| 20M1 | 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |
| 10M1 | 10-pad, 3 x 3 x 1 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |

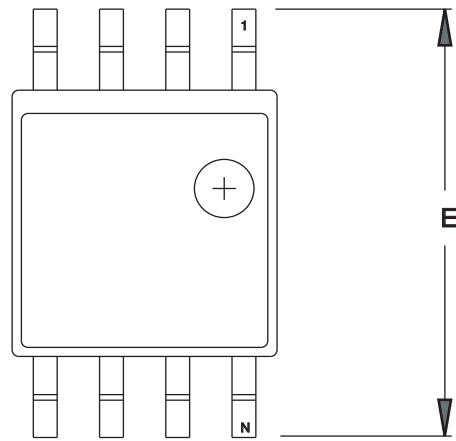


7. Packaging Information

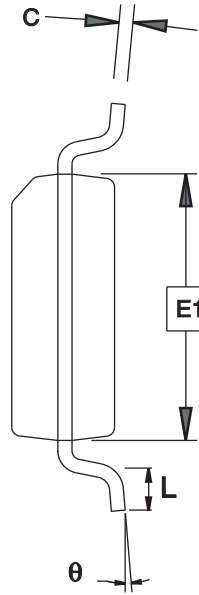
7.1 8P3



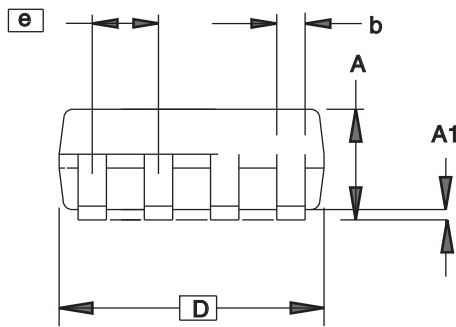
7.2 8S2



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|----------|----------|-----|------|------|
| A | 1.70 | | 2.16 | |
| A1 | 0.05 | | 0.25 | |
| b | 0.35 | | 0.48 | 4 |
| C | 0.15 | | 0.35 | 4 |
| D | 5.13 | | 5.35 | |
| E1 | 5.18 | | 5.40 | 2 |
| E | 7.70 | | 8.26 | |
| L | 0.51 | | 0.85 | |
| θ | 0° | | 8° | |
| e | 1.27 BSC | | | 3 |

- Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
 2. Mismatch of the upper and lower dies and resin burrs aren't included.
 3. Determines the true geometric position.
 4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

4/15/08



Package Drawing Contact:
packagedrawings@atmel.com

TITLE
8S2, 8-lead, 0.208" Body, Plastic Small
Outline Package (EIAJ)

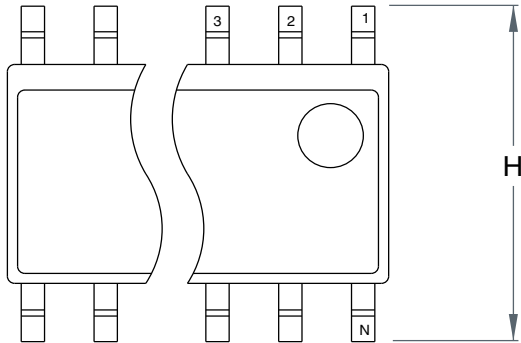
GPC
STN

DRAWING NO.
8S2

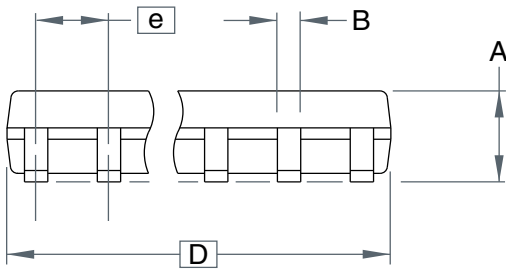
REV.
F



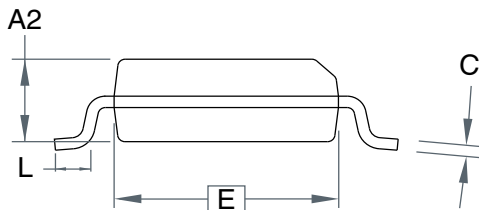
7.3 S8S1



Top View



Side View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|------|------|
| A | - | - | 1.75 | |
| B | - | - | 0.51 | |
| C | - | - | 0.25 | |
| D | - | - | 5.00 | |
| E | - | - | 4.00 | |
| e | 1.27 BSC | | | |
| H | - | - | 6.20 | |
| L | - | - | 1.27 | |

Note: This drawing is for general information only. Refer to JEDEC Drawing MS-012 for proper dimensions, tolerances, datums, etc.

10/10/01



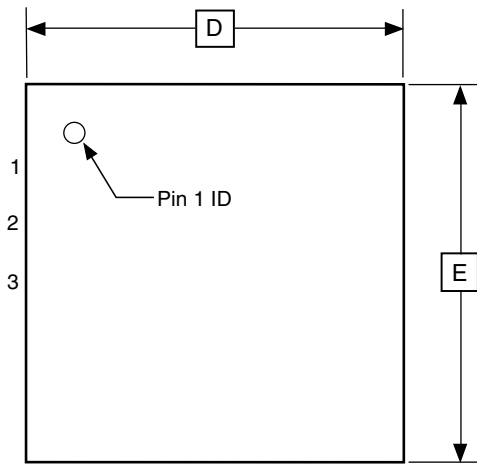
2325 Orchard Parkway
San Jose, CA 95131

TITLE
8S1, 8-lead (0.150" Wide Body), Plastic Gull Wing
Small Outline (JEDEC SOIC)

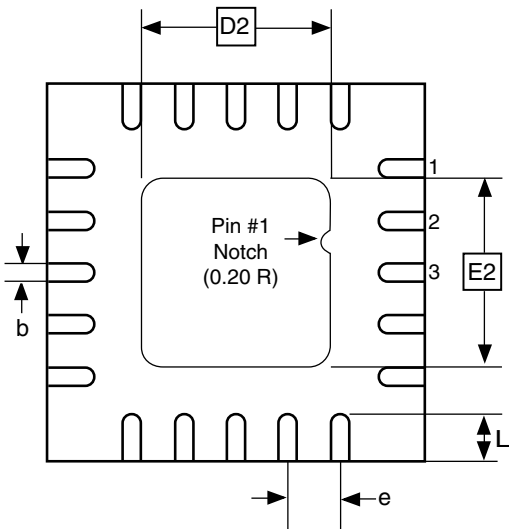
DRAWING NO.
8S1

REV.
A

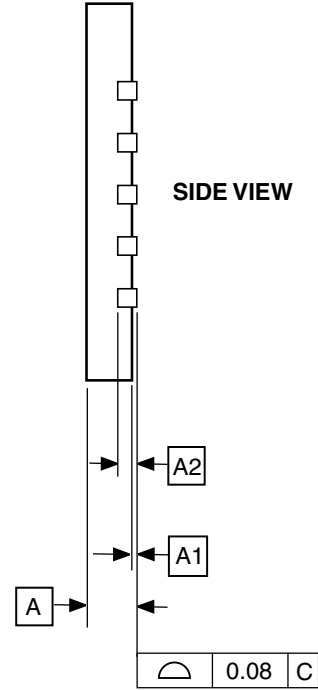
7.4 20M1



TOP VIEW



BOTTOM VIEW



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|------|
| A | 0.70 | 0.75 | 0.80 | |
| A1 | - | 0.01 | 0.05 | |
| A2 | 0.20 REF | | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 4.00 BSC | | | |
| D2 | 2.45 | 2.60 | 2.75 | |
| E | 4.00 BSC | | | |
| E2 | 2.45 | 2.60 | 2.75 | |
| e | 0.50 BSC | | | |
| L | 0.35 | 0.40 | 0.55 | |

Note: Reference JEDEC Standard MO-220, Fig.1 (SAW Singulation) WGGD-5.

10/27/04



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20M1, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm,
2.6 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

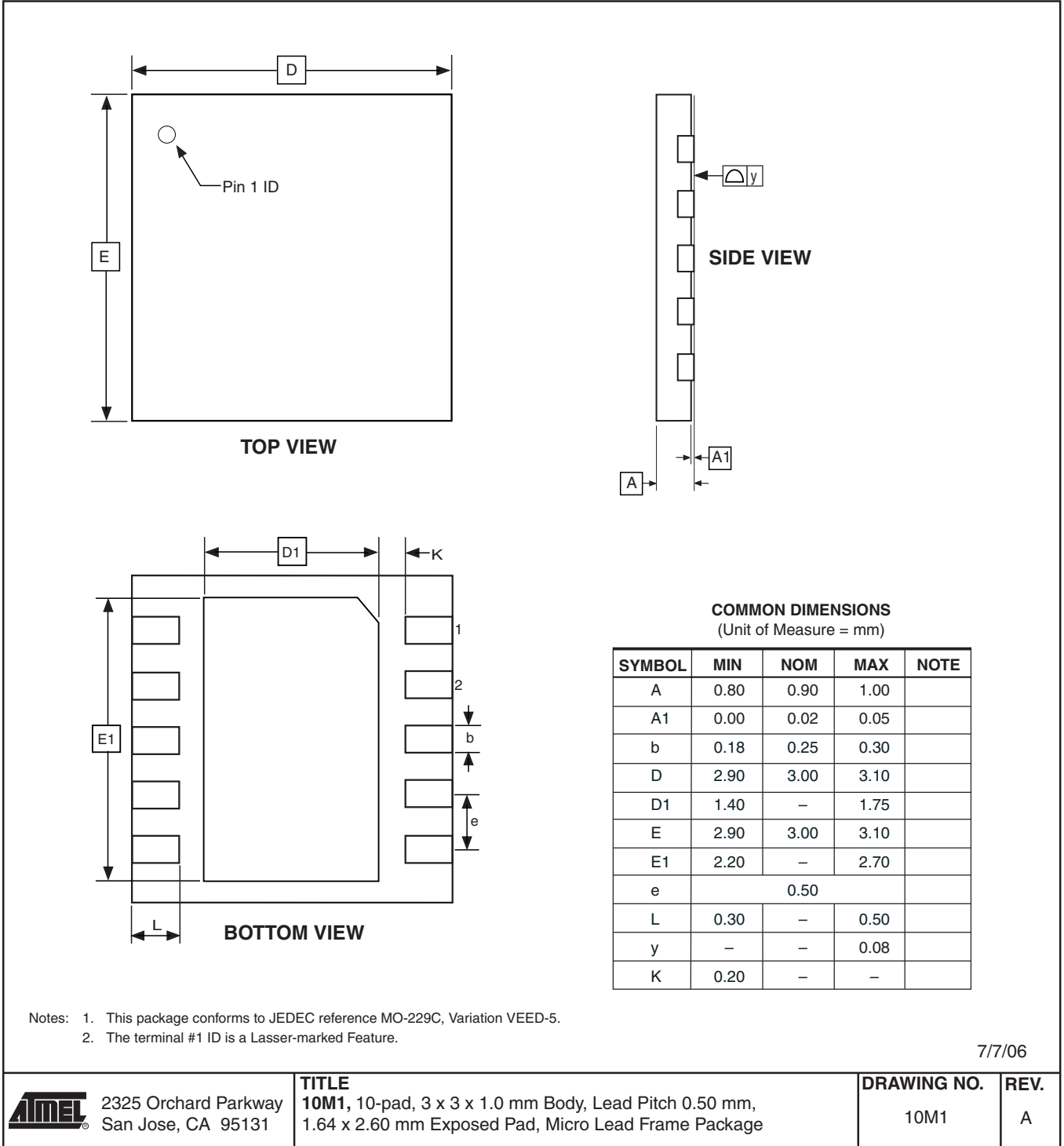
20M1

REV.

A



7.5 10M1



8. Errata

The revision letter in this section refers to the revision of the ATtiny13 device.

8.1 ATtiny13 Rev. D

- **EEPROM can not be written below 1.9 Volt**

1. **EEPROM can not be written below 1.9 Volt**

Writing the EEPROM at V_{CC} below 1.9 volts might fail.

Problem Fix/Workaround

Do not write the EEPROM when V_{CC} is below 1.9 volts.

8.2 ATtiny13 Rev. C

Revision C has not been sampled.

8.3 ATtiny13 Rev. B

- **Wrong values read after Erase Only operation**
- **High Voltage Serial Programming Flash, EEPROM, Fuse and Lock Bits may fail**
- **Device may lock for further programming**
- **debugWIRE communication not blocked by lock-bits**
- **Watchdog Timer Interrupt disabled**
- **EEPROM can not be written below 1.9 Volt**

8.3.1 **Wrong values read after Erase Only operation**

At supply voltages below 2.7 V, an EEPROM location that is erased by the Erase Only operation may read as programmed (0x00).

Problem Fix/Workaround

If it is necessary to read an EEPROM location after Erase Only, use an Atomic Write operation with 0xFF as data in order to erase a location. In any case, the Write Only operation can be used as intended. Thus no special considerations are needed as long as the erased location is not read before it is programmed.

8.3.2 **High Voltage Serial Programming Flash, EEPROM, Fuse and Lock Bits may fail**

Writing to any of these locations and bits may in some occasions fail.

Problem Fix/Workaround

After a writing has been initiated, always observe the RDY/\overline{BSY} signal. If the writing should fail, rewrite until the RDY/\overline{BSY} verifies a correct writing. This will be fixed in revision D.

8.3.3 **Device may lock for further programming**

Special combinations of fuse bits will lock the device for further programming effectively turning it into an OTP device. The following combinations of settings/fuse bits will cause this effect:

- 128 kHz internal oscillator (CKSEL[1..0] = 11), shortest start-up time (SUT[1..0] = 00), Debugwire enabled (DWEN = 0) or Reset disabled RSTDISBL = 0.
- 9.6 MHz internal oscillator (CKSEL[1..0] = 10), shortest start-up time (SUT[1..0] = 00), Debugwire enabled (DWEN = 0) or Reset disabled RSTDISBL = 0.

- 4.8 MHz internal oscillator (CKSEL[1..0] = 01), shortest start-up time (SUT[1..0] = 00), Debugwire enabled (DWEN = 0) or Reset disabled RSTDISBL = 0.

Problem fix/ Workaround

Avoid the above fuse combinations. Selecting longer start-up time will eliminate the problem.

8.3.4 debugWIRE communication not blocked by lock-bits

When debugWIRE on-chip debug is enabled (DWEN = 0), the contents of program memory and EEPROM data memory can be read even if the lock-bits are set to block further reading of the device.

Problem fix/ Workaround

Do not ship products with on-chip debug of the tiny13 enabled.

8.3.5 Watchdog Timer Interrupt disabled

If the watchdog timer interrupt flag is not cleared before a new timeout occurs, the watchdog will be disabled, and the interrupt flag will automatically be cleared. This is only applicable in interrupt only mode. If the Watchdog is configured to reset the device in the watchdog time-out following an interrupt, the device works correctly.

Problem fix / Workaround

Make sure there is enough time to always service the first timeout event before a new watchdog timeout occurs. This is done by selecting a long enough time-out period.

8.3.6 EEPROM can not be written below 1.9 Volt

Writing the EEPROM at V_{CC} below 1.9 volts might fail.

Problem Fix/Workaround

Do not write the EEPROM when V_{CC} is below 1.9 volts.

8.4 ATtiny13 Rev. A

Revision A has not been sampled.

9. Datasheet Revision History

Please note that the referring page numbers in this section refer to the complete document.

9.1 Rev. 2535J-08/10

Added tape and reel part numbers in [“Ordering Information” on page 160](#). Removed text “Not recommended for new design” from cover page. Updated last page.

9.2 Rev. 2535I-05/08

1. Updated document template, layout and paragraph formats.
2. Updated [“Features” on page 1](#).
3. Created Sections:
 - [“Calibrated Internal RC Oscillator Accuracy” on page 118](#)
 - [“Analog Comparator Characteristics” on page 119](#)
4. Updated Sections:
 - [“System Clock and Clock Options” on page 23](#)
 - [“Calibrated Internal 4.8/9.6 MHz Oscillator” on page 25](#)
 - [“External Interrupts” on page 45](#)
 - [“Analog Noise Canceling Techniques” on page 88](#)
 - [“Limitations of debugWIRE” on page 96](#)
 - [“Reading Fuse and Lock Bits from Firmware” on page 99](#)
 - [“Fuse Bytes” on page 103](#)
 - [“Calibration Bytes” on page 104](#)
 - [“High-Voltage Serial Programming” on page 108](#)
 - [“Ordering Information” on page 160](#)
5. Updated Figure:
 - [“Analog Input Circuitry” on page 87](#)
 - [“High-voltage Serial Programming Timing” on page 122](#)
6. Moved Figures:
 - [“Serial Programming Timing” on page 121](#)
 - [“Serial Programming Waveform” on page 121](#)
 - [“High-voltage Serial Programming Timing” on page 122](#)
7. Updated Tables:
 - [“DC Characteristics, \$T_A = -40^{\circ}\text{C}\$ to \$+85^{\circ}\text{C}\$ ” on page 115](#)
 - [“Serial Programming Characteristics, \$T_A = -40^{\circ}\text{C}\$ to \$+85^{\circ}\text{C}\$, \$V_{CC} = 1.8 - 5.5\text{V}\$ \(Unless Otherwise Noted\)” on page 121](#)
8. Moved Tables:
 - [“Serial Programming Instruction Set” on page 107](#)
 - [“Serial Programming Characteristics, \$T_A = -40^{\circ}\text{C}\$ to \$+85^{\circ}\text{C}\$, \$V_{CC} = 1.8 - 5.5\text{V}\$ \(Unless Otherwise Noted\)” on page 121](#)
 - [“High-voltage Serial Programming Characteristics \$T_A = 25^{\circ}\text{C}\$, \$V_{CC} = 5.0\text{V} \pm 10\%\$ \(Unless otherwise noted\)” on page 122](#)
9. Updated Register Description for Sections:

- “TCCR0A – Timer/Counter Control Register A” on page 69
- “DIDR0 – Digital Input Disable Register 0” on page 94
- 10. Updated description in [Step 1.](#) on page 106.
- 11. Changed device status to “Not Recommended for New Designs”.

9.3 Rev. 2535H-10/07

1. Updated [“Features”](#) on page 1.
2. Updated [“Pin Configurations”](#) on page 2.
3. Added [“Data Retention”](#) on page 6.
4. Updated [“Assembly Code Example^{\(1\)}”](#) on page 39.
5. Updated Table 21 in [“Alternate Functions of Port B”](#) on page 54.
6. Updated Bit 5 description in [“GIMSK – General Interrupt Mask Register”](#) on page 46.
7. Updated [“ADC Voltage Reference”](#) on page 87.
8. Updated [“Calibration Bytes”](#) on page 104.
9. Updated [“Read Calibration Byte”](#) on page 108.
10. Updated Table 51 in [“Serial Programming Characteristics”](#) on page 121.
11. Updated Algorithm in [“High-Voltage Serial Programming Algorithm”](#) on page 109.
12. Updated [“Read Calibration Byte”](#) on page 112.
13. Updated values in [“External Clock Drive”](#) on page 118.
14. Updated [“Ordering Information”](#) on page 160.
15. Updated [“Packaging Information”](#) on page 161.

9.4 Rev. 2535G-01/07

1. Removed Preliminary.
2. Updated [Table 7-1](#) on page 30, [Table 8-1](#) on page 42, [Table 18-8](#) on page 121.
3. Removed Note from [Table 7-1](#) on page 30.
4. Updated [“Bit 6 – ADBG: Analog Comparator Bandgap Select”](#) on page 79.
5. Updated [“Prescaling and Conversion Timing”](#) on page 83.
6. Updated [Figure 18-4](#) on page 121.
7. Updated [“DC Characteristics”](#) on page 115.
8. Updated [“Ordering Information”](#) on page 160.
9. Updated [“Packaging Information”](#) on page 161.

9.5 Rev. 2535F-04/06

1. Revision not published.

9.6 Rev. 2535E-10/04

1. Bits EEMWE/EEWE changed to EEMPE/EEPE in document.
2. Updated [“Pinout ATtiny13/ATtiny13V”](#) on page 2.
3. Updated [“Write Fuse Low Bits”](#) in [Table 17-13](#) on page 110, [Table 18-3](#) on page 118.
2. Added [“Pin Change Interrupt Timing”](#) on page 45.
4. Updated [“GIMSK – General Interrupt Mask Register”](#) on page 46.
5. Updated [“PCMSK – Pin Change Mask Register”](#) on page 47.
6. Updated item 4 in [“Serial Programming Algorithm”](#) on page 106.
7. Updated [“High-Voltage Serial Programming Algorithm”](#) on page 109.

8. Updated [“DC Characteristics”](#) on page 115.
9. Updated [“Typical Characteristics”](#) on page 122.
10. Updated [“Ordering Information”](#) on page 160.
11. Updated [“Packaging Information”](#) on page 161.
12. Updated [“Errata”](#) on page 166.

9.7 Rev. 2535D-04/04

1. Maximum Speed Grades changed: 12MHz to 10MHz, 24MHz to 20MHz
2. Updated [“Serial Programming Instruction Set”](#) on page 107.
3. Updated [“Speed Grades”](#) on page 117
4. Updated [“Ordering Information”](#) on page 160

9.8 Rev. 2535C-02/04

1. C-code examples updated to use legal IAR syntax.
2. Replaced occurrences of WDIF with WDTIF and WDIE with WDTIE.
3. Updated [“Stack Pointer”](#) on page 11.
4. Updated [“Calibrated Internal 4.8/9.6 MHz Oscillator”](#) on page 25.
5. Updated [“OSCCAL – Oscillator Calibration Register”](#) on page 27.
6. Updated typo in introduction on [“Watchdog Timer”](#) on page 37.
7. Updated [“ADC Conversion Time”](#) on page 86.
8. Updated [“Serial Programming”](#) on page 105.
9. Updated [“Electrical Characteristics”](#) on page 115.
10. Updated [“Ordering Information”](#) on page 160.
11. Removed rev. C from [“Errata”](#) on page 166.

9.9 Rev. 2535B-01/04

1. Updated [Figure 2-1](#) on page 4.
2. Updated [Table 7-1](#), [Table 8-1](#), [Table 14-2](#) and [Table 18-3](#).
3. Updated [“Calibrated Internal 4.8/9.6 MHz Oscillator”](#) on page 25.
4. Updated the whole [“Watchdog Timer”](#) on page 37.
5. Updated [Figure 17-1](#) on page 105 and [Figure 17-2](#) on page 108.
6. Updated registers [“MCUCR – MCU Control Register”](#), [“TCCR0B – Timer/Counter Control Register B”](#) and [“DIDR0 – Digital Input Disable Register 0”](#).
7. Updated Absolute Maximum Ratings and DC Characteristics in [“Electrical Characteristics”](#) on page 115.
8. Added [“Speed Grades”](#) on page 117
9. Updated [“”](#) on page 120.
10. Updated [“Typical Characteristics”](#) on page 123.
11. Updated [“Ordering Information”](#) on page 160.
12. Updated [“Packaging Information”](#) on page 161.
13. Updated [“Errata”](#) on page 166.
14. Changed instances of EEAR to EEARL.

9.10 Rev. 2535A-06/03

1. Initial Revision.



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